74ALVCH16374

2.5 V/3.3 V 16-bit edge-triggered D-type flip-flop; 3-state

Rev. 6.1 — 7 March 2019 Product data sheet

1. General description

The 74ALVCH16374 is 16-bit edge-triggered flip-flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications.

Incorporates bus hold data inputs which eliminate the need for external pull-up or pull-down resistors to hold unused inputs.

The 74ALVCH16374 consists of 2 sections of eight edge-triggered flip-flops. A clock (CP) input and an output enable ($\overline{OE}$) are provided per 8-bit section.

The flip-flops will store the state of their individual D-inputs that meet the set-up and hold time requirements on the LOW-to-HIGH CP transition.

When $\overline{OE}$ is LOW, the contents of the flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go the high-impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standard JESD8-B
- CMOS low power consumption
- MULTIBYTE flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels
- All data inputs have bus hold
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at V_{CC} = 3.0 V

3. Ordering information

Table 1. Ordering information

Type number	Temperature range	Package		
		Name	Description	Version
74ALVCH16374DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4. Functional diagram

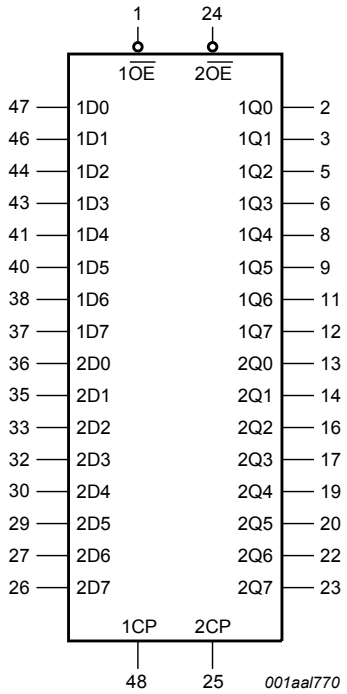


Fig. 1. Logic symbol

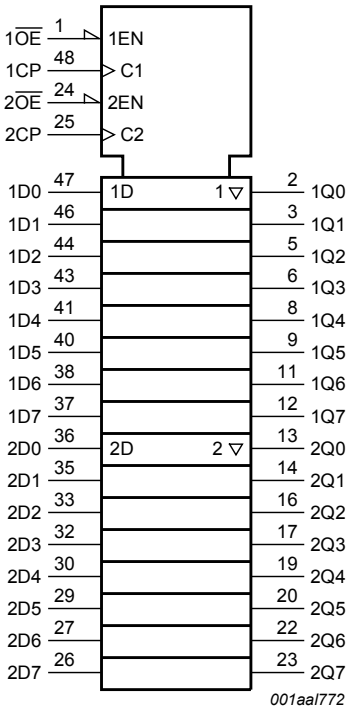


Fig. 2. IEC logic symbol

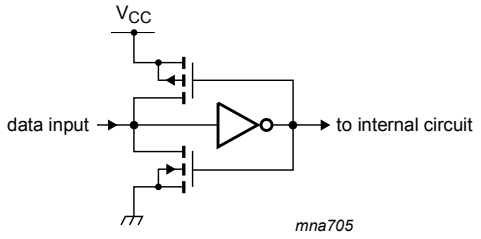


Fig. 3. Bus hold circuit

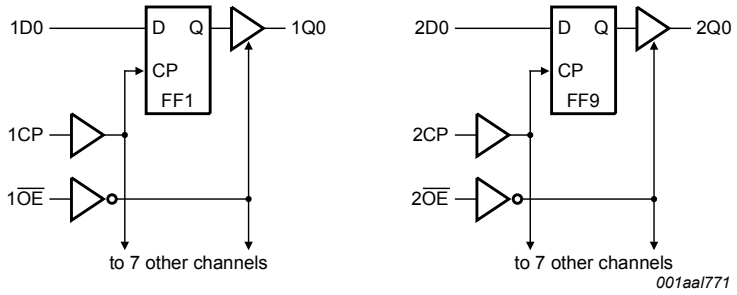


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

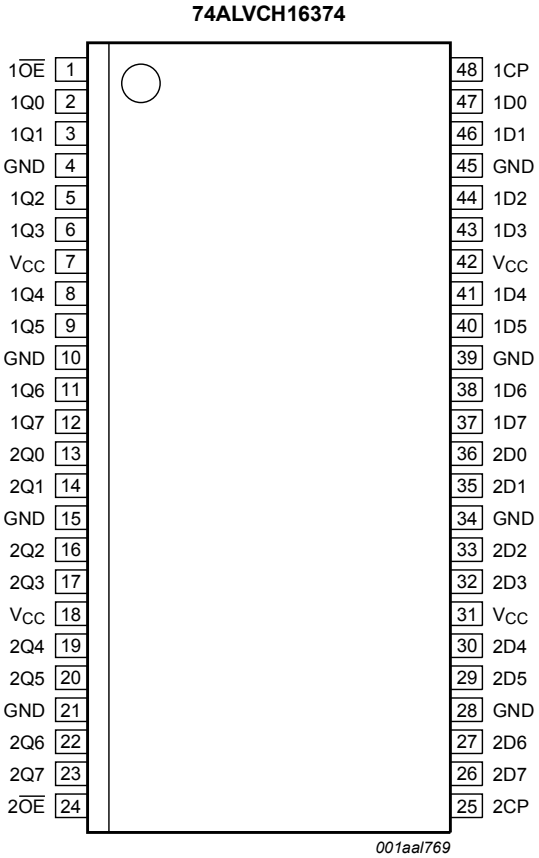


Fig. 5. Pin configuration SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{OE}$, 2$\overline{OE}$	1, 24	output enable input (active LOW)
1Q0, 1Q1, 1Q2, 1Q3, 1Q4, 1Q5, 1Q6, 1Q7	2, 3, 5, 6, 8, 9, 11, 12	3-state flip-flop outputs
2Q0, 2Q1, 2Q2, 2Q3, 2Q4, 2Q5, 2Q6, 2Q7	13, 14, 16, 17, 19, 20, 22, 23	3-state flip-flop outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	positive supply voltage
1D0, 1D1, 1D2, 1D3, 1D4, 1D5, 1D6, 1D7	47, 46, 44, 43, 41, 40, 38, 37	data inputs
2D0, 2D1, 2D2, 2D3, 2D4, 2D5, 2D6, 2D7	36, 35, 33, 32, 30, 29, 27, 26	data inputs
1CP, 2CP	48, 25	clock input

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;
L = LOW voltage level; l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;
↑ = LOW-to-HIGH clock transition;
Z = high-impedance OFF-state.

Inputs			Internal flip-flops	Outputs Q0 to Q7	Operating mode
n$\overline{OE}$	nCP	nDn			
L	↑	l	L	L	load and read register
L	↑	h	H	H	
H	↑	l	L	Z	load register and disable outputs
H	↑	h	H	Z	

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		-50	-	mA
V_I	input voltage	control inputs	[1]	-0.5	+4.6	V
		data inputs	[1]	-0.5	V_{CC} + 0.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V		-	±50	mA
V_O	output voltage		[1]	-0.5	V_{CC} + 0.5	V
I_O	output current	V_O = 0 V to V_{CC}		-	±50	mA
I_{CC}	supply current			-	100	mA
I_{GND}	ground current			-100	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C;	[2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] Above 55 °C the value of P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage	maximum speed performance				
		C_L = 30 pF	2.3	-	2.7	V
		C_L = 50 pF	3.0	-	3.6	V
		low voltage applications	1.2	-	3.6	V
V_I	input voltage	data inputs	0	-	V_{CC}	V
		control inputs	0	-	5.5	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.3 V to 3.0 V	0	-	20	ns/V
		V_{CC} = 3.0 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	V_{CC}	-	-	V
		V_{CC} = 1.8 V	$0.7V_{CC}$	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.7	1.2	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	1.5	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0	V
		V_{CC} = 1.8 V	-	0.9	$0.2V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	1.2	0.7	V
		V_{CC} = 2.7 V to 3.6 V	-	1.5	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = -100 µA; V_{CC} = 1.8 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_O = -6 mA; V_{CC} = 1.8 V	V_{CC} - 0.4	V_{CC} - 0.1	-	V
		I_O = -6 mA; V_{CC} = 2.3 V	V_{CC} - 0.3	V_{CC} - 0.08	-	V
		I_O = -12 mA; V_{CC} = 2.3 V	V_{CC} - 0.5	V_{CC} - 0.17	-	V
		I_O = -12 mA; V_{CC} = 2.7 V	V_{CC} - 0.5	V_{CC} - 0.14	-	V
		I_O = -18 mA; V_{CC} = 2.3 V	V_{CC} - 0.6	V_{CC} - 0.26	-	V
		I_O = -24 mA; V_{CC} = 3.0 V	V_{CC} - 1.0	V_{CC} - 0.28	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 100 µA; V_{CC} = 1.8 V to 3.6 V	-	0	0.20	V
		I_O = 6 mA; V_{CC} = 1.8 V	-	0.09	0.30	V
		I_O = 6 mA; V_{CC} = 2.3 V	-	0.07	0.20	V
		I_O = 12 mA; V_{CC} = 2.3 V	-	0.15	0.40	V
		I_O = 12 mA; V_{CC} = 2.7 V	-	0.14	0.40	V
		I_O = 18 mA; V_{CC} = 2.3 V	-	0.23	0.60	V
		I_O = 24 mA; V_{CC} = 3.0 V	-	0.27	0.55	V

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_I	input leakage current	V_{CC} = 1.8 V to 3.6 V				
		control input; V_I = 5.5 V or GND	-	0.1	5	µA
		data input; V_I = V_{CC} or GND	-	0.1	5	µA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_O = V_{CC} or GND				
		V_{CC} = 1.8 V to 2.7 V	-	0.1	5	µA
		V_{CC} = 2.7 V to 3.6 V	-	0.1	10	µA
I_{LIZ}	OFF-state input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 1.8 V to 2.7 V	-	0.1	10	µA
		V_{CC} = 3.6 V	-	0.1	15	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A;				
		V_{CC} = 1.8 V to 2.7 V	-	0.1	20	µA
		V_{CC} = 2.7 V to 3.6 V	-	0.2	40	µA
ΔI_{CC}	additional supply current	V_I = V_{CC} - 0.6 V; I_O = 0 A; V_{CC} = 2.7 V to 3.6 V				
		per control input	-	5	500	µA
		per data I/O input	-	150	750	µA
I_{BHL}	bus hold LOW current	V_{CC} = 2.3 V; V_I = 0.7 V [2]	45	-	-	µA
		V_{CC} = 3.0 V; V_I = 0.8 V [2]	75	150	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 2.3 V; V_I = 1.7 V [2]	-45	-	-	µA
		V_{CC} = 3.0 V; V_I = 2.0 V [2]	-75	-175	-	µA
I_{BHLO}	bus hold LOW overdrive current	V_{CC} = 2.7 V [2]	300	-	-	µA
		V_{CC} = 3.6 V [2]	450	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	V_{CC} = 2.7 V [2]	-300	-	-	µA
		V_{CC} = 3.6 V [2]	-450	-	-	µA
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
[2] Valid for data inputs of bus hold parts only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V); test circuit Fig. 9.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
f_{max}	maximum frequency	see Fig. 6				
		V_{CC} = 1.8 V	125	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V	150	300	-	MHz
		V_{CC} = 2.7 V	150	300	-	MHz
		V_{CC} = 3.0 V to 3.6 V	200	350	-	MHz
t_{pd}	propagation delay	nCP to nQn; see Fig. 6 [2]				
		V_{CC} = 1.2 V	-	7.7	-	ns
		V_{CC} = 1.8 V	1.5	3.6	6.5	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.3	4.3	ns
		V_{CC} = 2.7 V	1.0	2.3	3.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.4	3.4	ns

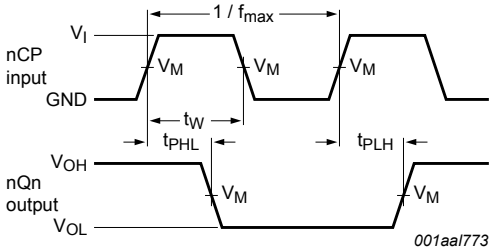
Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_{en}	enable time	$n\overline{OE}$ to nQn; see Fig. 7 [2]				
		V_{CC} = 1.2 V	-	8.7	-	ns
		V_{CC} = 1.8 V	1.5	4.0	7.2	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.6	4.8	ns
		V_{CC} = 2.7 V	1.0	2.9	4.8	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t_{dis}	disable time	$n\overline{OE}$ to nQn; see Fig. 7 [2]				
		V_{CC} = 1.2 V	-	6.2	-	ns
		V_{CC} = 1.8 V	1.5	3.1	5.4	ns
		V_{CC} = 2.3 V to 2.7 V	1.0	2.1	4.0	ns
		V_{CC} = 2.7 V	1.0	2.9	4.5	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.6	4.1	ns
t_W	pulse width	nCP HIGH or LOW; see Fig. 6				
		V_{CC} = 1.8 V	4.0	2.0	-	ns
		V_{CC} = 2.3 V to 2.7 V	3.0	1.6	-	ns
		V_{CC} = 2.7 V	3.0	1.6	-	ns
		V_{CC} = 3.0 V to 3.6 V	2.5	1.4	-	ns
t_{su}	set-up time	nDn to nCP; see Fig. 8				
		V_{CC} = 1.8 V	1.5	0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	1.2	0.2	-	ns
		V_{CC} = 2.7 V	1.5	0.4	-	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	0.2	-	ns
t_h	hold time	nDn to nCP; see Fig. 8				
		V_{CC} = 1.8 V	0.6	-0.2	-	ns
		V_{CC} = 2.3 V to 2.7 V	0.8	-0.1	-	ns
		V_{CC} = 2.7 V	0.6	-0.2	-	ns
		V_{CC} = 3.0 V to 3.6 V	0.8	0.0	-	ns
C_{PD}	power dissipation capacitance	per flip-flop; V_I = GND to V_{CC} [3]				
		outputs enabled	-	16	-	pF
		outputs disabled	-	10	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.
Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in Volts;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

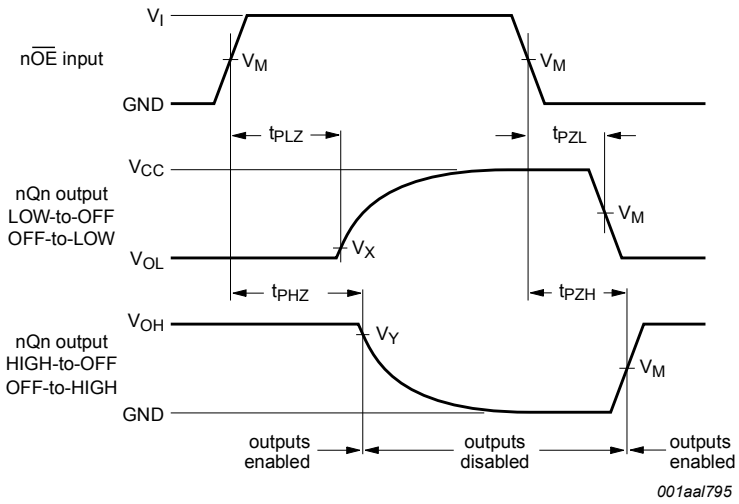
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

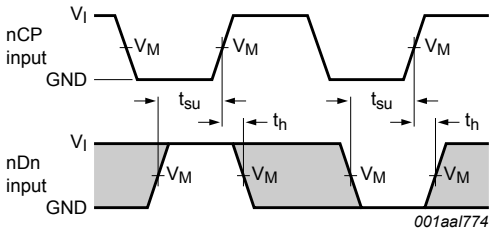
Fig. 6. Propagation delay, clock input (nCP) to data output (nQn), and pulse width



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical output levels that occur with the output load.

Fig. 7. 3-state enable and disable times



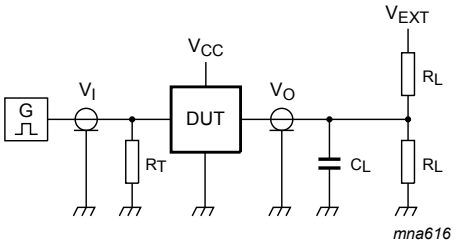
Measurement points are given in Table 8.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 8. Data setup and hold times for input (nDn) to input (nCP)

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V and < 2.3 V	V_{CC}	0.5 × V_{CC}	0.5 × V_{CC}	V_{OL} + 0.15 V	V_{OH} - 0.15 V
2.7 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

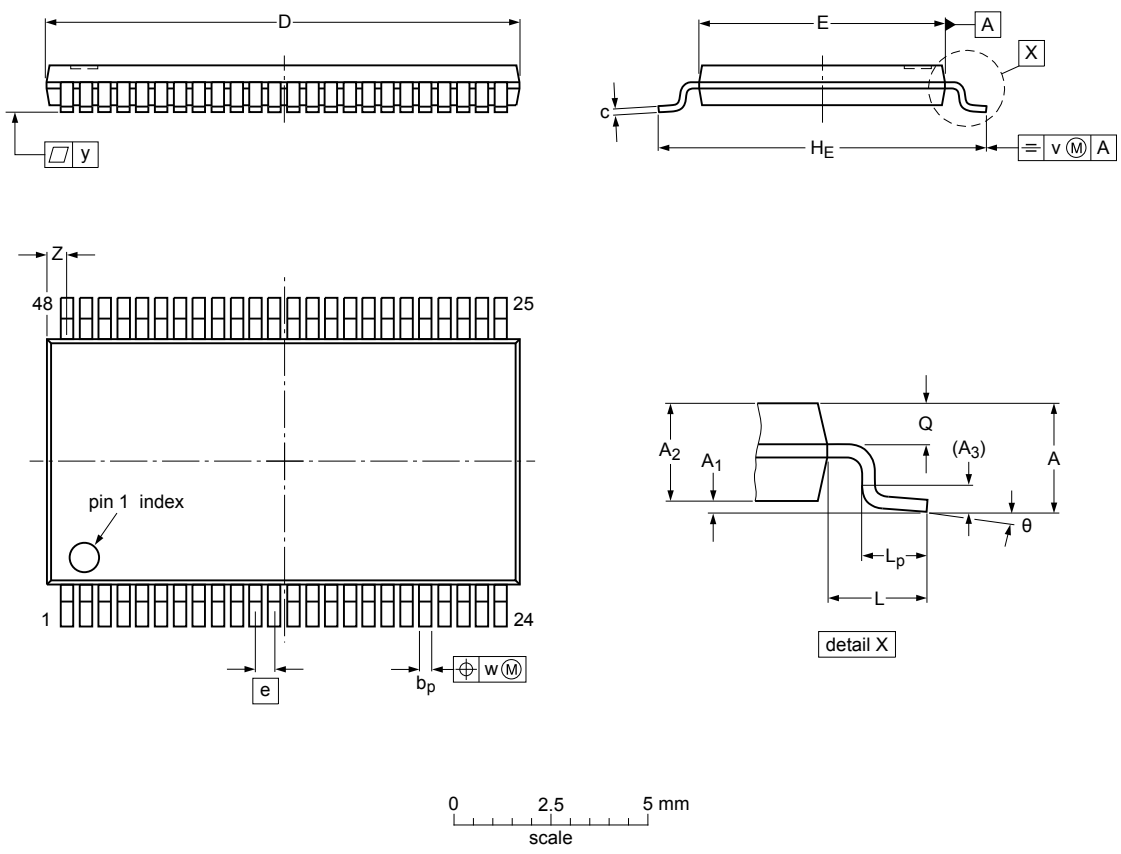
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V and < 2.3 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	2 × V_{CC}	GND
2.7 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND
3.0 V to 3.6 V	2.7 V	2.5 ns	50 pF	500 Ω	open	2 × V_{CC}	GND

11. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit	A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
mm nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
mm min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig. 10. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH16374 v.6.1	20190307	Product data sheet	-	74ALVCH16374 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ALVCH16374DL (SOT370-1) removed. • Removed typo in Table 1.			
74ALVCH16374 v.5	20120709	Product data sheet	-	74ALVCH16374 v.4
Modifications:	• Table 8 corrected (errata).			
74ALVCH16374 v.4	20111117	Product data sheet	-	74ALVCH16374 v.3
Modifications:	• Legal pages updated.			
74ALVCH16374 v.3	20100427	Product data sheet	-	74ALVCH16374 v.2
74ALVCH16374 v.2	19980618	Product specification	-	74ALVCH16374 v.1

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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