

# 74AVC16245

16-bit transceiver with direction pin; 3.6 V tolerant; 3-state

Rev. 3 — 31 January 2013

Product data sheet

## 1. General description

The 74AVC16245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. The device features two output enable inputs ( $\overline{\text{nOE}}$ ) for easy cascading and two send/receive inputs ( $\overline{\text{nDIR}}$ ) for direction control. Inputs  $\overline{\text{nOE}}$  control the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74AVC16245 is designed to have an extremely fast propagation delay and a minimum amount of power consumption.

To ensure the high-impedance output state during power-up or power-down, tie pins  $\overline{\text{nOE}}$  to  $V_{\text{CC}}$  through a pull-up resistor (Live Insertion).

A Dynamic Controlled Output (DCO) circuitry is implemented to support termination line drive during transient (see [Figure 4](#) and [Figure 5](#))

## 2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- Complies with JEDEC standards:
  - ◆ JESD8-7 (1.2 V to 1.95 V)
  - ◆ JESD8-5 (1.8 V to 2.7 V)
  - ◆ JESD8-1A (2.7 V to 3.6 V)
- CMOS low power consumption
- Input/output tolerant up to 3.6 V
- Dynamic Controlled Output (DCO) circuit dynamically changes output impedance, resulting in noise reduction without speed degradation
- Low inductance multiple VCC and GND pins to minimize noise and ground bounce
- Supports Live Insertion

## 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74AVC16245DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

nexperia

4. Functional diagram

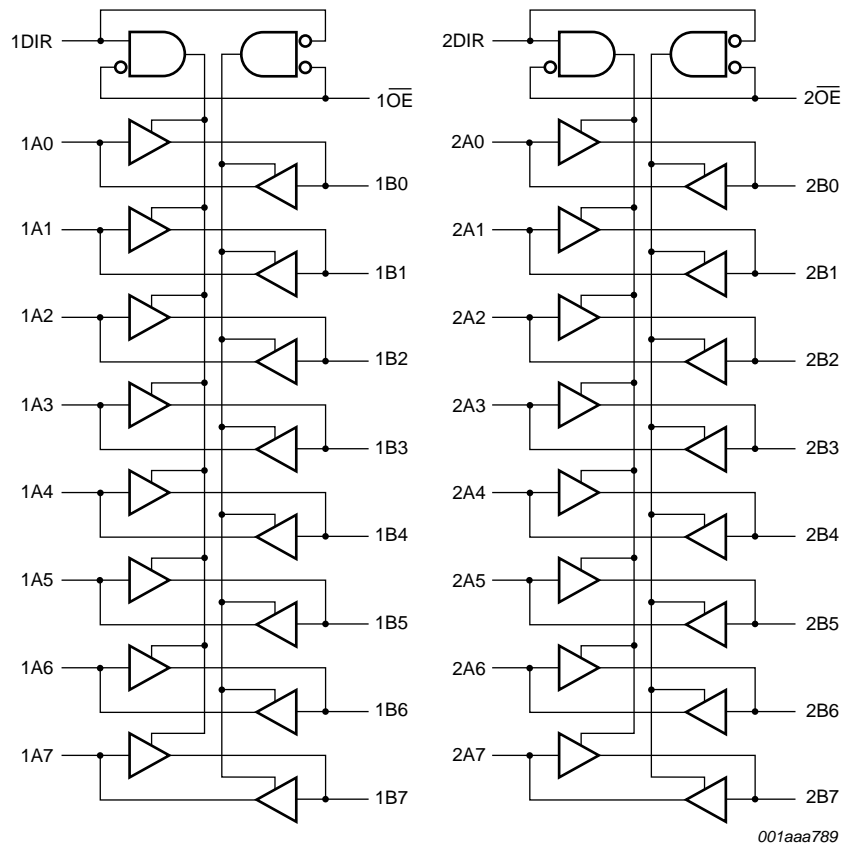


Fig 1. Logic symbol

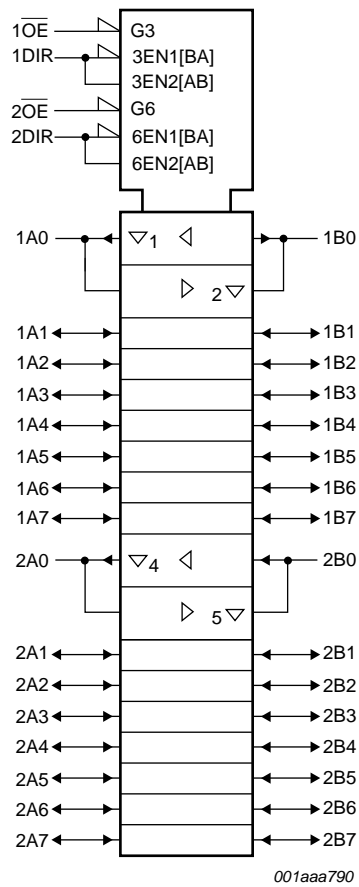
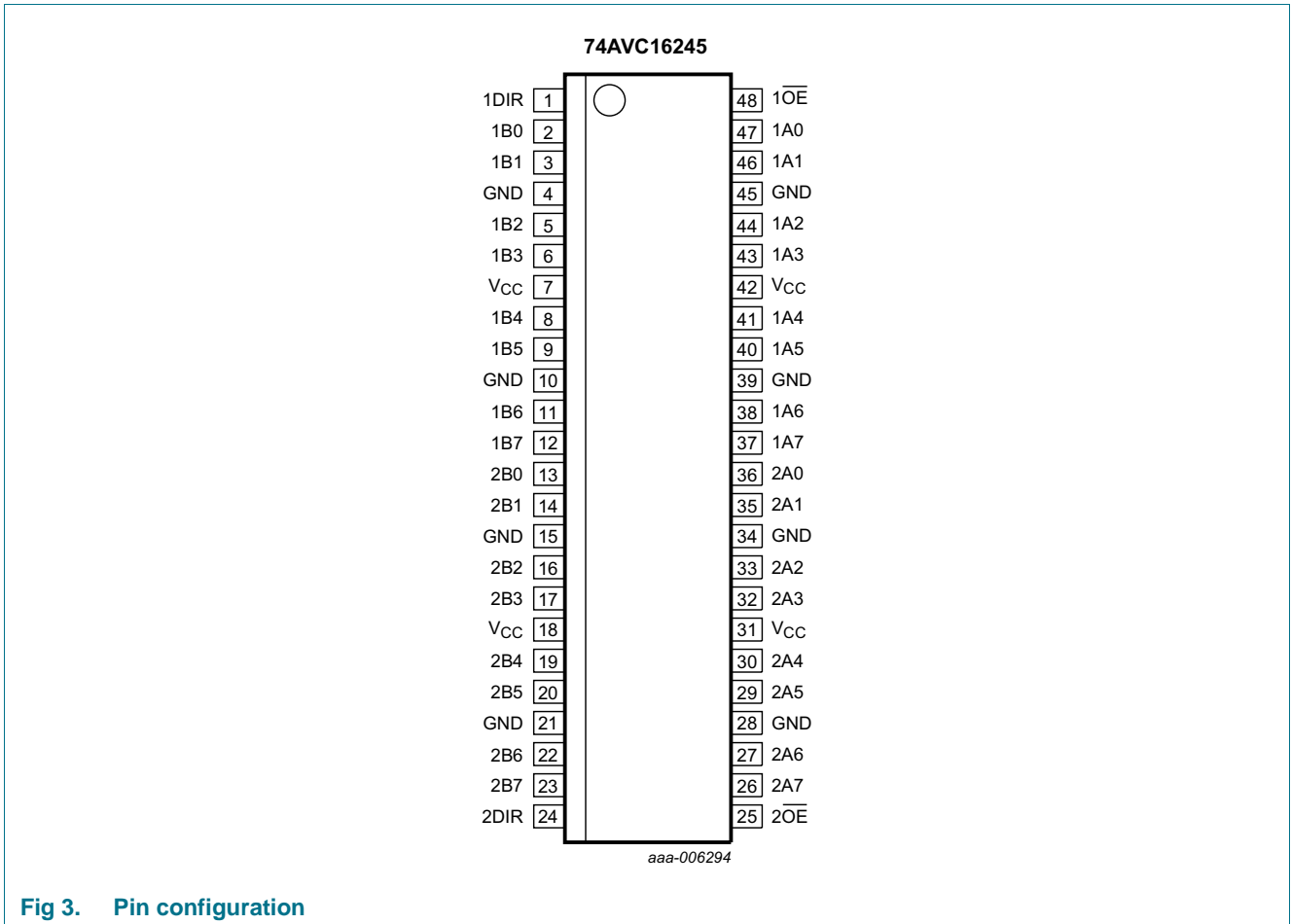


Fig 2. IEC logic symbol

## 5. Pinning information

### 5.1 Pinning



## 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1B0 to 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0 to 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V <sub>CC</sub>	7, 18, 31, 42	supply voltage
1 $\overline{\text{OE}}$ , 2 $\overline{\text{OE}}$	48, 25	output enable input (active LOW)
1A0 to 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0 to 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output

## 6. Functional description

Table 3. Function table<sup>[1]</sup>

Inputs		Outputs	
nOE	nDIR	nAn	nBn
L	L	A = B	inputs
L	H	inputs	B = A
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>CC</sub>	supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < 0 V	-50	-	mA
V <sub>I</sub>	input voltage		[1] -0.5	+4.6	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < 0 V	-50	-	mA
V <sub>O</sub>	output voltage	output HIGH or LOW	[1] -0.5	V <sub>CC</sub> + 0.5	V
		output 3-state	[1] -0.5	+4.6	V
I <sub>O</sub>	output current	V <sub>O</sub> = 0 V to V <sub>CC</sub>	-	±50	mA
I <sub>CC</sub>	supply current		-	100	mA
I <sub>GND</sub>	ground current		-100	-	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = -40 °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] Above 60 °C, the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>CC</sub>	supply voltage	according to JEDEC Low Voltage Standards	1.4	-	1.6	V
			1.65	-	1.95	V
			2.3	-	2.7	V
			3.0	-	3.6	V
		for low-voltage applications	1.2	-	3.6	V
V <sub>I</sub>	input voltage		0	-	3.6	V
V <sub>O</sub>	output voltage	output HIGH or LOW	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	3.6	V
T <sub>amb</sub>	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC</sub> = 1.4 V to 1.6 V	0	-	40	ns/V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0	-	30	ns/V
		V <sub>CC</sub> = 2.3 V to 3.0 V	0	-	20	ns/V
		V <sub>CC</sub> = 3.0 V to 3.6 V	0	-	10	ns/V

## 9. Static characteristics

**Table 6. Static characteristics**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
<b>T<sub>amb</sub> = -40 °C to +85 °C</b>						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC</sub> = 1.2 V	V <sub>CC</sub>	-	-	V
		V <sub>CC</sub> = 1.4 V to 1.6 V	0.65 × V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>	0.9	-	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7	1.2	-	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	2.0	1.5	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC</sub> = 1.2 V	-	-	GND	V
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	0.9	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 1.65 V to 1.95 V	-	0.9	0.35 × V <sub>CC</sub>	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	-	1.2	0.7	V
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	1.5	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = -100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	V <sub>CC</sub> - 0.20	V <sub>CC</sub>	-	V
		I <sub>O</sub> = -3 mA; V <sub>CC</sub> = 1.4 V	V <sub>CC</sub> - 0.35	V <sub>CC</sub> - 0.21	-	V
		I <sub>O</sub> = -4 mA; V <sub>CC</sub> = 1.65 V	V <sub>CC</sub> - 0.45	V <sub>CC</sub> - 0.25	-	V
		I <sub>O</sub> = -8 mA; V <sub>CC</sub> = 2.3 V	V <sub>CC</sub> - 0.55	V <sub>CC</sub> - 0.37	-	V
		I <sub>O</sub> = -12 mA; V <sub>CC</sub> = 3.0 V	V <sub>CC</sub> - 0.70	V <sub>CC</sub> - 0.47	-	V

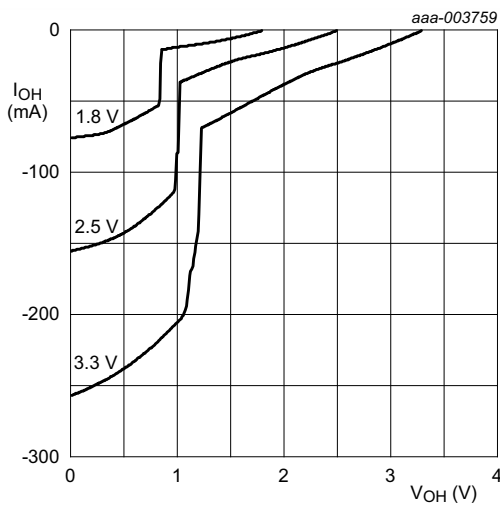
**Table 6. Static characteristics ...continued**

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

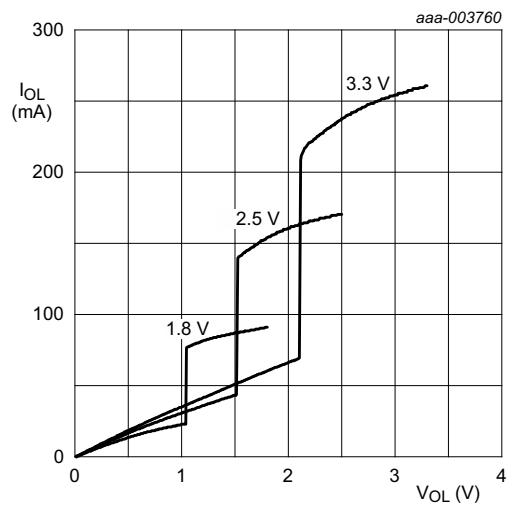
Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		I <sub>O</sub> = 100 μA; V <sub>CC</sub> = 1.65 V to 3.6 V	-	GND	0.20	V
		I <sub>O</sub> = 3 mA; V <sub>CC</sub> = 1.4 V	-	0.22	0.35	V
		I <sub>O</sub> = 4 mA; V <sub>CC</sub> = 1.65 V	-	0.24	0.45	V
		I <sub>O</sub> = 8 mA; V <sub>CC</sub> = 2.3 V	-	0.38	0.55	V
		I <sub>O</sub> = 12 mA; V <sub>CC</sub> = 3.0 V	-	0.53	0.70	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND; V <sub>CC</sub> = 1.4 V to 3.6 V	-	0.1	2.5	μA
I <sub>OFF</sub>	power-off leakage current	V <sub>I</sub> or V <sub>O</sub> = 3.6 V; V <sub>CC</sub> = 0.0 V	-	±0.1	±10	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = V <sub>CC</sub> or GND				
		V <sub>CC</sub> = 1.4 V to 2.7 V	-	0.1	5	μA
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.1	10	μA
I <sub>CC</sub>	supply current	V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0 A				
		V <sub>CC</sub> = 1.4 V to 2.7 V	-	0.1	20	μA
		V <sub>CC</sub> = 3.0 V to 3.6 V	-	0.2	40	μA
C <sub>I</sub>	input capacitance		-	5.0	-	pF

[1] All typical values are measured at T<sub>amb</sub> = 25 °C.

### 9.1 Graphs



**Fig 4. Output voltage as a function of the HIGH-level output current.**



**Fig 5. Output voltage as a function of the LOW-level output current.**

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

 Voltages are referenced to GND (ground = 0 V). For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	–40 °C to +85 °C			Unit
			Min	Typ <sup>[2]</sup>	Max	
t <sub>pd</sub>	propagation delay	nAn to nBn; nBn to nAn; see <a href="#">Figure 6</a> <sup>[1]</sup>				
		V <sub>CC</sub> = 1.2 V	-	2.8	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	1.8	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	0.7	1.8	3.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.6	1.3	1.9	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.5	1.1	1.7	ns
t <sub>en</sub>	enable time	nOE to nAn, nBn; see <a href="#">Figure 7</a> <sup>[1]</sup>				
		V <sub>CC</sub> = 1.2 V	-	5.9	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	3.9	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	1.4	3.3	6.5	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.0	2.4	4.5	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	0.7	2.0	3.7	ns
t <sub>dis</sub>	disable time	nOE to nAn, nBn; see <a href="#">Figure 7</a> <sup>[1]</sup>				
		V <sub>CC</sub> = 1.2 V	-	6.9	-	ns
		V <sub>CC</sub> = 1.4 V to 1.6 V	-	4.8	-	ns
		V <sub>CC</sub> = 1.65 V to 1.95 V	2.2	3.7	6.0	ns
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.1	2.0	4.2	ns
		V <sub>CC</sub> = 3.0 V to 3.6 V	1.2	2.2	3.7	ns
C <sub>PD</sub>	power dissipation capacitance	per input; V <sub>I</sub> = GND to V <sub>CC</sub> <sup>[3]</sup>				
		outputs enabled	-	42	-	pF
		outputs disabled	-	2	-	pF

[1] t<sub>pd</sub> is the same as t<sub>PLH</sub> and t<sub>PHL</sub>.

t<sub>en</sub> is the same as t<sub>PZL</sub> and t<sub>PZH</sub>.

t<sub>dis</sub> is the same as t<sub>PLZ</sub> and t<sub>PHZ</sub>.

[2] Typical values are measured at T<sub>amb</sub> = 25 °C and V<sub>CC</sub> = 1.2 V, 1.5 V, 1.8 V, 2.5 V and 3.3 V respectively.

[3] C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:

f<sub>i</sub> = input frequency in MHz; f<sub>o</sub> = output frequency in MHz

C<sub>L</sub> = output load capacitance in pF

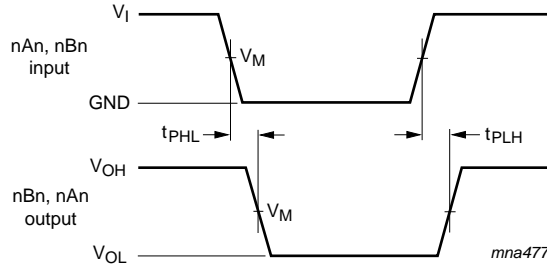
V<sub>CC</sub> = supply voltage in Volts

N = number of inputs switching

$\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

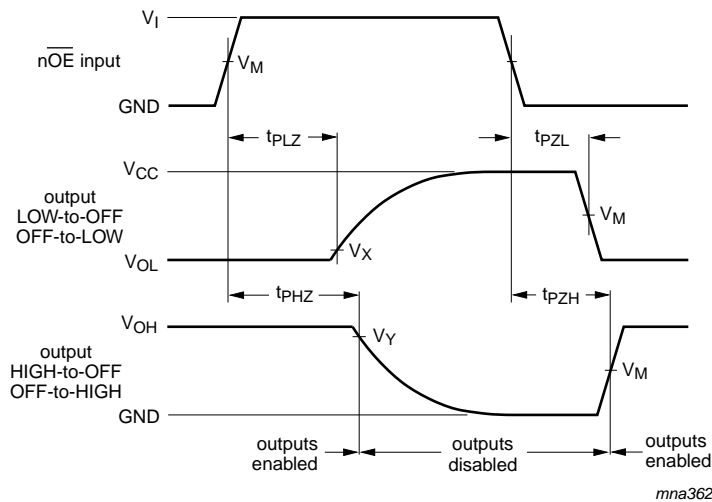


11. Waveforms



Measurement points are given in [Table 8](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 6. The input (nAn, nBn) to output (nBn, nAn) propagation delays**

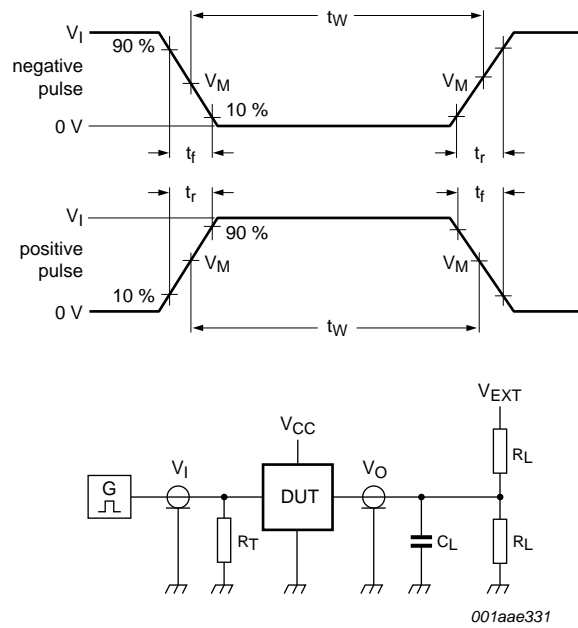


Measurement points are given in [Table 8](#).  
 Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

**Fig 7. 3-state enable and disable times**

**Table 8. Measurement points**

Supply voltage $V_{CC}$	$V_M$	Input			
		$V_I$	$t_r = t_f$	$V_X$	$V_Y$
1.2 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2$ ns	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
1.4 V to 1.6 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2$ ns	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2$ ns	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2$ ns	$V_{OL} + 0.15$ V	$V_{OH} - 0.15$ V
3.0 V to 3.6 V	$0.5 \times V_{CC}$	$V_{CC}$	$\leq 2$ ns	$V_{OL} + 0.3$ V	$V_{OH} - 0.3$ V



Test data is given in [Table 9](#).

Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

$V_{EXT}$  = External voltage for measuring switching times.

**Fig 8. Test circuit for measuring switching times**

**Table 9. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
1.2 V	$V_{CC}$	$\leq 2$ ns	15 pF	2 k $\Omega$	open	$2 \times V_{CC}$	GND
1.4 V to 1.6 V	$V_{CC}$	$\leq 2$ ns	15 pF	2 k $\Omega$	open	$2 \times V_{CC}$	GND
1.65 V to 1.95 V	$V_{CC}$	$\leq 2$ ns	30 pF	1 k $\Omega$	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	$V_{CC}$	$\leq 2$ ns	30 pF	500 $\Omega$	open	$2 \times V_{CC}$	GND

12. Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1

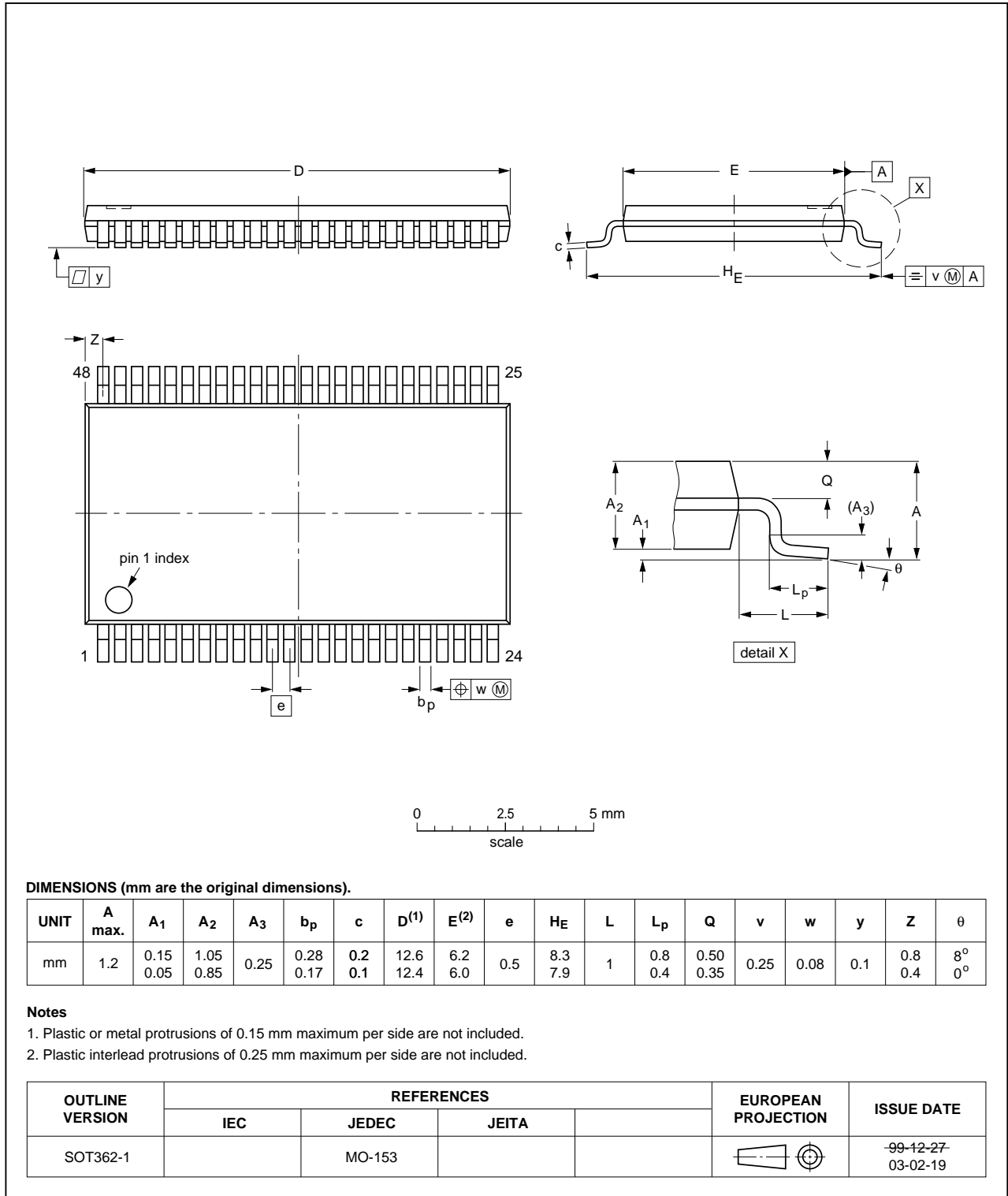


Fig 9. Package outline SOT362-1 (TSSOP48)

## 13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Order number	Supersedes
74AVC16245 v.3	20130131	Product data sheet	-	-	74AVC16245 v.2
Modifications:		<ul style="list-style-type: none"><li>The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li><li>Legal texts have been adapted to the new company name where appropriate.</li></ul>			
74AVC16245 v.2	19991115	Product specification	-	-	74AVC16245 v.1
74AVC16245 v.1	19981211	Product specification	-	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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## 16. Contact information

For more information, please visit: <http://www.nexperia.com>

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