74HC4050

Hex non-inverting HIGH-to-LOW level shifter

Rev. 4 — 5 February 2016 Product data sheet

1. General description

The 74HC4050 is a hex buffer with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V which enables the device to be used in HIGH-to-LOW level shifting applications.

2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4050D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4050DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4050PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

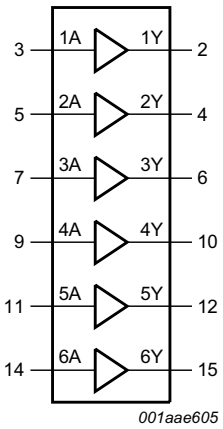


Fig 1. Logic symbol

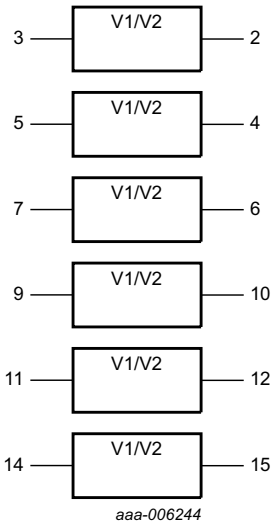


Fig 2. IEC logic symbol

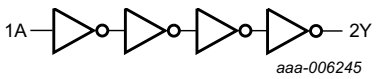


Fig 3. Logic diagram (one level shifter)

5. Pinning information

5.1 Pinning

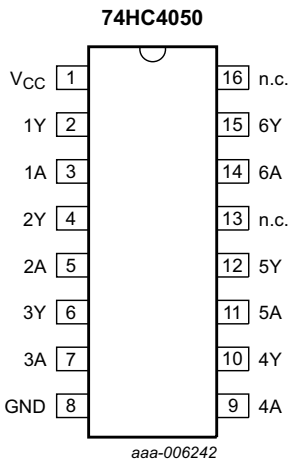


Fig 4. Pin configuration SO16

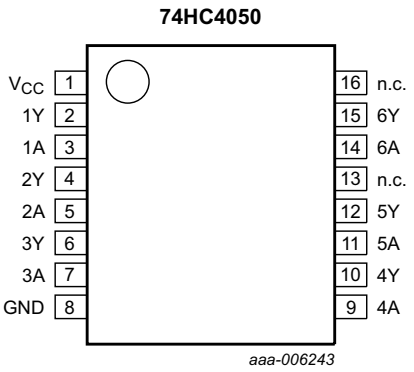


Fig 5. Pin configuration SSOP16 and TSSOP16

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V_{CC}	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output
1A to 6A	3, 5, 7, 9, 11, 14	input
GND	8	ground (0 V)
n.c.	13, 16	not connected

6. Functional description

Table 3. Function table [1]

Input	Output
nA	**nY**
L	L
H	H

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		−0.5	+7	V
V_{IK}	input clamping voltage		−0.5	+16	V
I_{IK}	input clamping current	$V_I < -0.5$ V	−20	-	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $(V_{CC} + 0.5$ V)	-	±25	mA
I_{CC}	supply current		-	+50	mA
I_{GND}	ground current		-	−50	mA
T_{stg}	storage temperature		−65	+150	°C
P_{tot}	total power dissipation	SO16, SSOP16 and TSSOP16 packages [1]	-	500	mW

[1] For SO16 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP16 and TSSOP16 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

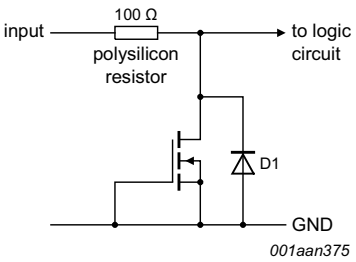


Fig 6. Input protection for the 74HC4050

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	15	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		−40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V; V_I = 2.0 V	-	-	625	ns/V
		V_{CC} = 4.5 V; V_I = 4.5 V	-	1.67	139	ns/V
		V_{CC} = 6.0 V; V_I = 6.0 V	-	-	83	ns/V
		V_{CC} = 6.0 V; V_I = 10.0 V	-	-	81	ns/V
		V_{CC} = 6.0 V; V_I = 15.0 V	-	-	83	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = −40 °C to +85 °C		T_{amb} = −40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.7	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	1.8	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.3	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = −20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = −20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = −20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = −4.0 mA; V_{CC} = 4.5 V	3.98	-	-	3.84	-	3.7	-	V
		I_O = −5.2 mA; V_{CC} = 6.0 V	5.48	-	-	5.34	-	5.2	-	V

Table 6. Static characteristics *...continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	-	0.1	-	0.1	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.26	-	0.33	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
		V_I = 15 V; V_{CC} = 2.0 V to 6.0 V	-	-	±0.5	-	±5.0	-	±5.0	μA
I_{CC}	supply current	V_I = 15 V or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	2.0	-	20	-	40	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	nA to nY; see Figure 7 [1]								
		V_{CC} = 2.0 V	-	25	85	-	105	-	130	ns
		V_{CC} = 4.5 V	-	9	17	-	21	-	26	ns
		V_{CC} = 5 V; C_L = 15 pF	-	7	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	7	14	-	18	-	22	ns
t_t	transition time	Yn; see Figure 7 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns

Table 7. Dynamic characteristics *...continued*

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see Figure 8.

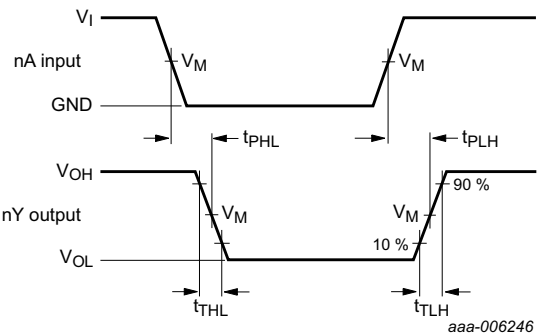
Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	C_L = 50 pF; f = 1 MHz; [3] V_I = GND to V_{CC}	-	14	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



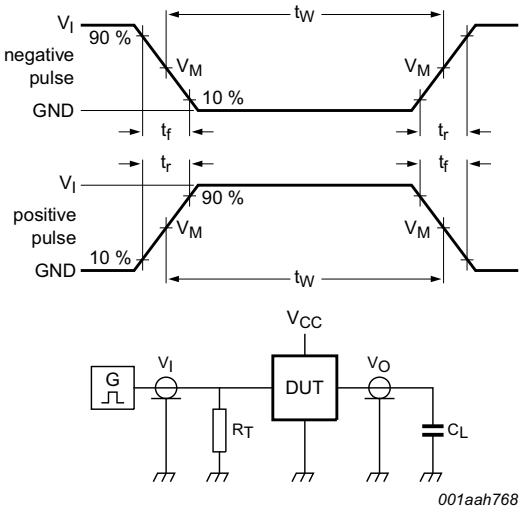
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 7. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Type	Input	Output
	V_M	V_M
74HC4050	0.5V_{CC}	0.5V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

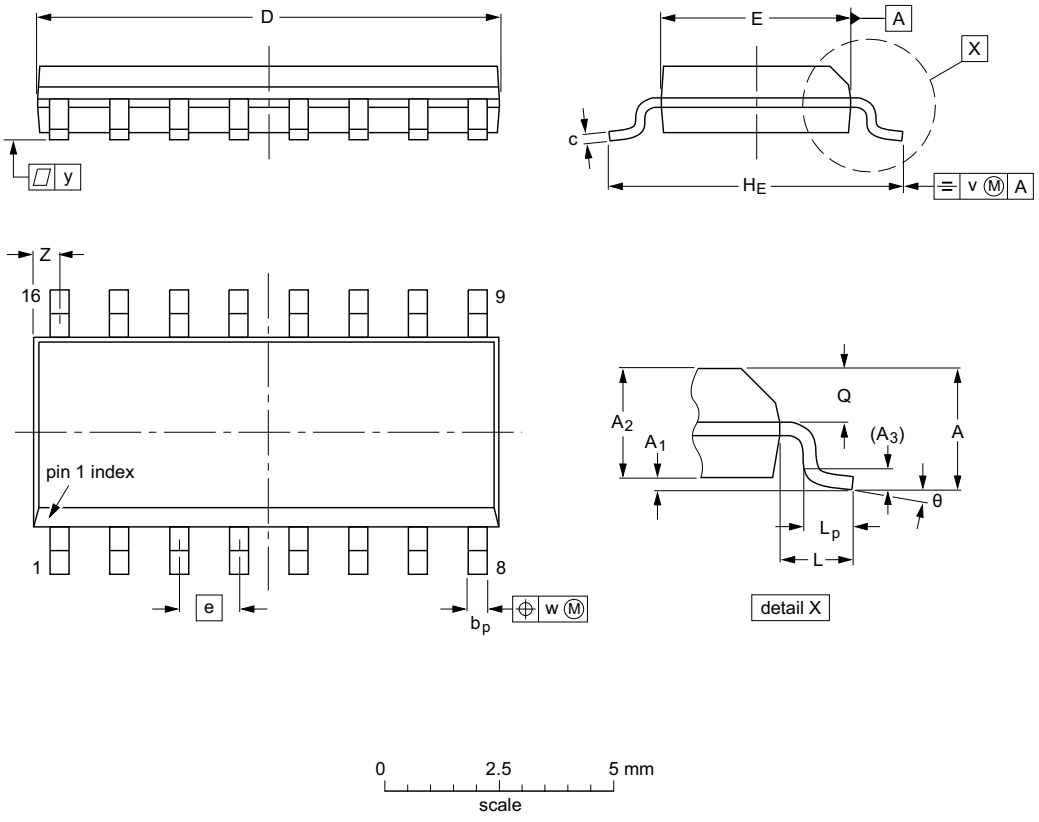
Fig 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC4050	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

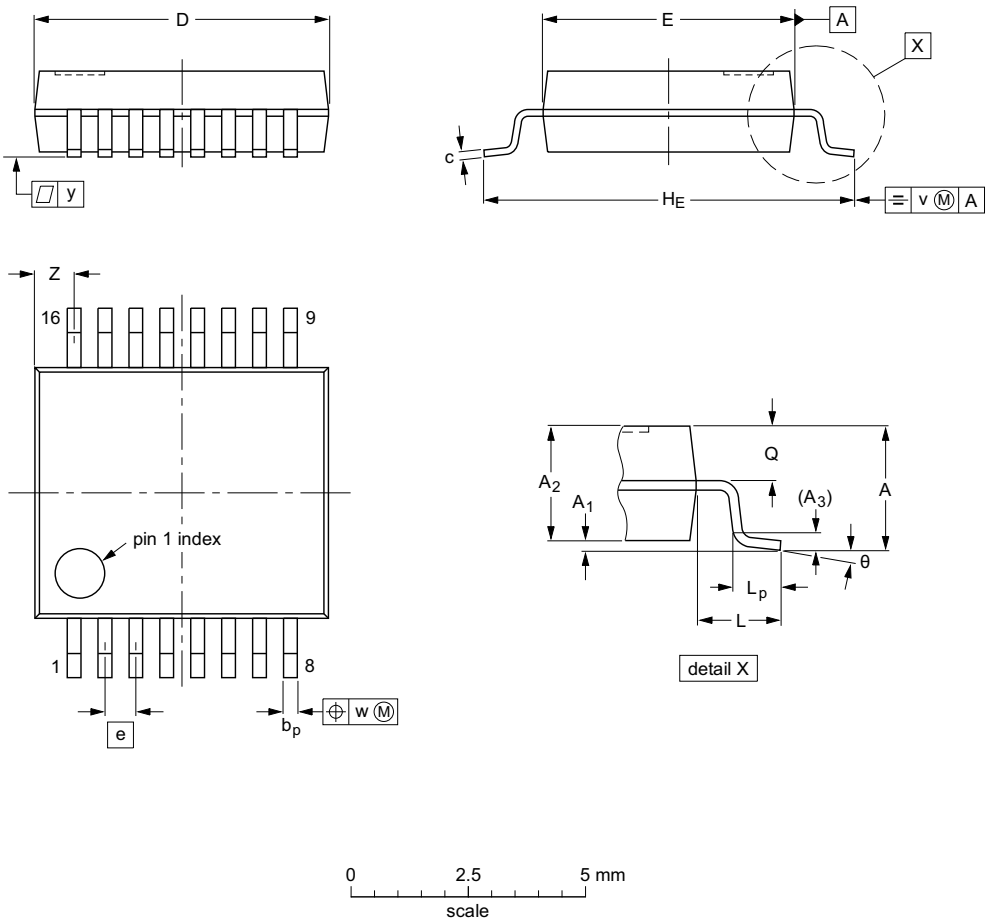
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

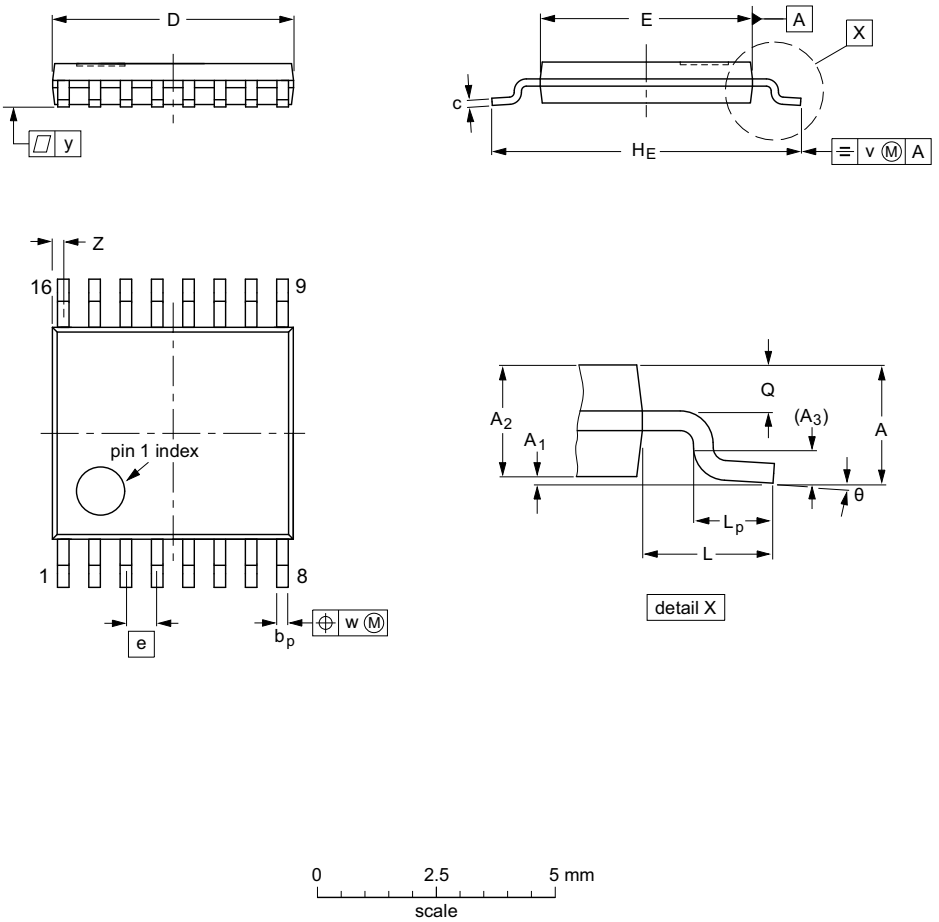
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 11. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4050 v.4	20160205	Product data sheet	-	74HC4050 v.3
Modifications:	• Type number 74HC4050N (SOT38-4) removed.			
74HC4050 v.3	20130131	Product data sheet	-	74HC4050_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74HC4050_CNV v.2	19970826	Product specification	-	-

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 05 February 2016

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