74HC241; 74HCT241

Octal buffer/line driver; 3-state

Rev. 3 — 20 February 2018 Product data sheet

1 General description

The 74HC241; 74HCT241 is an 8-bit buffer/line driver with 3-state outputs. The device can be used as two 4-bit buffers or one 8-bit buffer. The device features two output enables ($1\overline{OE}$ and 2OE), each controlling four of the 3-state outputs. A HIGH on $1\overline{OE}$ or LOW on 2OE causes the associated outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

The 74HCT241 device features reduced input threshold levels to allow interfacing to TTL logic levels.

2 Features and benefits

- Input levels:
  - For 74HC241: CMOS level
  - For 74HCT241: TTL level
- Octal bus interface
- Non-inverting 3-state outputs
- Complies with JEDEC standard no. 7 A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3 Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC241D	-40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT241D				
74HC241DB	-40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HCT241DB				
74HC241PW	-40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT241PW				

4 Functional diagram

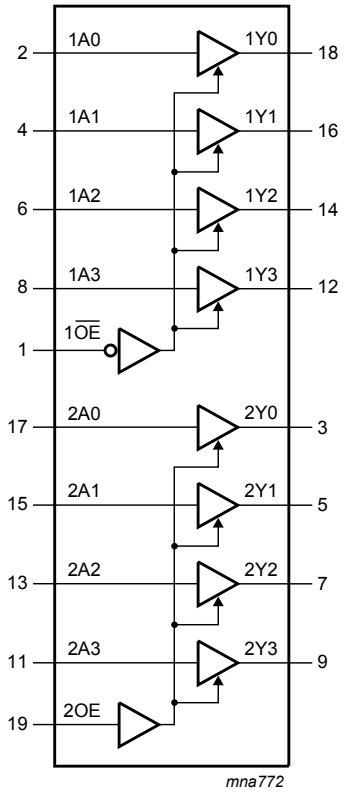


Figure 1. Logic symbol

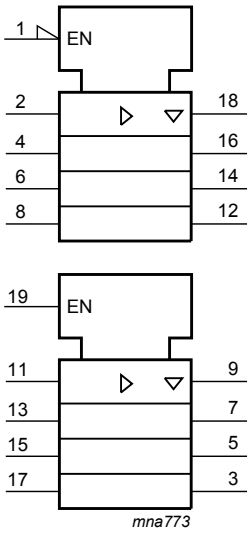


Figure 2. IEC logic symbol

5 Pinning information

5.1 Pinning

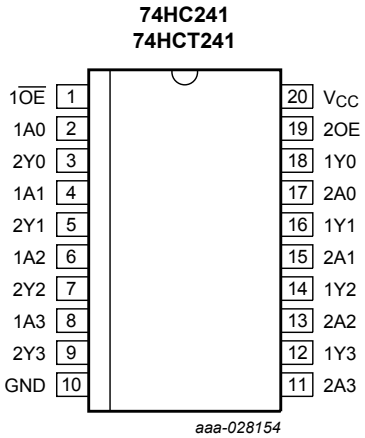


Figure 3. Pin configuration for SO20

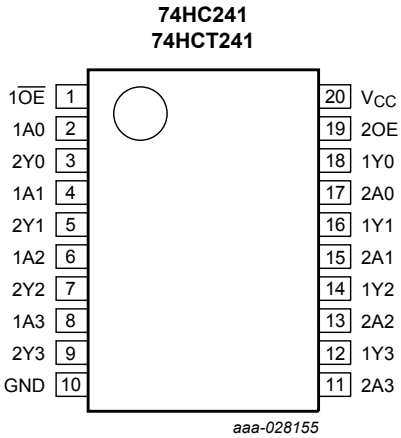


Figure 4. Pin configuration for (T)SSOP20

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$	1	output enable input (active LOW)
1A0, 1A1, 1A2, 1A3	2, 4, 6, 8	data input
2A0, 2A1, 2A2, 2A3	17, 15, 13, 11	data input
GND	10	ground (0 V)
1Y0, 1Y1, 1Y2, 1Y3	18, 16, 14, 12	data output
2Y0, 2Y1, 2Y2, 2Y3	3, 5, 7, 9	data output
2OE	19	output enable input (active HIGH)
V_{CC}	20	supply voltage

6 Functional description

Table 3. Function table [1]

Inputs		Outputs	Inputs		Outputs
$1\overline{OE}$	1An	1Yn	2OE	2An	2Yn
L	L	L	H	L	L
L	H	H	H	H	H
H	X	Z	L	X	Z

[1] H = HIGH voltage level;
L = LOW voltage level;
X = Don't care;
Z = High impedance "OFF" state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	-	±35	mA
I_{CC}	supply current		-	70	mA
I_{GND}	ground current		-70	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	SO20, SSOP20 and TSSOP20 [1]	-	500	mW

[1] For SO20 packages: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC241			74HCT241			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
$\Delta t/\Delta V$	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
T_{amb}	ambient temperature		-40	-	+125	-40	-	+125	°C

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
74HC241										
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = -20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = -20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = -6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = -7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	V_I = V_{IH} or V_{IL}; V_{CC} = 6.0 V; V_O = V_{CC} or GND	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT241										
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V								
		I_O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = -6 mA	3.98	4.32	-	3.84	-	3.7	-	V

Symbol	Parameter	Conditions	T_{amb} (°C)							Unit
			25			−40 to +85		−40 to +125		
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V								
		I_O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{OZ}	OFF-state output current	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 5.5 V; $V_O = V_{CC}$ or GND	-	-	±0.5	-	±5.0	-	±10	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	8.0	-	80	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A								
		nAn; $1\overline{OE}$	-	70	252	-	315	-	343	µA
		2OE	-	150	540	-	675	-	735	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10 Dynamic characteristics

Table 7. Dynamic characteristics

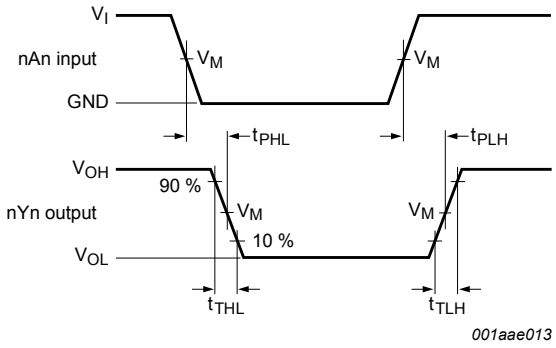
Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 8.

Symbol	Parameter	Conditions	T_{amb} (°C)					Unit
			+25			−40 to +85	−40 to +125	
			Min	Typ	Max	Max	Max	
74HC241								
t_{pd}	propagation delay	nAn to nYn; see Figure 5 [1]						
		V_{CC} = 2.0 V	-	25	100	125	150	ns
		V_{CC} = 4.5 V	-	9	20	25	30	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	ns
		V_{CC} = 6.0 V	-	7	17	21	26	ns
t_{en}	enable time	$1\overline{OE}$ to 1Yn; see Figure 6; 2OE to 2Yn; see Figure 7 [2]						
		V_{CC} = 2.0 V	-	30	150	190	225	ns
		V_{CC} = 4.5 V	-	11	30	38	45	ns
		V_{CC} = 6.0 V	-	9	26	33	38	ns
t_{dis}	disable time	$1\overline{OE}$ to 1Yn; see Figure 6; 2OE to 2Yn; see Figure 7 [3]						
		V_{CC} = 2.0 V	-	39	150	190	225	ns
		V_{CC} = 4.5 V	-	14	30	38	45	ns
		V_{CC} = 6.0 V	-	11	26	33	38	ns

Symbol	Parameter	Conditions	T_{amb} (°C)					Unit
			+25			−40 to +85	−40 to +125	
			Min	Typ	Max	Max	Max	
t_t	transition time	see Figure 5 [4]						
		V_{CC} = 2.0 V	-	14	60	75	90	ns
		V_{CC} = 4.5 V	-	5	12	15	18	ns
		V_{CC} = 6.0 V	-	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} [5]	-	30	-	-	-	pF
74HCT241								
t_{pd}	propagation delay	nAn to nYn; see Figure 5 [1]						
		V_{CC} = 4.5 V	-	13	22	28	33	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	11	-	-	-	ns
t_{en}	enable time	$1\overline{OE}$ to 1Yn; see Figure 6; 2OE to 2Yn; see Figure 7; V_{CC} = 4.5 V [2]	-	15	30	38	45	ns
t_{dis}	disable time	$1\overline{OE}$ to 1Yn; see Figure 6; 2OE to 2Yn; see Figure 7; V_{CC} = 4.5 V [3]	-	18	30	38	45	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 5 [4]	-	5	12	15	18	ns
C_{PD}	power dissipation capacitance	per buffer; V_I = GND to V_{CC} - 1.5 V [5]	-	30	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{en} is the same as t_{PZH} and t_{PZL}.
[3] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
[4] t_t is the same as t_{THL} and t_{TLH}.
[5] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} V_{CC}^2 f_i N + \sum(C_L V_{CC}^2 f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum(C_L V_{CC}^2 f_o)$ = sum of outputs.

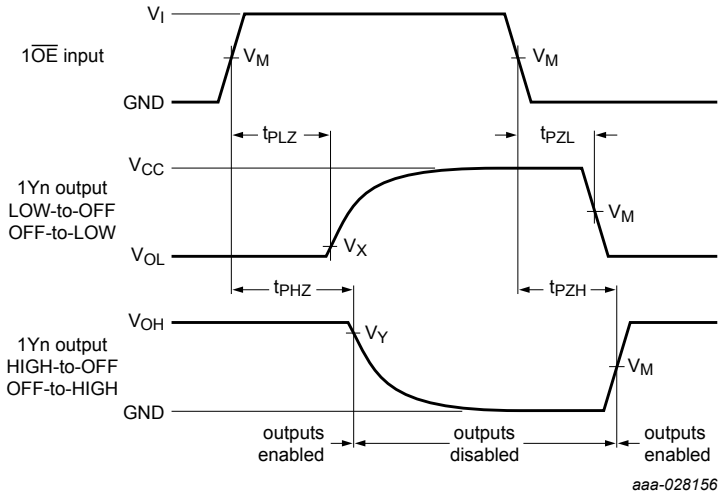
10.1 Waveforms and test circuit



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

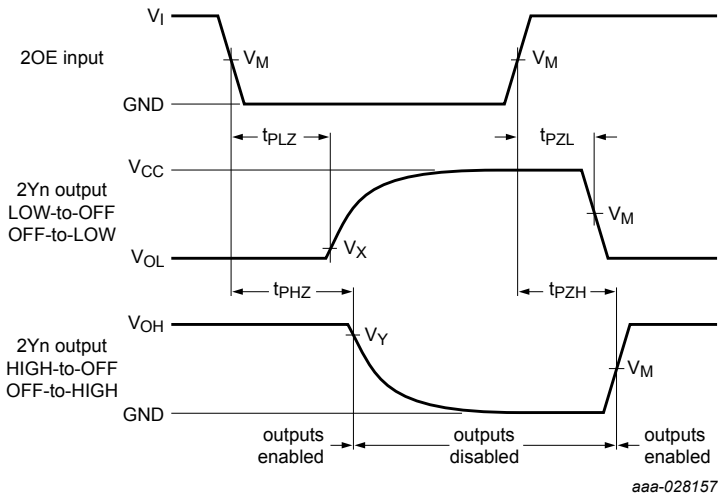
Figure 5. Input (nAn) to output (nYn) propagation delays and output transition times



See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. 3-state output ($1\overline{OE}$ to 1Yn) enable and disable times



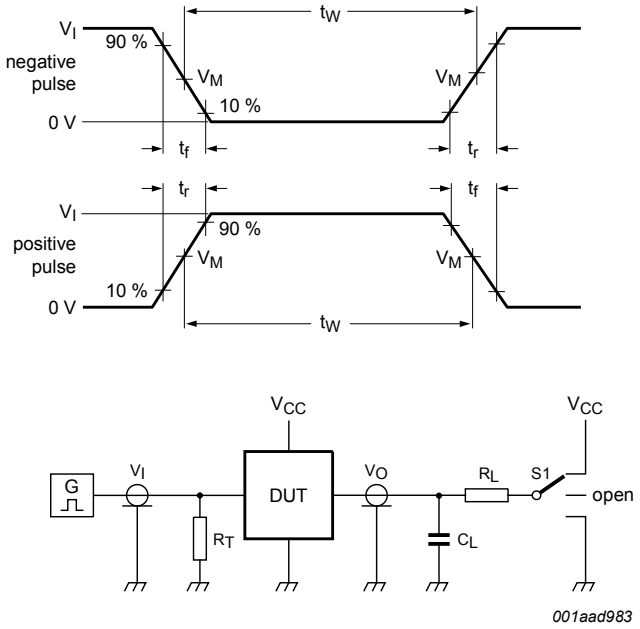
See Table 8 for measurement points.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 7. 3-state output (2OE to 2Yn) enable and disable times

Table 8. Measurement points

Type	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
74HC241	GND to V_{CC}	0.5 x V_{CC}	0.5 x V_{CC}	0.1 x V_{CC}	0.9 x V_{CC}
74HCT241	GND to 3 V	1.3 V	1.3 V	0.1 x V_{CC}	0.9 x V_{CC}



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

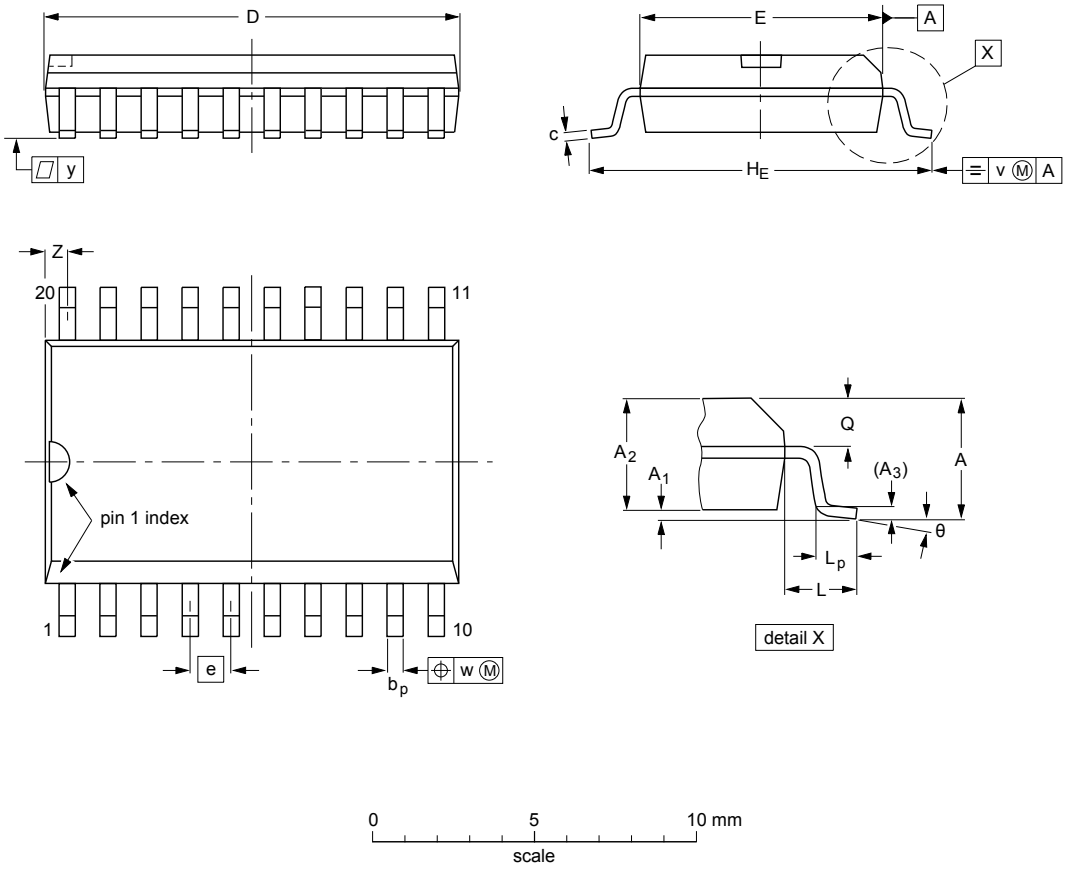
Figure 8. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC241	GND to V_{CC}	6 ns	50 pF	1 kΩ	open	GND	V_{CC}
74HCT241	GND to 3 V	6 ns	50 pF	1 kΩ	open	GND	V_{CC}

11 Package outline

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

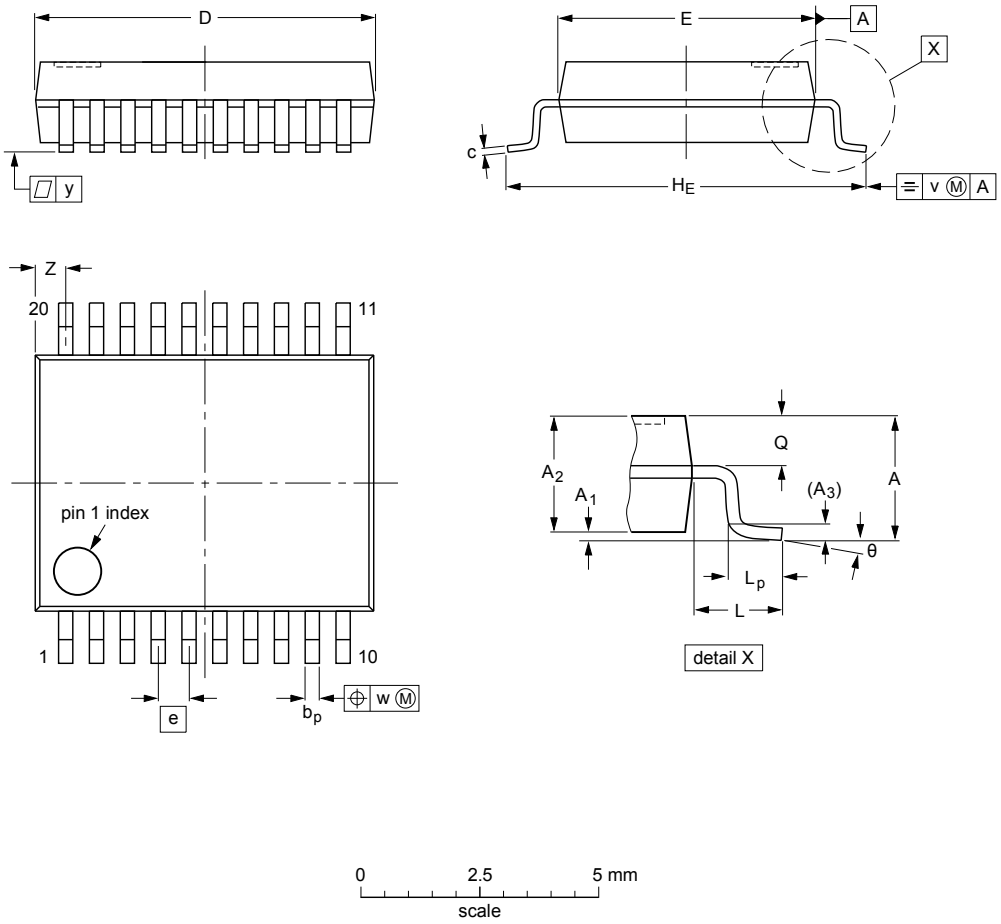
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Figure 9. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

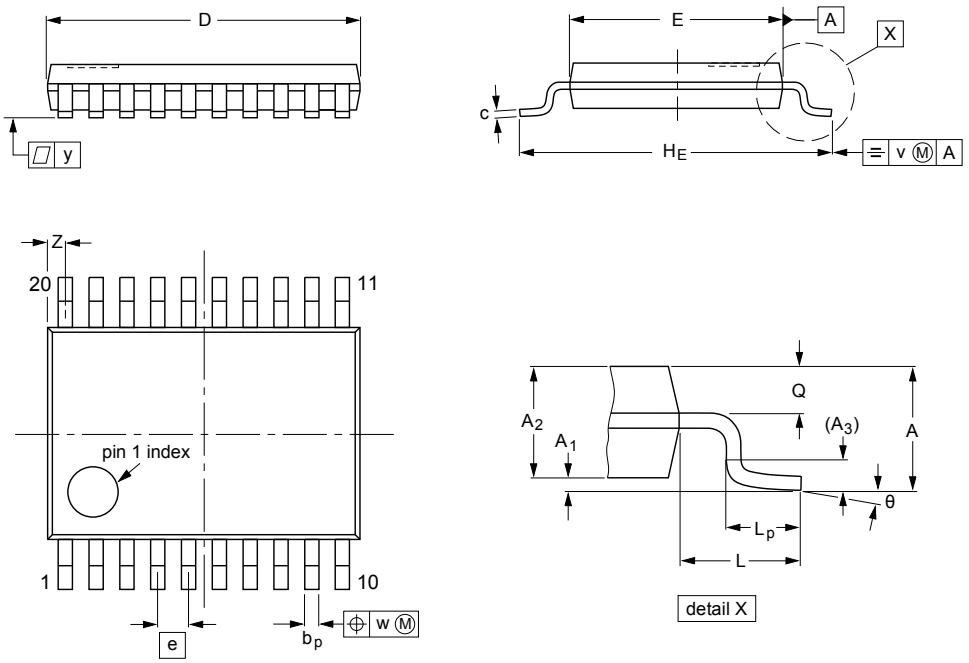
Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Figure 10. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Figure 11. Package outline SOT360-1 (TSSOP20)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT241 v.3	20180220	Product data sheet	-	74HC_HCT241 v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT241 v.2	19930801	Product data sheet	-	74HC_HCT241 v.1

14 Legal information

14.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nexperia.com.

14.2 Definitions

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