74HC4316; 74HCT4316

Quad single-pole single-throw analog switch

Rev. 5 — 10 March 2021 | Product data sheet

1. General description

The 74HC4316; 74HCT4316 is a quad single pole, single throw analog switch (SPST). Each switch features two input/output terminals (nY and nZ) and an active HIGH enable input (nS). When nS is LOW, the analog switch is turned off. When $\overline{E}$ is HIGH all four analog switches are turned off. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Input levels $\overline{E}$ and nS inputs:
  - For 74HC4316: CMOS level
  - For 74HCT4316: TTL level
- Low ON resistance:
  - 160 Ω (typical) at V_{CC} - V_{EE} = 4.5 V
  - 120 Ω (typical) at V_{CC} - V_{EE} = 6.0 V
  - 80 Ω (typical) at V_{CC} - V_{EE} = 9.0 V
- Logic level translation:
  - To enable 5 V logic to communicate with ±5 V analog signals
- Typical break-before-make built in
- Specified in compliance with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Applications

- Signal gating
- Modulation
- Demodulation
- Chopper

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4316D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT4316D				
74HC4316DB	-40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC4316PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT4316PW				

5. Functional diagram

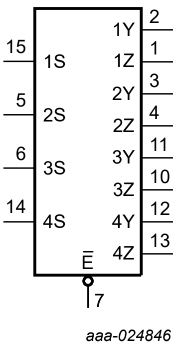


Fig. 1. Logic symbol

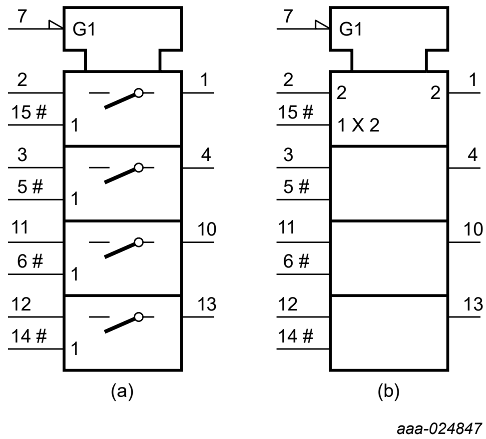


Fig. 2. IEC logic symbol

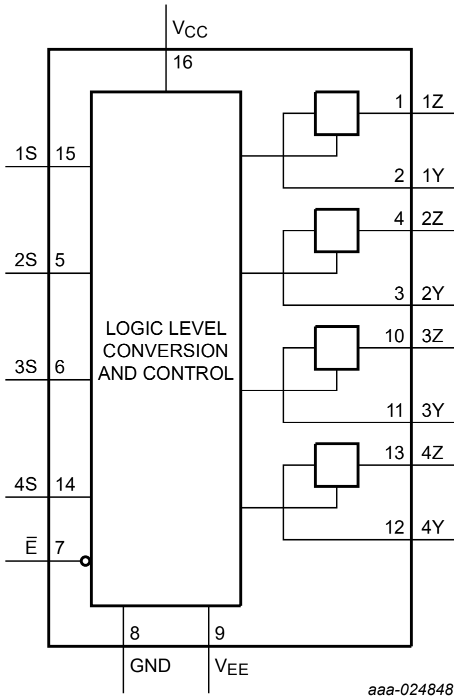


Fig. 3. Functional diagram

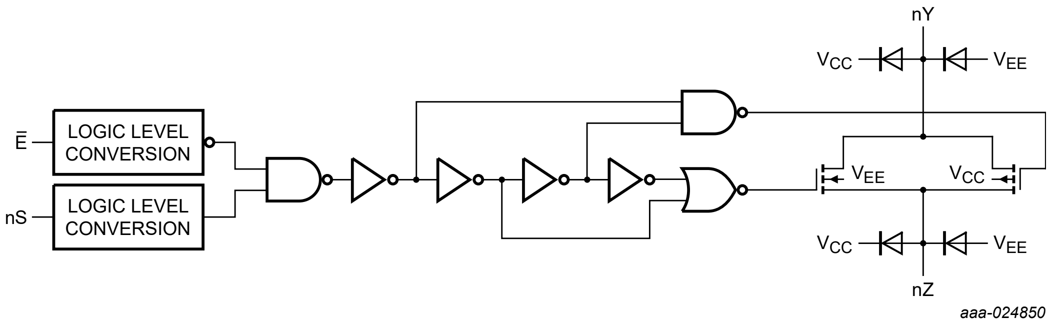


Fig. 4. Schematic diagram (one switch)

6. Pinning information

6.1. Pinning

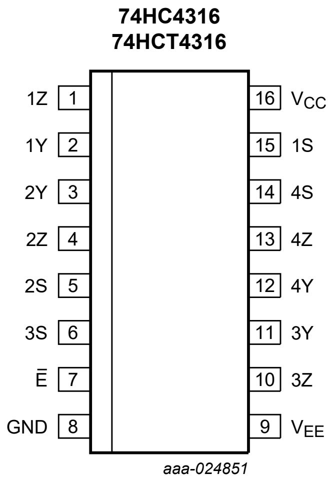


Fig. 5. Pin configuration SOT109-1 (SO16)

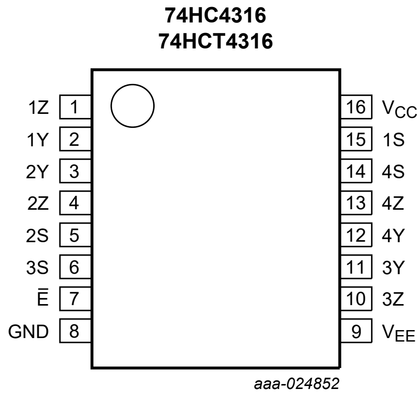


Fig. 6. Pin configuration SOT338-1 (SSOP16) and SOT403-1 (TSSOP16)

6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Z, 2Z, 3Z, 4Z	1, 4, 10, 13	independent input or output
1Y, 2Y, 3Y, 4Y	2, 3, 11, 12	independent input or output
$\overline{E}$	7	enable input (active LOW)
GND	8	ground (0 V)
V_{EE}	9	negative supply voltage
1S, 2S, 3S, 4S	15, 5, 6, 14	select input (active HIGH)
V_{CC}	14	positive supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input		Switch
$\overline{E}$	nS	
L	L	OFF
L	H	ON
H	X	OFF

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+11.0	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V		-	±20	mA
I_{SK}	switch clamping current	V_{SW} < -0.5 V or V_{SW} > V_{CC} + 0.5 V		-	±20	mA
I_{SW}	switch current	V_{SW} = -0.5 V to V_{CC} + 0.5 V	[1]	-	±25	mA
I_{EE}	supply current			-	20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-50	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW
P	power dissipation	per switch		-	100	mW

[1] To avoid drawing V_{CC} current out of terminal nZ, when switch current flows in terminals nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no V_{CC} current will flow out of terminals nY. In this case there is no limit for the voltage drop across the switch, but the voltages at nY and nZ may not exceed V_{CC} or V_{EE}.

[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT338-1 (SSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	74HC4316			74HCT4316			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage	see Fig. 7 and Fig. 8							
		V_{CC} - GND	2.0	5.0	10.0	4.5	5.0	5.5	V
		V_{EE} - GND	2.0	5.0	10.0	2.0	5.0	10.0	V
V_I	input voltage		GND	-	V_{CC}	GND	-	V_{CC}	V
V_{SW}	switch voltage		V_{EE}	-	V_{CC}	V_{EE}	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V
		V_{CC} = 10.0 V	-	-	35	-	-	-	ns/V

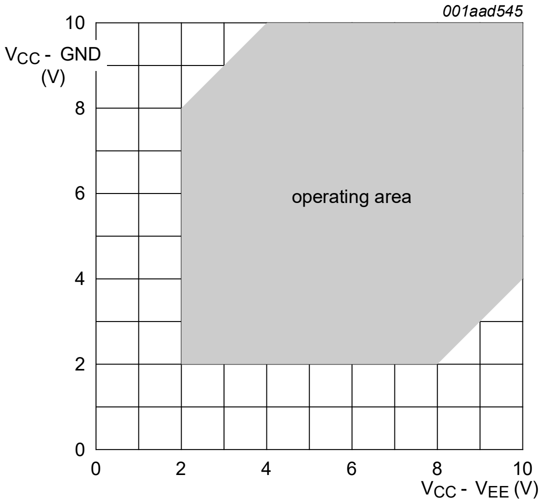


Fig. 7. Guaranteed operating area as a function of the supply voltages for 74HC4316

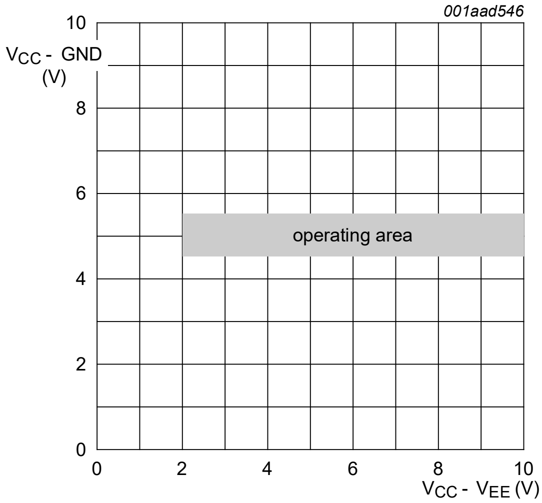


Fig. 8. Guaranteed operating area as a function of the supply voltages for 74HCT4316

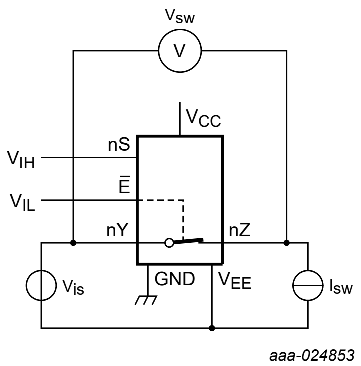
10. Static characteristics

Table 6. R_{ON} resistance per switch for types 74HC4316 and 74HCT4316

$V_I = V_{IH}$ or V_{IL}; for test circuit see Fig. 9.
V_{is} is the input voltage at a nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nY or nZ terminal, whichever is assigned as an output.
For 74HC4316: V_{CC} - GND or V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.
For 74HCT4316: V_{CC} - GND = 4.5 V and 5.5 V; V_{CC} - V_{EE} = 2.0 V, 4.5 V, 6.0 V and 9.0 V.

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Typ	Max	Min	Max	Min	Max	
$R_{ON(peak)}$	ON resistance (peak)	$V_{is} = V_{CC}$ to V_{EE} [1]							
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	-	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	160	320	-	400	-	480	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	120	240	-	300	-	360	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	85	170	-	215	-	255	Ω
$R_{ON(rail)}$	ON resistance (rail)	$V_{is} = V_{EE}$ [1]							
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	160	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	80	160	-	200	-	240	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	70	140	-	175	-	210	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	60	120	-	150	-	180	Ω
		$V_{is} = V_{CC}$ [1]							
		V_{CC} = 2.0 V; V_{EE} = 0 V; I_{SW} = 100 μA	170	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V; I_{SW} = 1000 μA	90	180	-	225	-	270	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V; I_{SW} = 1000 μA	80	160	-	200	-	240	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V; I_{SW} = 1000 μA	65	135	-	170	-	205	Ω
ΔR_{ON}	ON resistance mismatch between channels	$V_{is} = V_{CC}$ to V_{EE} [1]							
		V_{CC} = 2.0 V; V_{EE} = 0 V	-	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = 0 V	16	-	-	-	-	-	Ω
		V_{CC} = 6.0 V; V_{EE} = 0 V	9	-	-	-	-	-	Ω
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	6	-	-	-	-	-	Ω

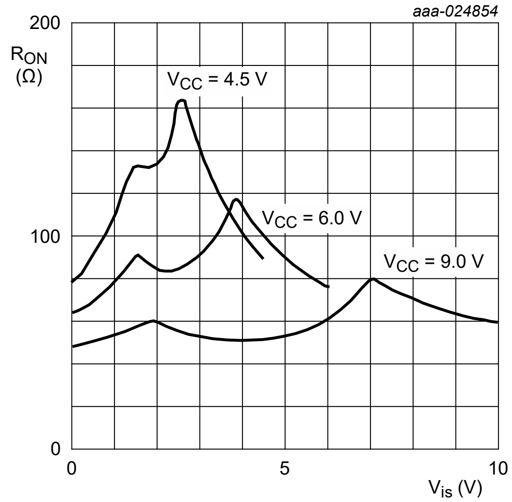
[1] When supply voltages (V_{CC} - V_{EE}) near 2.0 V the analog switch ON resistance becomes extremely non-linear. When using a supply of 2 V, it is recommended to use these devices only for transmitting digital signals.



V_{is} = 0 V to (V_{CC} - V_{EE})

$$R_{ON} = \frac{V_{SW}}{I_{SW}}$$

Fig. 9. Test circuit for measuring R_{ON}



V_{is} = 0 V to (V_{CC} - V_{EE})

Fig. 10. Typical R_{ON} as a function of input voltage V_{is}

Table 7. Static characteristics 74HC4316

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nY or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
		V_{CC} = 9.0 V	6.3	4.3	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
		V_{CC} = 9.0 V	-	4.3	2.7	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	±0.1	μA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	±0.2	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} - V_{EE}; see Fig. 11	-	-	±0.1	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\lvert V_{SW}\rvert$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	8.0	μA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	16.0	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance		-	5	-	pF

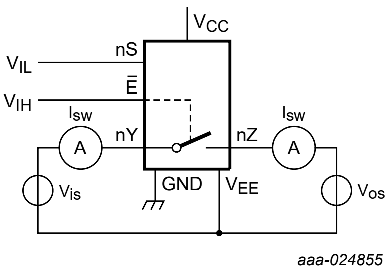
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
		V_{CC} = 9.0 V	-	-	2.7	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	±1.0	µA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	±2.0	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11	-	-	±1.0	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	80.0	µA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	160.0	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
		V_{CC} = 9.0 V	6.3	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
		V_{CC} = 9.0 V	-	-	2.7	V
I_I	input leakage current	V_I = V_{CC} or GND				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	±1.0	µA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	±2.0	µA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11	-	-	±1.0	µA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10.0 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 6.0 V; V_{EE} = 0 V	-	-	160	µA
		V_{CC} = 10.0 V; V_{EE} = 0 V	-	-	320	µA

Table 8. Static characteristics 74HCT4316

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).
V_{is} is the input voltage at a nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nY or nZ terminal, whichever is assigned as an output.

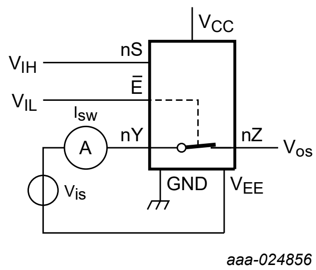
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±0.1	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11	-	-	±0.1	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±0.1	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	8.0	μA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	16.0	μA
ΔI_{CC}	additional supply current	nS and $\overline{E}$; per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	50	180	μA
C_I	input capacitance		-	3.5	-	pF
C_{sw}	switch capacitance		-	5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 11	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; V_I = V_{IH} or V_{IL}; $\|V_{SW}\|$ = V_{CC} - V_{EE}; see Fig. 12	-	-	±1.0	μA
I_{CC}	supply current	V_I = V_{CC} or GND; V_{is} = V_{EE} or V_{CC}; V_{os} = V_{CC} or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	80	μA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	160	μA
ΔI_{CC}	additional supply current	nS and $\overline{E}$; per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	-	225	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	±1.0	μA
$I_{S(OFF)}$	OFF-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - V_{EE}$; see Fig. 11	-	-	±1.0	μA
$I_{S(ON)}$	ON-state leakage current	V_{CC} = 10 V; V_{EE} = 0 V; $V_I = V_{IH}$ or V_{IL}; $\|V_{SW}\| = V_{CC} - V_{EE}$; see Fig. 12	-	-	±1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $V_{is} = V_{EE}$ or V_{CC}; $V_{os} = V_{CC}$ or V_{EE}				
		V_{CC} = 5.5 V; V_{EE} = 0 V	-	-	160	μA
		V_{CC} = 5.0 V; V_{EE} = -5.0 V	-	-	320	μA
ΔI_{CC}	additional supply current	nS and $\overline{E}$; per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V; V_{EE} = 0 V	-	-	245	μA



$V_{is} = V_{CC}$ and $V_{os} = V_{EE}$
$V_{is} = V_{EE}$ and $V_{os} = V_{CC}$

Fig. 11. Test circuit for measuring OFF-state leakage current



$V_{is} = V_{CC}$ and V_{os} = open
$V_{is} = V_{EE}$ and V_{os} = open

Fig. 12. Test circuit for measuring ON-state leakage current

11. Dynamic characteristics

Table 9. Dynamic characteristics

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF unless specified otherwise; for test circuit see Fig. 15.
V_{is} is the input voltage at a nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nY or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Typ	Max	Min	Max	Min	Max	
74HC4316										
t_{pd}	propagation delay	nY to nZ or nZ to nY; R_L = ∞ Ω; see Fig. 13	[1]							
		V_{CC} = 2.0 V; V_{EE} = 0 V		17	60	-	75	-	90	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		6	12	-	15	-	18	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		5	10	-	13	-	15	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		4	8	-	10	-	12	ns
t_{off}	turn-off time	$\overline{E}$ to nY or nZ; see Fig. 14	[2]							
		V_{CC} = 2.0 V; V_{EE} = 0 V		63	220	-	275	-	330	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		23	44	-	55	-	66	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V;C_L = 15 pF		20	-	-	-	-	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		18	37	-	47	-	56	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		21	39	-	49	-	59	ns
		nS to nY or nZ; see Fig. 14	[2]							
		V_{CC} = 2.0 V; V_{EE} = 0 V		55	175	-	220	-	265	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		20	35	-	44	-	53	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		16	-	-	-	-	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		16	30	-	37	-	45	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		18	36	-	45	-	54	ns
t_{on}	turn-on time	$\overline{E}$ to nY or nZ; see Fig. 14	[3]							
		V_{CC} = 2.0 V; V_{EE} = 0 V		61	205	-	255	-	310	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		22	41	-	51	-	62	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		19	-	-	-	-	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		18	35	-	43	-	53	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		19	37	-	47	-	56	ns
		nS to nY or nZ; see Fig. 14	[3]							
		V_{CC} = 2.0 V; V_{EE} = 0 V		52	175	-	220	-	265	ns
		V_{CC} = 4.5 V; V_{EE} = 0 V		19	35	-	44	-	53	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		16	-	-	-	-	-	ns
		V_{CC} = 6.0 V; V_{EE} = 0 V		15	30	-	37	-	45	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		17	34	-	43	-	51	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to V_{CC}	[4]	13	-	-	-	-	-	pF

Symbol	Parameter	Conditions		25 °C		-40 °C to +85 °C		-40 °C to +125 °C		Unit
				Typ	Max	Min	Max	Min	Max	
74HCT4316										
t_{pd}	propagation delay	nY to nZ or nZ to nY; $R_L = \infty\ \Omega$; see Fig. 13	[1]							
		V_{CC} = 4.5 V; V_{EE} = 0 V		6	12	-	15	-	18	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		4	8	-	10	-	12	ns
t_{PZH}	OFF-state to HIGH propagation delay	$\overline{E}$ to nY or nZ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V		22	44	-	55	-	66	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		19	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		21	42	-	53	-	63	ns
		nS to nY or nZ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V		20	40	-	53	-	60	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		17	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		17	34	-	43	-	51	ns
t_{PZL}	OFF-state to LOW propagation delay	$\overline{E}$ to nY or nZ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V		28	56	-	70	-	84	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		24	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		21	42	-	53	-	63	ns
		nS to nY or nZ; see Fig. 14								
		V_{CC} = 4.5 V; V_{EE} = 0 V		25	50	-	63	-	75	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		21	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		17	34	-	43	-	51	ns
t_{off}	turn-off time	$\overline{E}$ to nY or nZ; see Fig. 14	[2]							
		V_{CC} = 4.5 V; V_{EE} = 0 V		25	50	-	63	-	75	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		21	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		23	46	-	58	-	69	ns
		nS to nY or nZ; see Fig. 14	[2]							
		V_{CC} = 4.5 V; V_{EE} = 0 V		22	44	-	55	-	66	ns
		V_{CC} = 5.0 V; V_{EE} = 0 V; C_L = 15 pF		19	-	-	-	-	-	ns
		V_{CC} = 4.5 V; V_{EE} = -4.5 V		20	40	-	50	-	60	ns
C_{PD}	power dissipation capacitance	per switch; V_I = GND to (V_{CC} - 1.5 V)	[4]	14	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] t_{off} is the same as t_{PHZ} and t_{PLZ}.
[3] t_{on} is the same as t_{PZH} and t_{PZL}.
[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
$P_D = C_{PD} \times V_{CC}{}^2 \times f_i + \sum((C_L + C_{sw}) \times V_{CC}{}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\sum((C_L + C_{sw}) \times V_{CC}{}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
C_{sw} = switch capacitance in pF;
V_{CC} = supply voltage in V.

11.1. Waveforms and test circuit

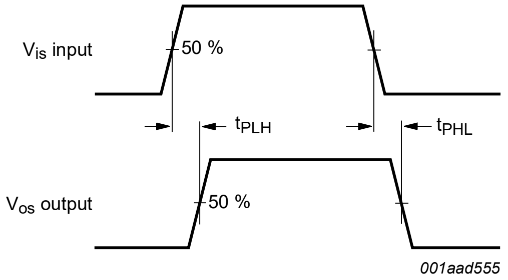
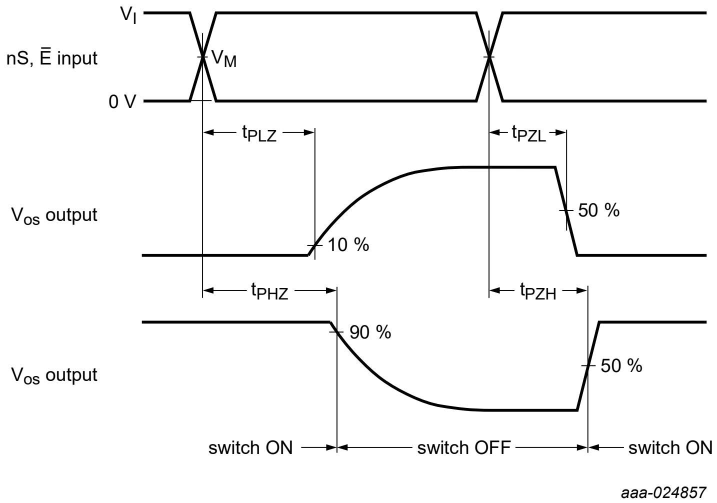


Fig. 13. Input (V_{is}) to output (V_{os}) propagation delays

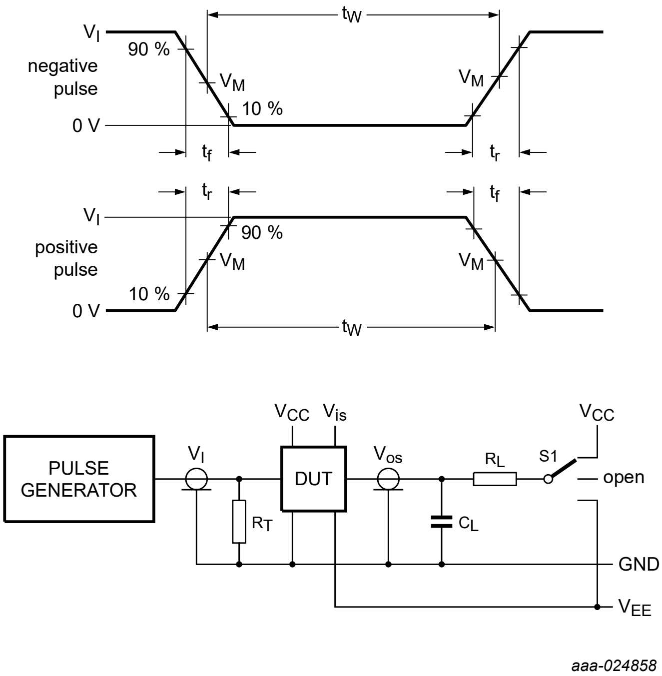


Measurement points are shown in Table 10.

Fig. 14. Turn-on and turn-off times

Table 10. Measurement points

Type	V_I	V_M
74HC4316	V_{CC}	$0.5V_{CC}$
74HCT4316	3.0 V	1.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

S1 = Test selection switch.

Fig. 15. Test circuit for measuring switching times

Table 11. Test data

Test	Input					Output		S1 position
	$\overline{E}$	nS	Switch nY (nZ)	t_r, t_f		Switch nZ (nY)		
	V_I		V_{is}	at f_{max}	other [1]	C_L	R_L	
t_{PHL}, t_{PLH}	[2]		GND to V_{CC}	< 2 ns	6 ns	50 pF	-	open
t_{PHZ}, t_{PZH}	[2]		V_{CC}	< 2 ns	6 ns	50 pF, 15 pF	1 kΩ	V_{EE}
t_{PLZ}, t_{PZL}	[2]		V_{EE}	< 2 ns	6 ns	50 pF, 15 pF	1 kΩ	V_{CC}

[1] $t_r = t_f = 6$ ns; when measuring f_{max}, there is no constraint to t_r and t_f with 50 % duty factor.

[2] V_I values:

For 74HC4316: $V_I = V_{CC}$

For 74HCT4316: $V_I = 3$ V

11.2. Additional dynamic characteristics

Table 12. Additional dynamic characteristics

Recommended conditions and typical values; GND = 0 V; T_{amb} = 25 °C; C_L = 50 pF.
V_{is} is the input voltage at a nY or nZ terminal, whichever is assigned as an input.
V_{os} is the output voltage at a nY or nZ terminal, whichever is assigned as an output.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
THD	total harmonic distortion	f_i = 1 kHz; R_L = 10 kΩ; see Fig. 16				
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	0.80	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	0.40	-	%
		f_i = 10 kHz; R_L = 10 kΩ; see Fig. 16				
		V_{is} = 4.0 V (p-p); V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	2.40	-	%
		V_{is} = 8.0 V (p-p); V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	1.20	-	%
$f_{(-3dB)}$	-3 dB frequency response	R_L = 50 Ω; C_L = 10 pF; see Fig. 17 [1]				
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	150	-	MHz
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	160	-	MHz
α_{iso}	isolation (OFF-state)	R_L = 600 Ω; f_i = 1 MHz; see Fig. 18 [2]				
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	-50	-	dB
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-50	-	dB
V_{ct}	crosstalk voltage	between digital input and switch (peak to peak value); R_L = 600 Ω; f_i = 1 MHz; $\overline{E}$ or nS square wave between V_{CC} and GND; t_r = t_f = 6 ns; see Fig. 19				
		V_{CC} = 4.5 V; V_{EE} = 0 V	-	110	-	mV
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	220	-	mV
Xtalk	crosstalk	between switches; R_L = 600 Ω; f_i = 1 MHz; see Fig. 20 [2]				
		V_{CC} = 2.25 V; V_{EE} = -2.25 V	-	-60	-	dB
		V_{CC} = 4.5 V; V_{EE} = -4.5 V	-	-60	-	dB

[1] Adjust input voltage V_{is} to 0 dBm level at V_{os} for 1 MHz (0 dBm = 1 mW into 50 Ω).
[2] Adjust input voltage V_{is} to 0 dBm level (0 dBm = 1 mW into 600 Ω).

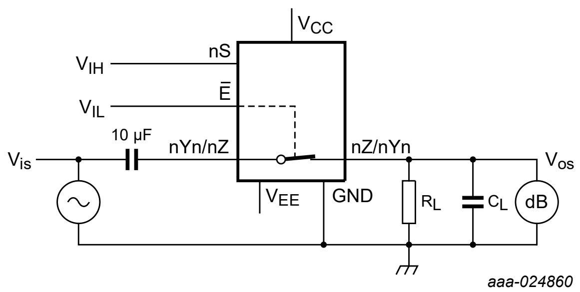
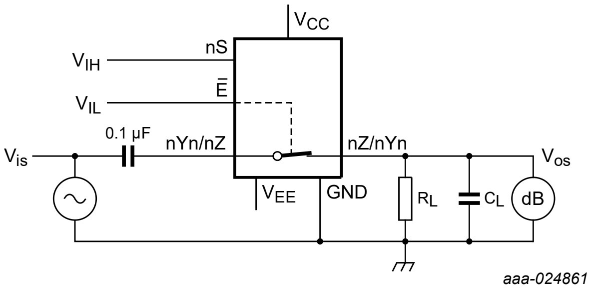
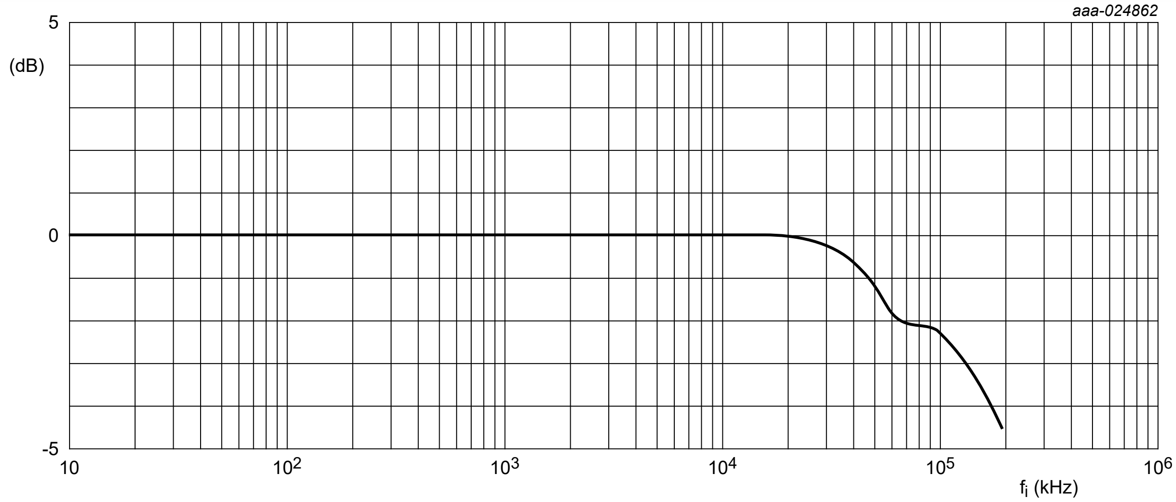


Fig. 16. Test circuit for measuring total harmonic distortion



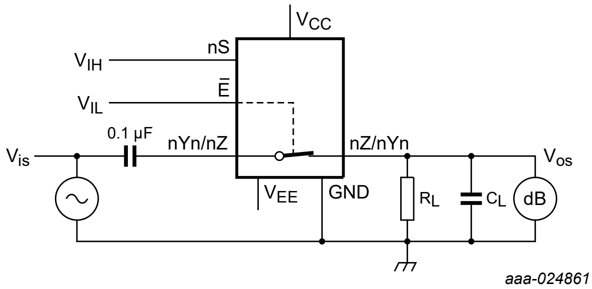
V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 50 Ω; R_S = 1 kΩ.

a. Test circuit



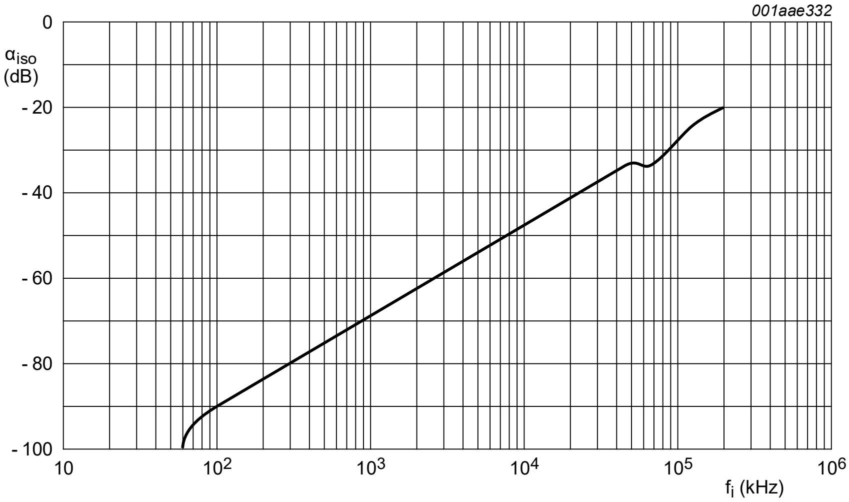
b. Typical -3 dB frequency response

Fig. 17. -3 dB frequency response



V_{CC} = 4.5 V; GND = 0 V; V_{EE} = -4.5 V; R_L = 600 Ω; R_S = 1 kΩ.

a. Test circuit



b. Isolation (OFF-state) as a function of frequency

Fig. 18. Isolation (OFF-state) as a function of frequency

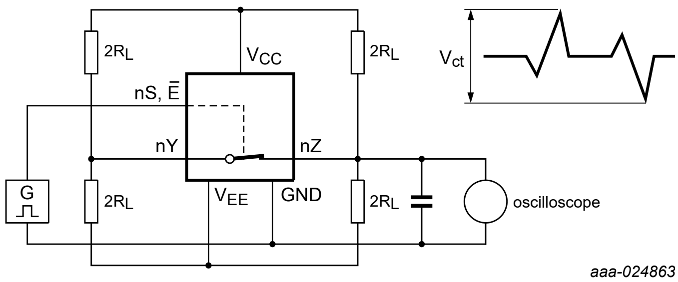


Fig. 19. Test circuit for measuring crosstalk voltage (between the digital input and the switch)

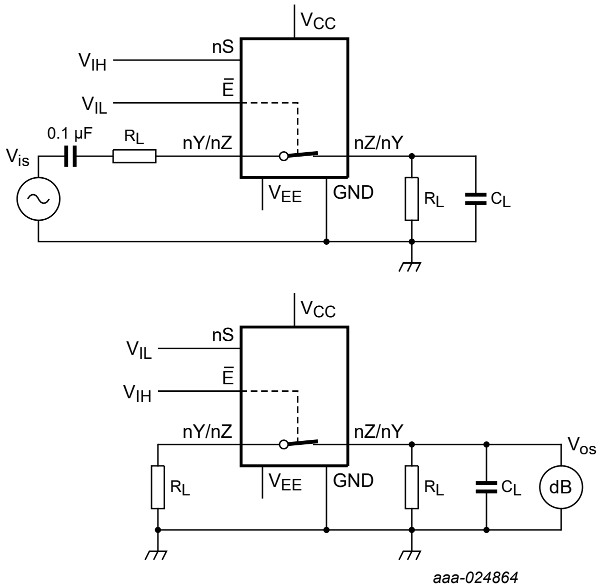
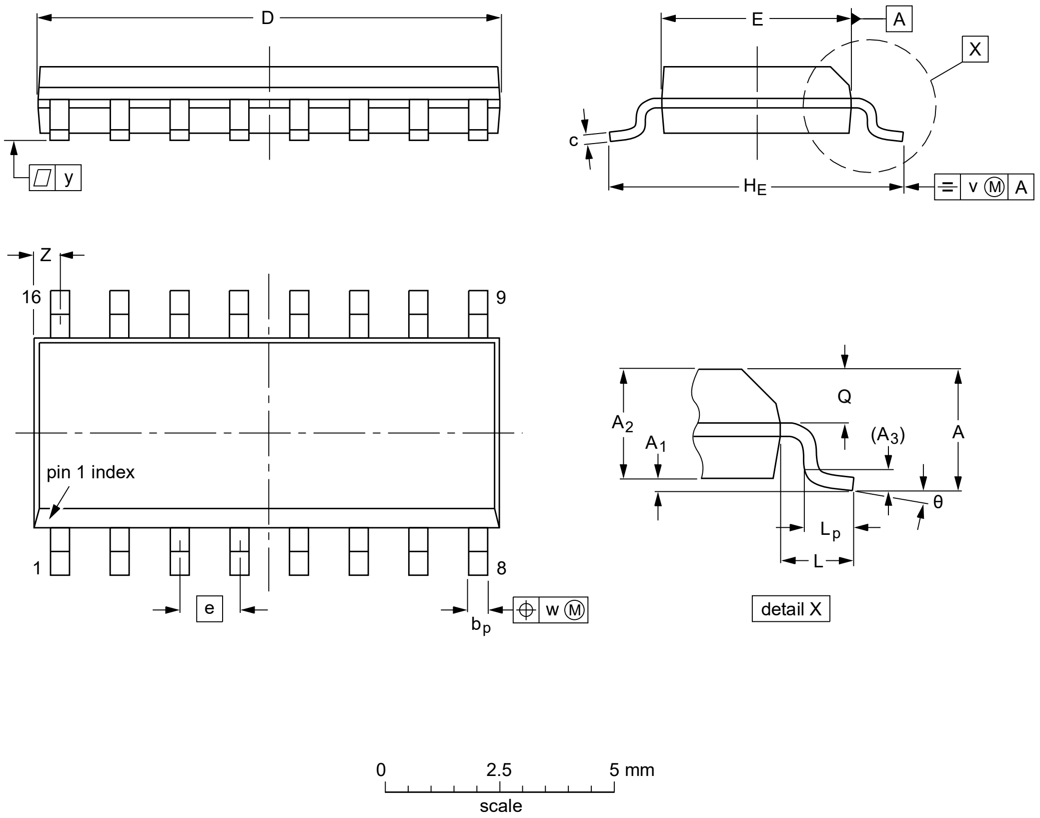


Fig. 20. Test circuit for measuring crosstalk (between the switches)

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D[(1)]	E[(1)]	e	H_E	L	L_p	Q	v	w	y	Z[(1)]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

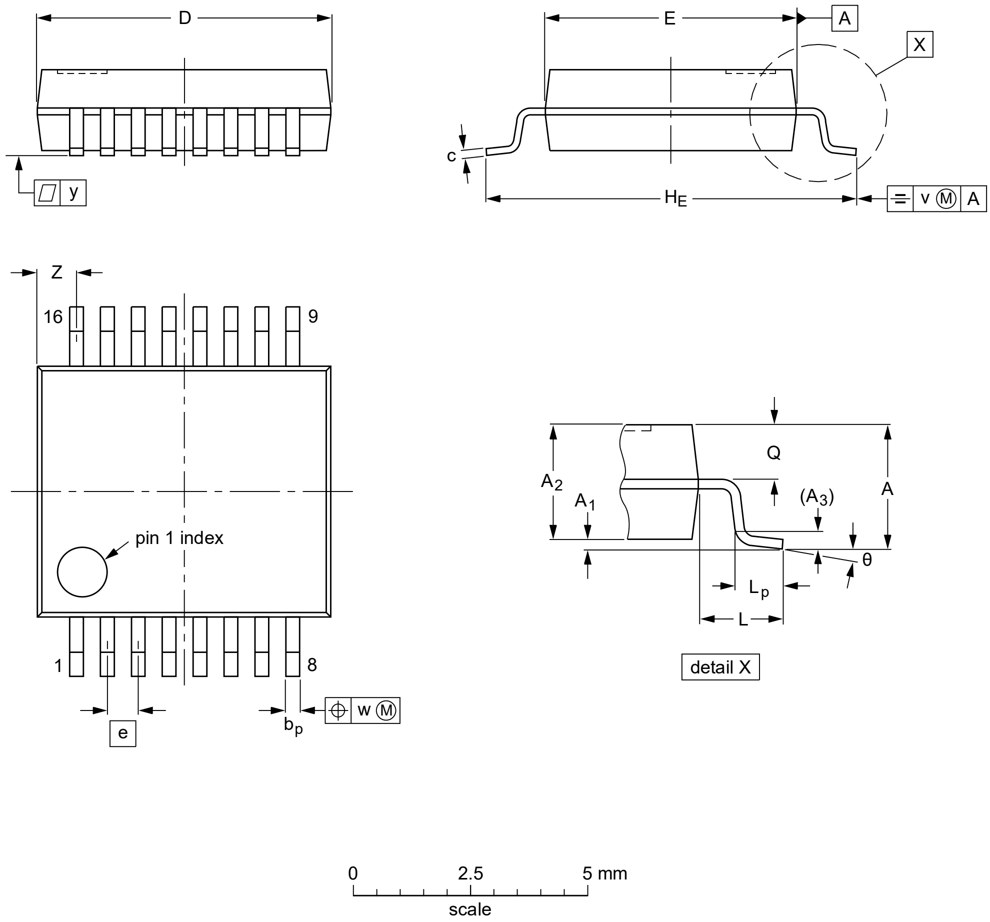
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig. 21. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

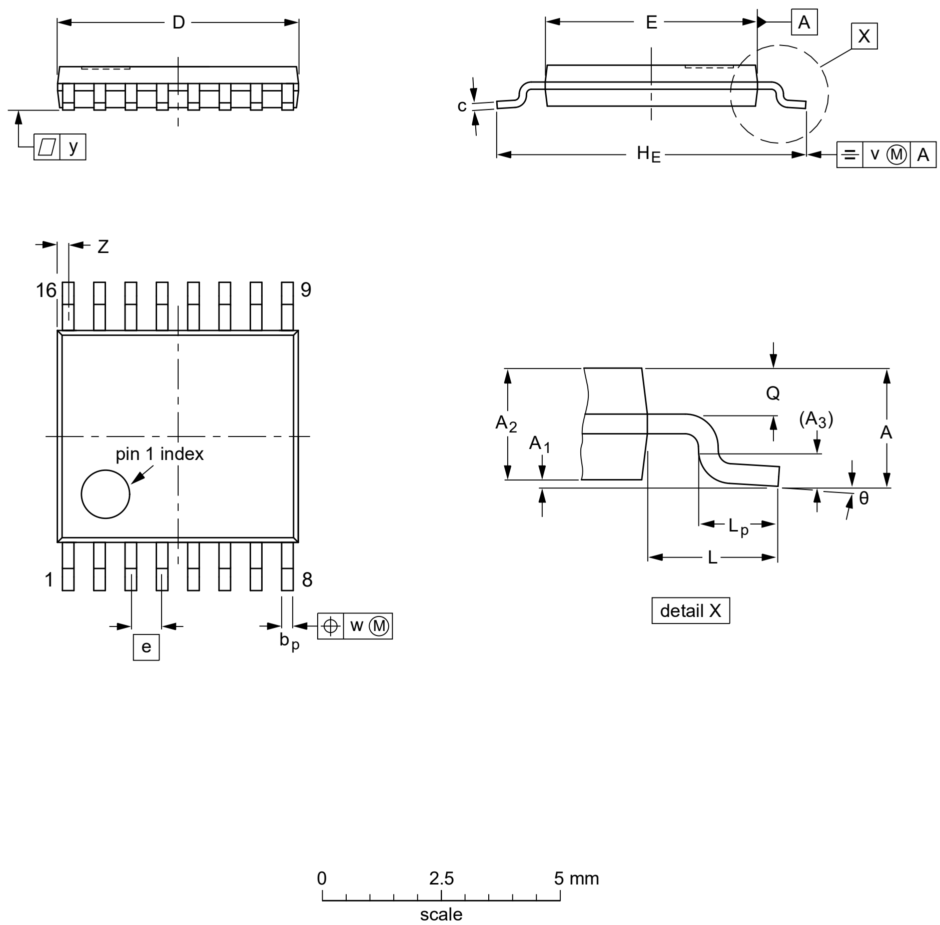
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT338-1		MO-150				~~99-12-27~~ 03-02-19

Fig. 22. Package outline SOT338-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 23. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 13. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 14. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4316 v.5	20210310	Product data sheet	-	74HC_HCT4316 v.4
Modifications:	• Section 8: Derating values for P_{tot} total power dissipation have changed. • Type number 74HCT4316DB (SOT338-1/SSOP16) removed.			
74HC_HCT4316 v.4	20181016	Product data sheet	-	74HC_HCT4316 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4316 v.3	20170102	Product data sheet	-	74HC_HCT4316_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74HC4316N and 74HCT4316N removed.			
74HC_HCT4316_CNV v.2	19930901	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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