74LV00A Quad 2-input NAND gate

Product data sheet

1. General description

The 74LV00A is a quad 2-input NAND gate.

Rev. 1 — 19 December 2018

Inputs are overvoltage tolerant. This feature allows the use of these devices as translators in mixed voltage environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 5.5 V
- Maximum t_{pd} of 9 ns at 5 V
- Typical $V_{OL(p)}$ < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25 °C
- Typical $V_{OH(v)} > 2.3 \text{ V}$ at $V_{CC} = 3.3 \text{ V}$, $T_{amb} = 25 \text{ °C}$
- Supports mixed-mode voltage operation on all ports
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 250 mA per JESD 78 Class II
- ESD protection:
 - MM: MM JESD22-A115-B exceeds 200 V
 - HBM: ANSI/ESDA/JEDEC JS-001 Class 3A exceeds 4 kV
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 2 kV
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

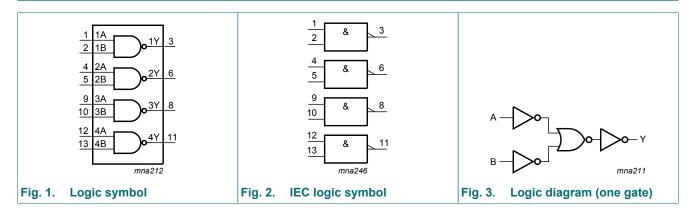
Table 1. Ordering information

Type number Package									
	Temperature range	Name	Description	Version					
74LV00APW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1					



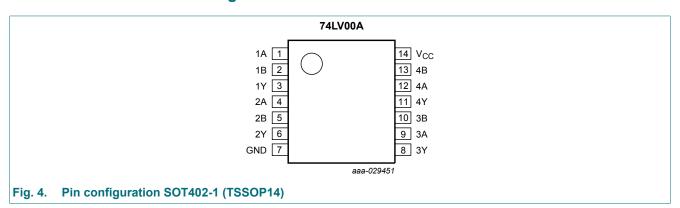
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4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A, 4A	1, 4, 9, 12	data input
1B, 2B, 3B, 4B	2, 5, 10, 13	data input
1Y, 2Y, 3Y, 4Y	3, 6, 8, 11	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

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6. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care.$

Input	Input					
nA	nB	nY				
L	X	Н				
X	L	Н				
Н	Н	L				

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+7.0	V
VI	input voltage		[1]	-0.5	+7.0	V
Vo	output voltage	output HIGH or LOW state	[2] [3]	-0.5	V _{CC} + 0.5	V
		output power-down	[2]	-0.5	+7.0	V
I _{IK}	input clamping current	V _I < 0 V		-20	-	mA
I _{OK}	output clamping current	V _O < 0 V		-50	-	mA
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±35	mA
I _{CC}	supply current			-	70	mA
I _{GND}	ground current			-70	-	mA
T _{stg}	storage temperature			-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[4]	-	500	mW

^[1] If the input current ratings are observed, the minimum input voltage ratings may be exceeded.

^[2] If the output current ratings are observed, the output voltage ratings may be exceeded.

^[3] This value is limited to 7 V maximum.

^[4] For SOT402-1 package: above 116 °C, the value of Ptot derates linearly at 7.3 mW/K.

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8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		2.0	5.0	5.5	V
VI	input voltage		0	-	5.5	V
Vo	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
		output power-down	0	-	5.5	V
T _{amb}	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	-	-	200	ns/V
		V _{CC} = 3.0 V to 3.6 V	-	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C	;	-40 °C to	o +85 °C	-40 °C to	Unit	
			Min	Тур	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 2 V	1.5	-	-	1.5	-	-	-	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	0.7V _{CC}	-	-	0.7V _{CC}	-	-	-	V
		V _{CC} = 3.0 V to 3.6 V	0.7V _{CC}	-	-	0.7V _{CC}	-	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	-	-	V
V _{IL}	LOW-level	V _{CC} = 2 V	-	-	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	-	0.3V _{CC}	V
V _{OH}	HIGH-level	$V_I = V_{IH}$ or V_{IL}								
	output voltage	V_{CC} = 2.0 V to 5.5 V; I_{O} = -50 μ A	V _{CC} -0.1	-	-	V _{CC} -0.1	-	V _{CC} -0.1	-	V
		V _{CC} = 2.3 V; I _O = -2 mA	2	-	-	2	-	2	-	V
		V _{CC} = 3.0 V; I _O = -6 mA	2.48	-	-	2.48	-	2.48	-	V
		V _{CC} = 4.5 V; I _O = -12 mA	3.8	-	-	3.8	-	3.8	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}							1	,
	output voltage	V _{CC} = 2.0 V to 5.5 V; I _O = 50 μA	-	-	0.1	-	0.1	-	0.1	V
		V _{CC} = 2.3 V; I _O = 2 mA	-	-	0.4	-	0.4	-	0.4	V
		V _{CC} = 3.0 V; I _O = 6 mA	-	-	0.44	-	0.44	-	0.44	V
		V _{CC} = 4.5 V; I _O = 12 mA	-	-	0.55	-	0.55	-	0.55	V
I _{OFF}	power-off leakage current	V_I or V_O = GND to 5.5 V; V_{CC} = 0 V	-	-	0.5	-	5	-	5	μΑ
I _I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 0$ V to 5.5 V	-	-	±0.1	-	±1	-	±1	μΑ
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5 \text{ V}$	-	-	2	-	20	-	20	μΑ

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10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions		25 °C		-40 °C to	o +85 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{pd}	propagation	nA, nB to nY; see Fig. 5								
	delay	V _{CC} = 2.3 V to 2.7 V								
		C _L = 15 pF	-	5.7	12.9	1	15	1	16	ns
		C _L = 50 pF	-	7.8	16.6	1	20	1	21	ns
		V _{CC} = 3.0 V to 3.6 V								
		C _L = 15 pF	-	4.3	7.9	1	9.5	1	10.5	ns
		C _L = 50 pF	-	6.1	11.4	1	13	1	14	ns
		V _{CC} = 4.5 V to 5.5 V								
		C _L = 15 pF	-	3.4	5.5	1	6.5	1	7	ns
		C _L = 50 pF	-	4.8	7.5	1	8.5	1	9	ns
C _I	input capacitance	$V_I = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	2	6	-	6	-	6	pF
Co	output capacitance	$V_O = V_{CC}$ or GND; $V_{CC} = 3.3 \text{ V}$	-	5.6	-	-	-	-	-	pF
C _{PD}	power dissipation	per buffer; $C_L = 50 \text{ pF}$; [3] f = 10 MHz; $V_I = \text{GND to } V_{CC}$								
	capacitance	V _{CC} = 3.3 V	-	9.3	-	-	-	-	-	pF
		V _{CC} = 5.0 V	-	9.5	-	-	-	-	-	pF

^[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 2.5 V, 3.3 V, and 5 V respectively, unless otherwise specified.

 f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$

Table 8. Noise characteristics at T_{amb} = 25 °C

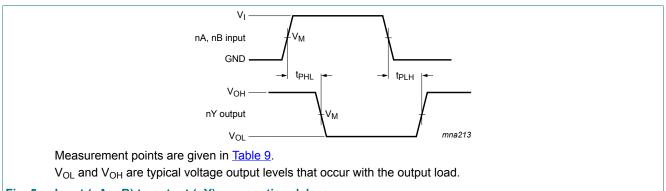
Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{OL(p)}$	LOW-level output voltage (peak)	$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	-	0.2	0.8	V
$V_{OL(v)}$	LOW-level output voltage (valley)	$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	-0.8	-0.1	-	V
$V_{OH(v)}$	HIGH-level output voltage (valley)	$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	-	3.1	-	V
V _{IH(AC)}	AC HIGH-level input voltage	$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	2.31	-	-	V
V _{IL(AC)}	AC LOW-level input voltage	$V_{CC} = 3.3 \text{ V}; C_L = 50 \text{ pF}$	-	-	0.99	V

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μ W): $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

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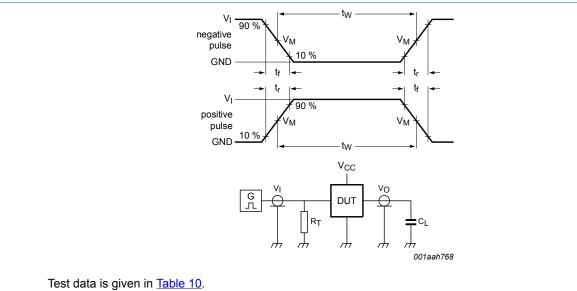
10.1. Waveforms and test circuit



Input (nA, nB) to output (nY) propagation delays

Table 9. Measurement points

Input	Output
V_{M}	V_{M}
0.5V _{CC}	0.5V _{CC}



Definitions test circuit:

 R_T = Termination resistance should be equal to output impedance Z_0 of the pulse generator

C_L = Load capacitance including jig and probe capacitance

Test circuit for measuring switching times Fig. 6.

Table 10. Test data

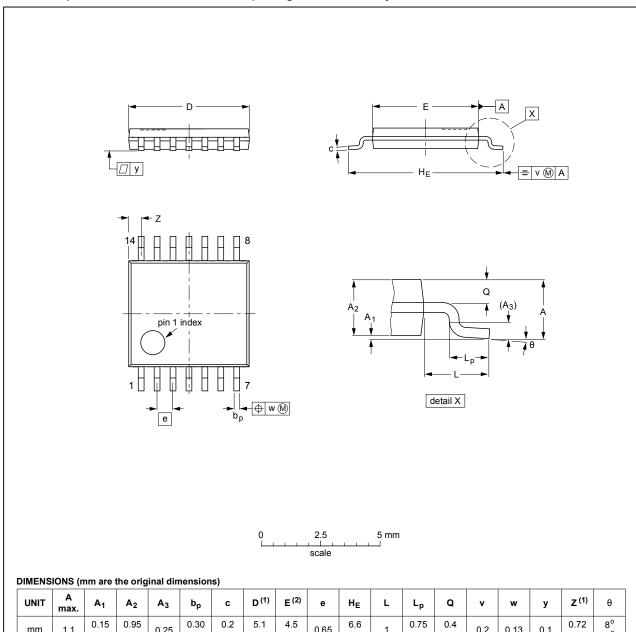
Input		Load	Test
V _I	t _r , t _f	CL	
GND to V _{CC}	3.0 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

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11. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



UNIT	A max.	A ₁	A ₂	A ₃	b _p	С	D ⁽¹⁾	E (2)	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT402-1		MO-153			99-12-27 03-02-18

Fig. 7. Package outline SOT402-1 (TSSOP14)

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12. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charge Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TBD	To Be Determined

13. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV00A v.1	20181219	Product data sheet	-	-

Product data sheet

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14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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