74LV74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 5 — 24 March 2021 Product data sheet

1. General description

The 74LV74 is a dual positive edge triggered D-type flip-flop with individual data (nD), clock (nCP), set ($n\overline{SD}$) and reset ($n\overline{RD}$) inputs, and complementary nQ and $n\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the nQ output. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess V_{CC}.

2. Features and benefits

- Wide supply voltage range from 1.0 V to 5.5 V
- Optimized for low voltage applications from 1.0 V to 3.6 V
- CMOS low power dissipation
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Direct interface with TTL levels (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LV74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

nexperia

4. Functional diagram

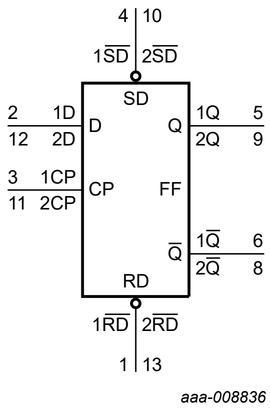


Fig. 1. Logic symbol

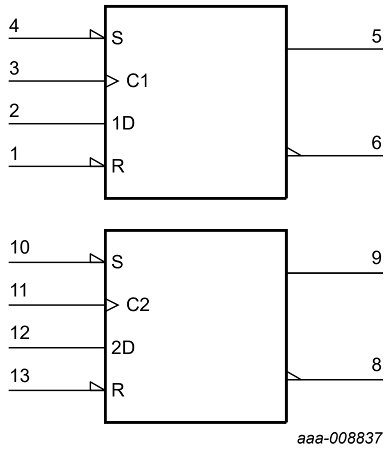


Fig. 2. IEC logic symbol

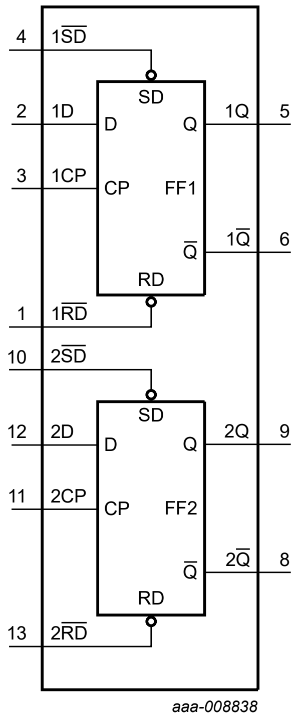


Fig. 3. Functional diagram

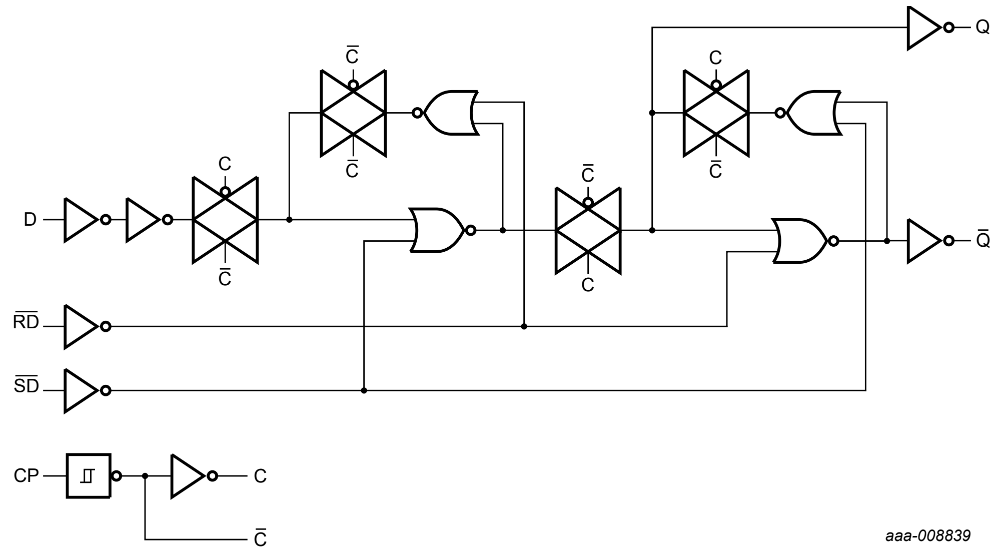


Fig. 4. Logic diagram (one flip-flop)

5. Pinning information

5.1. Pinning

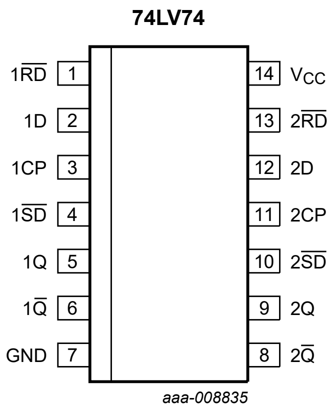


Fig. 5. Pin configuration SOT108-1 (SO14)

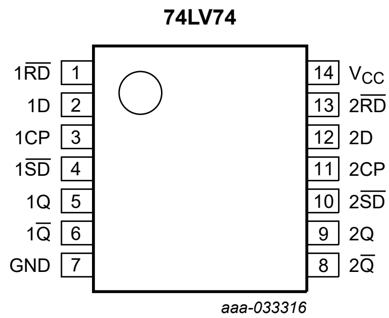


Fig. 6. Pin configuration SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{RD}$, $2\overline{RD}$	1, 13	asynchronous reset-direct input (active-LOW)
1D, 2D	2, 12	data inputs
1CP, 2CP	3, 11	clock input (LOW-to-HIGH), edge-triggered)
$1\overline{SD}$, $2\overline{SD}$	4, 10	asynchronous set-direct input (active-LOW)
1Q, 2Q	5, 9	true flip-flop outputs
$1\overline{Q}$, $2\overline{Q}$	6, 8	complement flip-flop outputs
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW-to-HIGH clock transition; Q_{n+1} = state after the next LOW-to-HIGH CP transition

Input				Output			
$n\overline{SD}$	$n\overline{RD}$	nCP	nD	nQ	$n\overline{Q}$	Q_{n+1}	$n\overline{Q}_{n+1}$
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage	[1]	-0.5	+7	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{CC} + 0.5 V	-	20	mA
V_I	input voltage	[1]	-0.5	+7	V
I_{OK}	output clamping current	V_O > V_{CC} or V_O < 0	-	±50	mA
I_O	output current	-0.5 V < V_O < V_{CC} + 0.5 V	-	±25	mA
I_{CC}	supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [2]	-	500	

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage [1]		1.0	3.3	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 1.0 V to 2.0 V	0	-	500	ns/V
		V_{CC} = 2.0 V to 2.7 V	0	-	200	ns/V
		V_{CC} = 2.7 V to 3.6 V	0	-	100	ns/V
		V_{CC} = 3.6 V to 5.5 V	0	-	50	ns/V

[1] 74LV74 is guaranteed to function down to V_{CC} = 1.0 V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2 V to V_{CC} = 5.5 V.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	V_{CC} = 1.2 V	0.9	-	-	0.9	-	V
		V_{CC} = 2.3 V to 2.7 V	1.4	-	-	1.4	-	V
		V_{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V_{CC} = 4.5 V to 5.5 V	$0.7V_{CC}$	-	-	$0.7V_{CC}$	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 1.2 V	-	-	0.3	-	0.3	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.6	-	0.6	V
		V_{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V_{CC} = 4.5 V to 5.5 V	-	-	$0.3V_{CC}$	-	$0.3V_{CC}$	
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = -100 μA						
		V_{CC} = 1.2 V	-	1.2		-		
		V_{CC} = 2.0 V	1.8	2.0	-	1.8	-	V
		V_{CC} = 2.7 V	2.5	2.7	-	2.5	-	V
		V_{CC} = 3.0 V	2.8	3.0	-	2.8	-	V
		V_{CC} = 4.5 V	4.3	4.5	-	4.3	-	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		V_{CC} = 3.0 V; I_O = -6 mA	2.40	2.82	-	2.20	-	V
		V_{CC} = 4.5 V; I_O = -12 mA	3.60	4.20	-	3.50	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; I_O = 100 μA						
		V_{CC} = 1.2 V	-	0	-	-	-	
		V_{CC} = 2.0 V	-	0	0.2		0.2	V
		V_{CC} = 2.7 V	-	0	0.2		0.2	V
		V_{CC} = 3.0 V	-	0	0.2		0.2	V
		V_{CC} = 4.5 V	-	0	0.2		0.2	V
		standard outputs: $V_I = V_{IH}$ or V_{IL}						
		V_{CC} = 3.0 V; I_O = 6 mA	-	0.25	0.40	-	0.50	V
		V_{CC} = 4.5 V; I_O = 12 mA	-	0.35	0.55	-	0.65	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1	-	±1	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	20	-	80	μA
ΔI_{CC}	additional supply current	$V_I = V_{CC} - 0.6$ V; V_{CC} = 2.7 V to 3.6 V	-	-	500	-	850	μA
C_I	input capacitance		-	3.5	-			pF

[1] Typical values are measured at T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

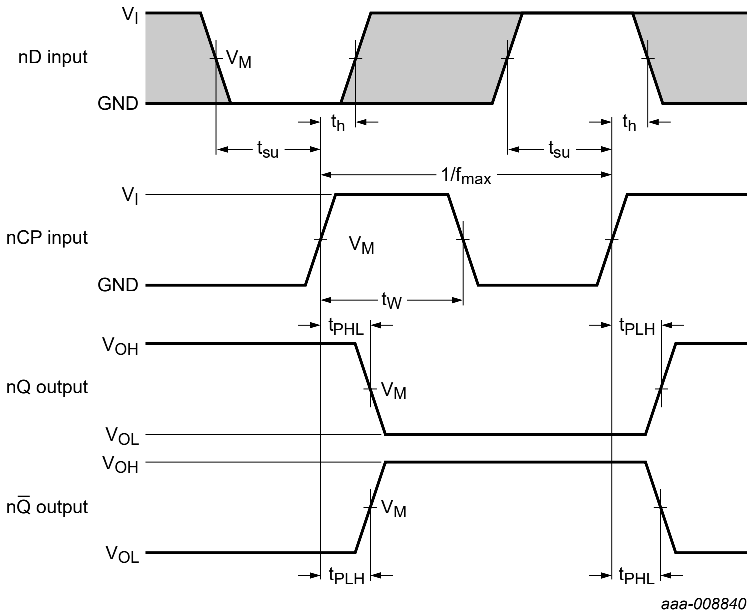
GND (ground = 0 V): for test circuit, see Fig. 9

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nCP to nQ, $n\overline{Q}$; see Fig. 7	[2]						
		V_{CC} = 1.2 V		-	70	-	-	-	ns
		V_{CC} = 2.0 V		-	24	44	-	56	ns
		V_{CC} = 2.7 V		-	18	28	-	41	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	13	26	-	33	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	11	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	9.5	17	-	23	ns
		$n\overline{SD}$ to nQ, $n\overline{Q}$; see Fig. 8							
		V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	31	46	-	58	ns
		V_{CC} = 2.7 V		-	23	34	-	43	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	14	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	12	19	-	24	ns
		$n\overline{RD}$ to nQ, $n\overline{Q}$; see Fig. 8							
		V_{CC} = 1.2 V		-	90	-	-	-	ns
		V_{CC} = 2.0 V		-	31	46	-	58	ns
		V_{CC} = 2.7 V		-	23	34	-	43	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	-	17	27	-	34	ns
		V_{CC} = 3.3 V; C_L = 15 pF		-	14	-	-	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	-	12	19	-	24	ns
t_W	pulse width	nCP input HIGH to LOW; see Fig. 7							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	15	6	-	18	-	ns
		$n\overline{SD}$ or $n\overline{RD}$ pulse width LOW; see Fig. 8							
		V_{CC} = 2.0 V		34	10	-	41	-	ns
		V_{CC} = 2.7 V		25	8	-	30	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	20	7	-	24	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	15	6	-	18	-	ns
t_{rec}	recovery time	$n\overline{RD}$; see Fig. 8							
		V_{CC} = 1.2 V		-	5	-	-	-	ns
		V_{CC} = 2.0 V		14	2	-	15	-	ns
		V_{CC} = 2.7 V		10	1	-	11	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	8	1	-	9	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	6	1	-	7	-	ns

Symbol	Parameter	Conditions		-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ[1]	Max	Min	Max	
t_{su}	set-up time	nD to nCP; see Fig. 7							
		V_{CC} = 1.2 V		-	10	-	-	-	ns
		V_{CC} = 2.0 V		22	4	-	26	-	ns
		V_{CC} = 2.7 V		12	3	-	15	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	8	2	-	10	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	6	1	-	8	-	ns
t_h	hold time	nD to nCP; see Fig. 7							
		V_{CC} = 1.2 V		-	-10	-	-	-	ns
		V_{CC} = 2.0 V		3	-2	-	3	-	ns
		V_{CC} = 2.7 V		3	-2	-	3	-	ns
		V_{CC} = 3.0 V to 3.6 V	[3]	3	-2	-	3	-	ns
		V_{CC} = 4.5 V to 5.5 V	[4]	3	-2	-	3	-	ns
f_{max}	maximum frequency	nCP; see Fig. 7							
		V_{CC} = 2.0 V		14	40	-	12	-	MHz
		V_{CC} = 2.7 V		50	90	-	40	-	MHz
		V_{CC} = 3.0 V to 3.6 V	[3]	60	100	-	48	-	MHz
		V_{CC} = 4.5 V to 5.5 V	[4]	70	110	-	56	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}	[5]	-	24	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C.
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.
[3] Typical value measured at V_{CC} = 3.3 V.
[4] Typical values are measured at V_{CC} = 5.0 V.
[5] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ (P_D in μW), where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V.

10.1. Waveforms and test circuit

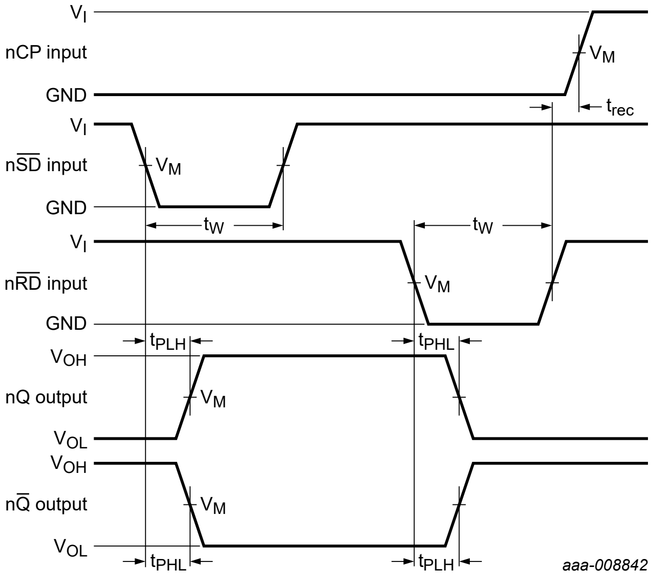


Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 7. Clock pulse (nCP) to output (nQ, nQ̄) propagation delays, nCP pulse width and maximum frequency



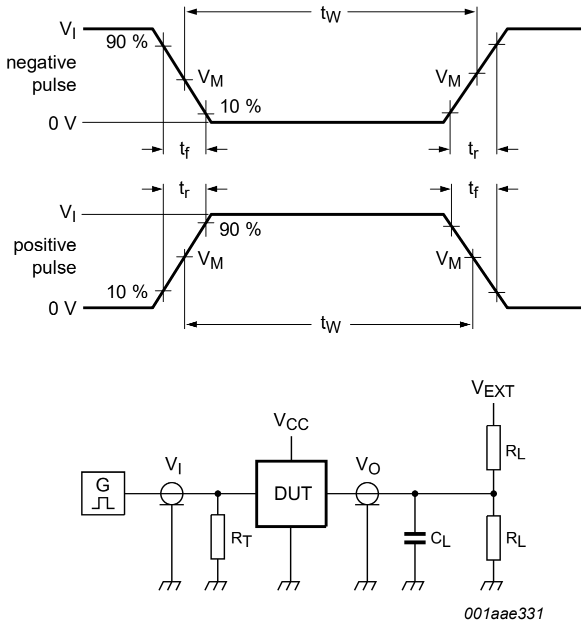
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. The set (nS̄D̄) and reset (nR̄D̄) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the nR̄D̄ to nCP recovery time

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
< 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$
2.7 V to 3.6 V	1.5 V	1.5 V
≥ 4.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in Table 9.
Definitions for test circuit:
R_L = Load resistance.
C_L = Load capacitance including jig and probe capacitance.
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.
V_{EXT} = External voltage for measuring switching times.

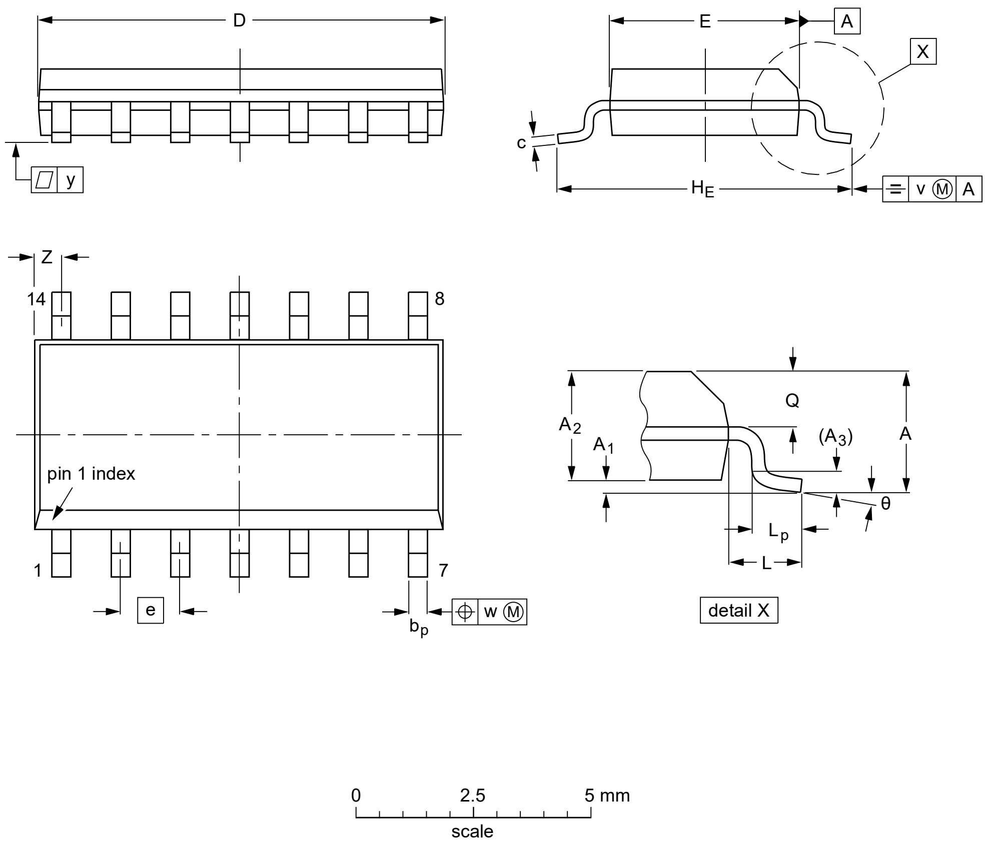
Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
< 2.7 V	V_{CC}	2.5 ns	50 pF	1 kΩ	open
2.7 V to 3.6 V	2.7 V	2.5 ns	50 pF, 15 pF	1 kΩ	open
≥ 4.5 V	V_{CC}	2.5 ns	50 pF	1 kΩ	open

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

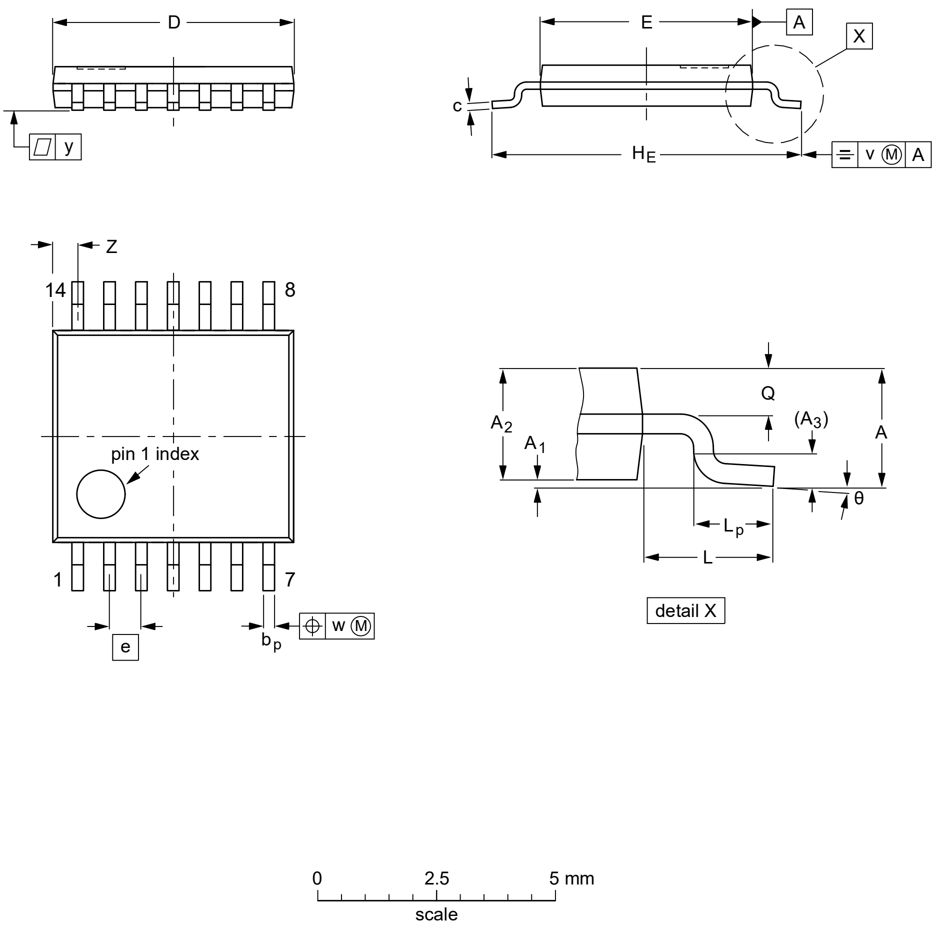
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig. 11. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV74 v.5	20210324	Product data sheet	-	74LV74 v.4
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Section 7: Derating values for P_{tot} total power dissipation updated. • Type number 74LV74DB (SOT337-1/SSOP14) removed.			
74LV74 v.4	20151209	Product data sheet	-	74LV74 v.3
Modifications:	• Type number 74LV74N (SOT27-1) removed.			
74LV74 v.3	20130909	Product data sheet	-	74LV74_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Family data added, see Section 9			
74LV74_CNV v.2	April 1998	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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Date of release: 24 March 2021

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