74LVC11-Q100

Triple 3-input AND gate Rev. 2 — 13 January 2020

Product data sheet

1. General description

The 74LVC11-Q100 provides three 3-input AND functions.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Wide supply voltage range from 1.2 V to 3.6 V
- Inputs accept voltages up to 5.5 V
- CMOS low power consumption
- · Direct interface with TTL levels
- · Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

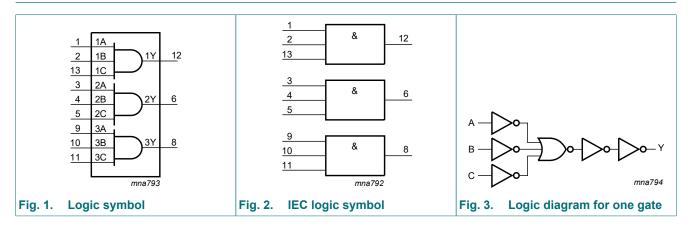
3. Ordering information

Table 1. Ordering information

Type number	Package	Package									
	Temperature range	Name	Description	Version							
74LVC11D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1							
74LVC11PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1							
74LVC11BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1							

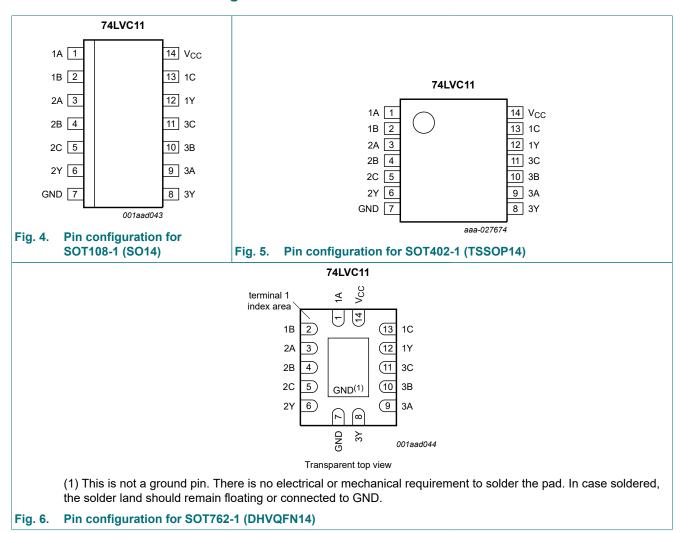


4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 9	data input
1B, 2B, 3B	2, 4, 10	data input
1C, 2C, 3C	13, 5, 11	data input
1Y, 2Y, 3Y	12, 6, 8	data output
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input	Input							
nA	nB	nC	nY					
L	Х	X	L					
X	L	X	L					
X	X	L	L					
Н	Н	Н	Н					

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CC}	supply voltage			-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V		-50	-	mA
VI	input voltage		[1]	-0.5	+6.5	V
I _{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0 V$		-	±50	mA
Vo	output voltage		[2]	-0.5	V _{CC} + 0.5	V
Io	output current	$V_O = 0 V \text{ to } V_{CC}$		-	±50	mA
I _{CC}	supply current			-	100	mA
I _{GND}	ground current			-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[3]	-	500	mW
T _{stg}	storage temperature			-65	+150	°C

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
- [2] The output voltage ratings may be exceeded if the output current ratings are observed.
- [3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C. For SOT402-1 (TSSOP14) packages: P_{tot} derates linearly with 7.3 mW/K above 81 °C. For SOT762-1 (DHVQFN14) packages: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
VI	input voltage		0	-	5.5	V
Vo	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
rate	rate	V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40	°C to +8	55 °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
V _{IH}	HIGH-level	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	0.65xV _{CC}	-	-	0.65xV _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
	input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35xV _{CC}	-	0.35xV _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level V _I = V _{IH} or V _{IL}							
	output voltage	I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} -0.2	-	-	V _{CC} -0.3	-	V
	I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V	
		I_{O} = -8 mA; V_{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.2	-	-	2.0	-	V
V _{OL}	LOW-level	$V_I = V_{IH}$ or V_{IL}						
	output voltage	I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μΑ
I _{CC}	supply current	$V_{CC} = 3.6 \text{ V}; V_I = V_{CC} \text{ or GND}; I_O = 0 \text{ A}$	-	0.1	10	-	40	μA
ΔI _{CC}	additional supply current	per input pin; V _{CC} = 2.7 V to 3.6 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	-	5000	μΑ

Symbol	Parameter	Conditions	-40 °C to +85 °C		-40 °C to	Unit		
			Min	Typ[1]	Max	Min	Max	
Cı	input capacitance	V_{CC} = 0 V to 3.6 V; V_{I} = GND to V_{CC}	-	5.0	-	-	-	pF

^[1] All typical values are measured at V_{CC} = 3.3 V (unless stated otherwise) and T_{amb} = 25 °C.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 8.

Symbol	Parameter	Conditions	-40	°C to +85	S °C	-40 °C to	+125 °C	Unit
			Min	Typ[1]	Max	Min	Max	
t _{pd}	propagation delay	nA, nB, nC to nY; see Fig. 7 [2]						
		V _{CC} = 1.2 V	-	14.0	-	-	-	ns
	V _{CC} = 1.65 V to 1.95 V	1.0	4.7	12.2	1.0	14.1	ns	
	V _{CC} = 2.3 V to 2.7 V	1.5	2.8	6.9	1.5	8.0	ns	
		V _{CC} = 2.7 V	1.5	2.9	7.0	1.5	8.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.5	2.5	6.2	1.5	7.2	ns
C _{PD}	power dissipation	per gate; $V_I = GND$ to V_{CC} [3]						
	capacitance	V _{CC} = 1.65 V to 1.95 V	-	3.1	-	-	-	pF
		V _{CC} = 2.3 V to 2.7 V	-	6.2	-	-	-	pF
		V _{CC} = 3.0 V to 3.6 V	-	9.0	-	-	-	pF

Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.2 V, 1.8 V, 2.5 V, 2.7 V, and 3.3 V respectively.

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in Volts

N = number of inputs switching

 $\Sigma(C_L \times V_{CC}^2 \times f_0) = \text{sum of the outputs}$

 t_{pd} is the same as t_{PLH} and t_{PHL} . C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

10.1. Waveforms and test circuit

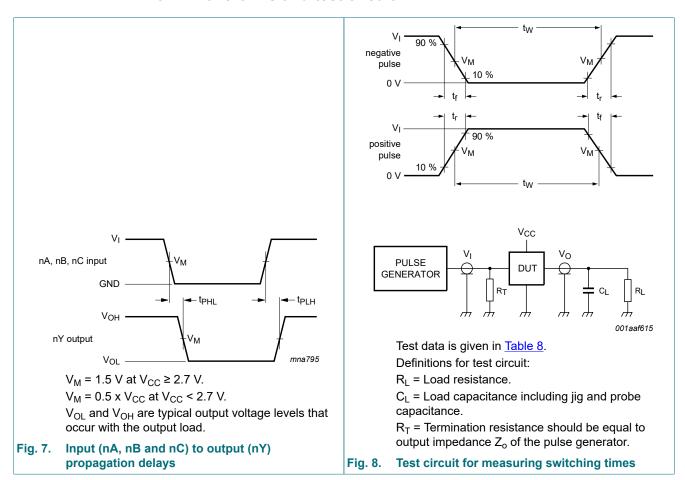


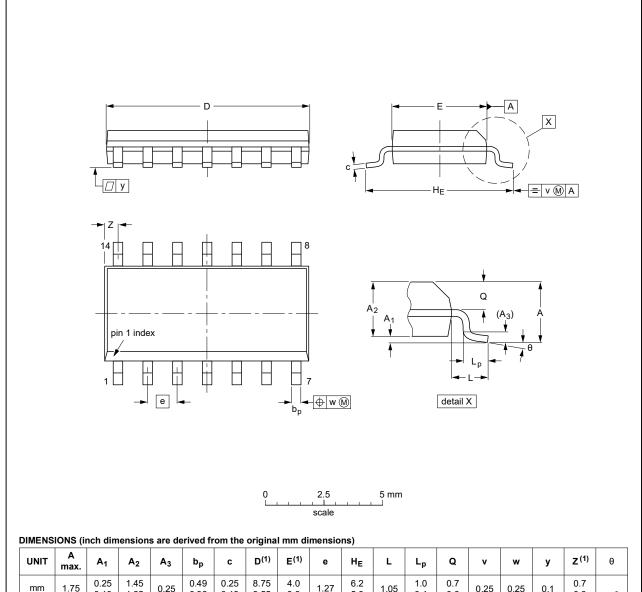
Table 8. Test data

Supply voltage	Input		Load	Load			
	VI	t _r , t _f	C _L	R _L			
1.2 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ			
1.65 V to 1.95 V	V _{CC}	≤ 2 ns	30 pF	1 kΩ			
2.3 V to 2.7 V	V _{CC}	≤ 2 ns	30 pF	500 Ω			
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω			

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	0°

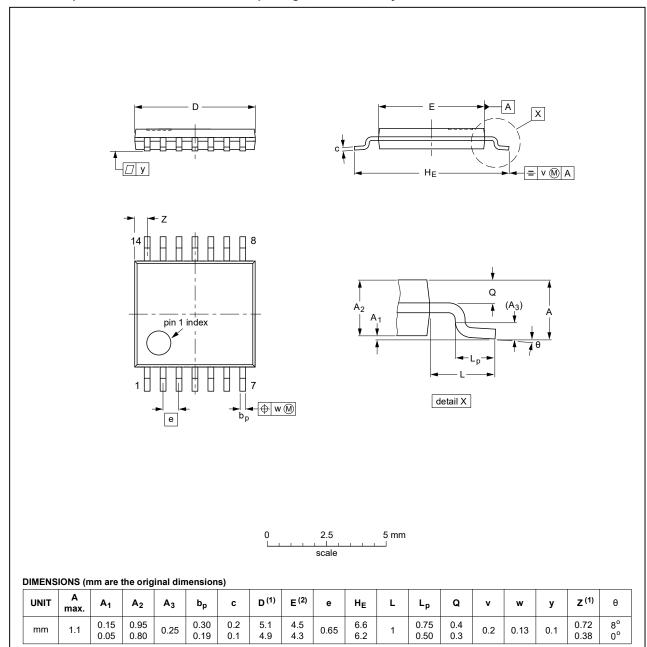
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	N IEC JEDEC JEITA		JEITA		PROJECTION	ISSUE DATE	
SOT108-1	076E06	MS-012				99-12-27 03-02-19	

Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	IEC JEDEC JEITA			PROJECTION	ISSUE DATE	
SOT402-1		MO-153				99-12-27 03-02-18	

Fig. 10. Package outline SOT402-1 (TSSOP14)

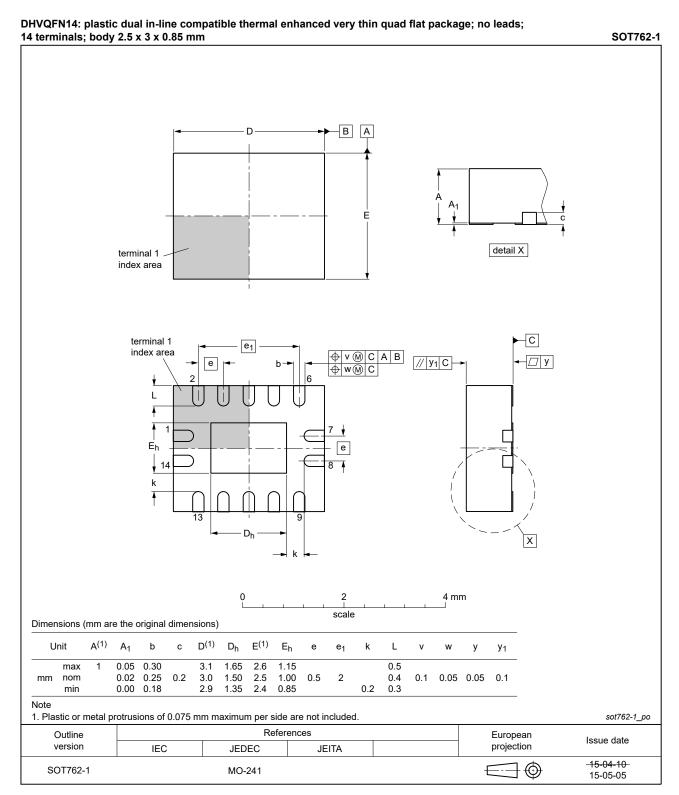


Fig. 11. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

1440-1411-1411-1411-1411-1411-1411-1411							
Document ID	Release date	Data sheet status	Change notice	Supersedes			
74LVC11_Q100 v.2	20200113	Product data sheet	-	74LVC11_Q100 v.1			
Modifications:	 Table 4: Derating values for P_{tot} total power dissipation updated. Added type number 74LVC11BQ-Q100 (SOT762-1/DHVQFN14) 						
74LVC11_Q100 v.1	20180307	Product data sheet	-	-			

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Product [short] data sheet	Production	This document contains the product specification.

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