

74LVC138A-Q100

3-to-8 line decoder/demultiplexer; inverting

Rev. 2 — 23 January 2019

Product data sheet

1. General description

The 74LVC138A-Q100 is a 3-to-8 line decoder/demultiplexer. It accepts three binary weighted address inputs (A0, A1 and A2). When the inputs are enabled, it provides eight mutually exclusive outputs (Y0 to Y7) that are LOW when selected.

There are three enable inputs: two active LOW ($\bar{E}1$ and $\bar{E}2$) and one active HIGH (E3). Every output is HIGH unless $\bar{E}1$ and $\bar{E}2$ are LOW and E3 is HIGH.

This multiple enable function allows easy parallel expansion of the device to a 1-of-32 (5 lines to 32 lines) decoder with just four 74LVC138A-Q100 devices and one inverter. The 74LVC138A-Q100 can be used as an eight output demultiplexer by using one of the active LOW enable inputs as the data input and the remaining enable inputs as strobes. Unused enable inputs must be permanently tied to their appropriate active HIGH or LOW state.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

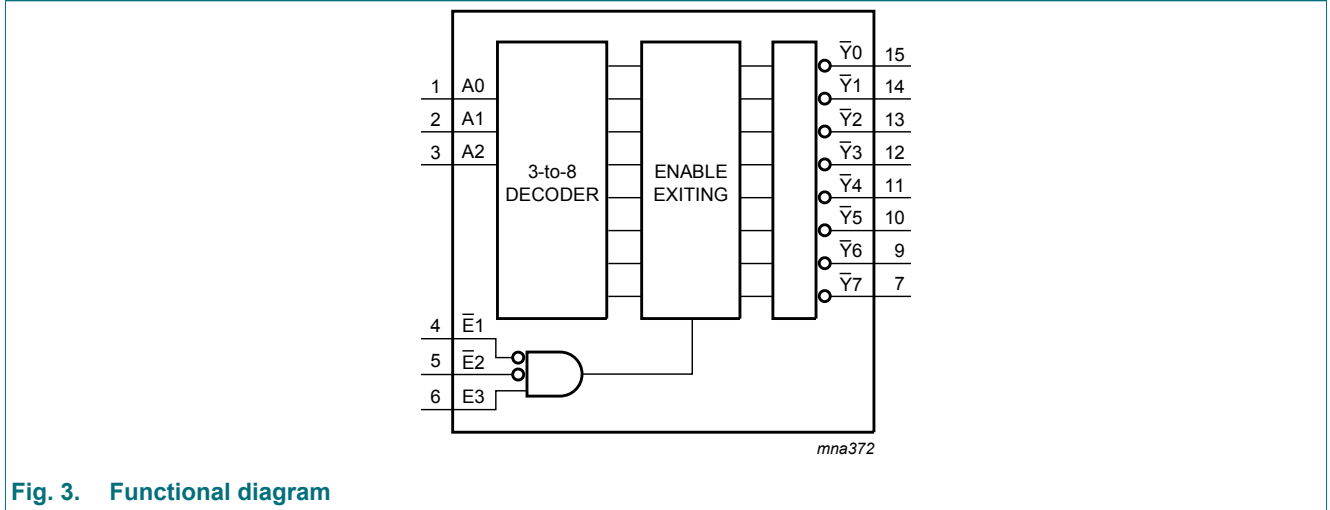
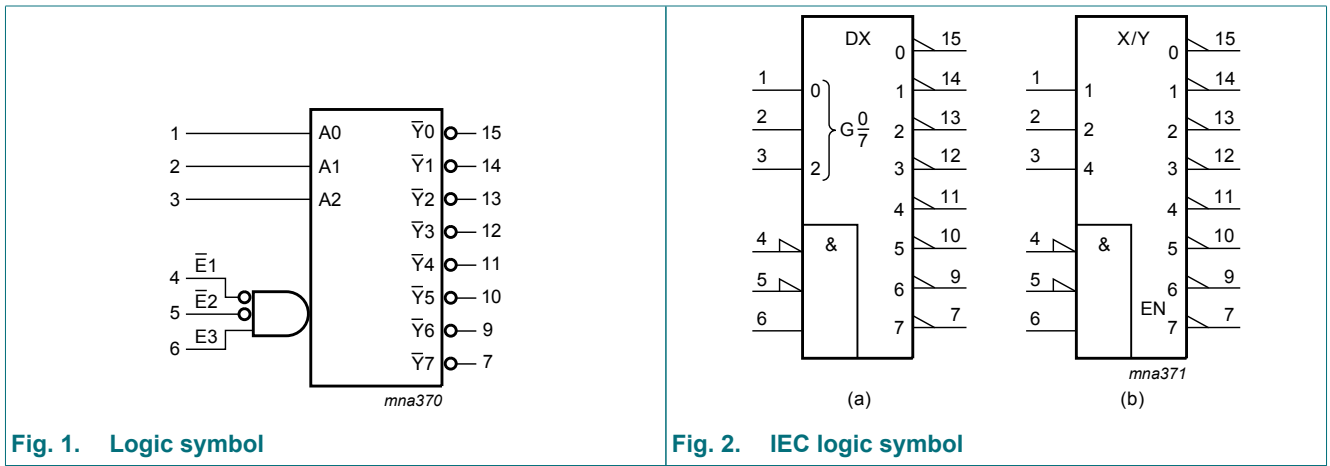
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- 5 V tolerant inputs for interfacing with 5 V logic
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Demultiplexing capability
- Multiple input enable for easy expansion
- Ideal for memory chip select decoding
- Mutually exclusive outputs
- Output drive capability 50 Ω transmission lines at 125 °C
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - MIL-STD-883, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)
- Multiple package options

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC138AD-Q100	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC138APW-Q100	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC138ABQ-Q100	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal-enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

4. Functional diagram



5. Pinning information

5.1. Pinning

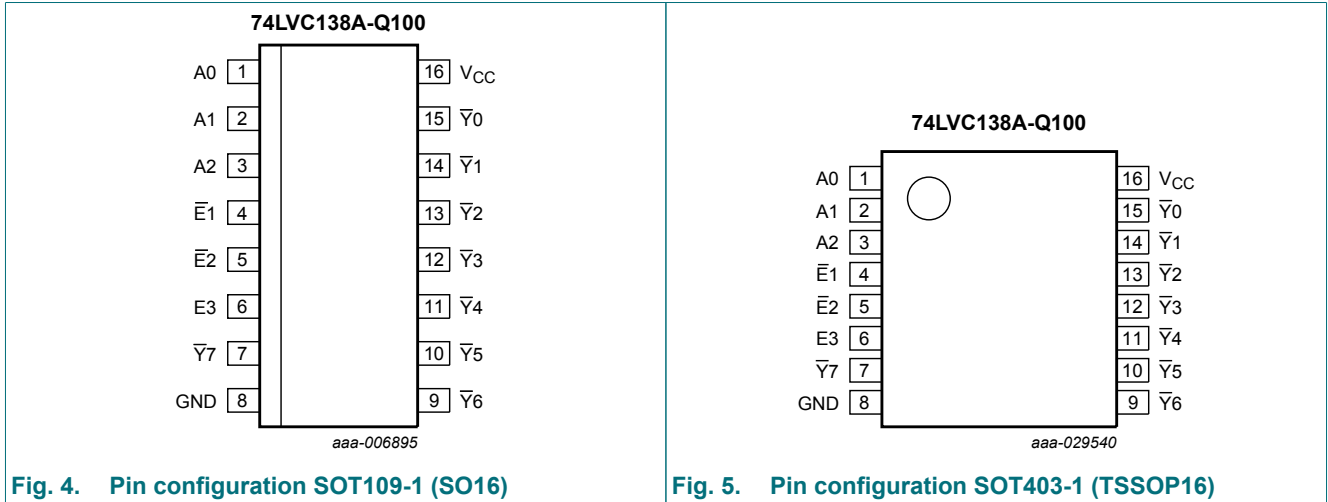


Fig. 4. Pin configuration SOT109-1 (SO16)

Fig. 5. Pin configuration SOT403-1 (TSSOP16)

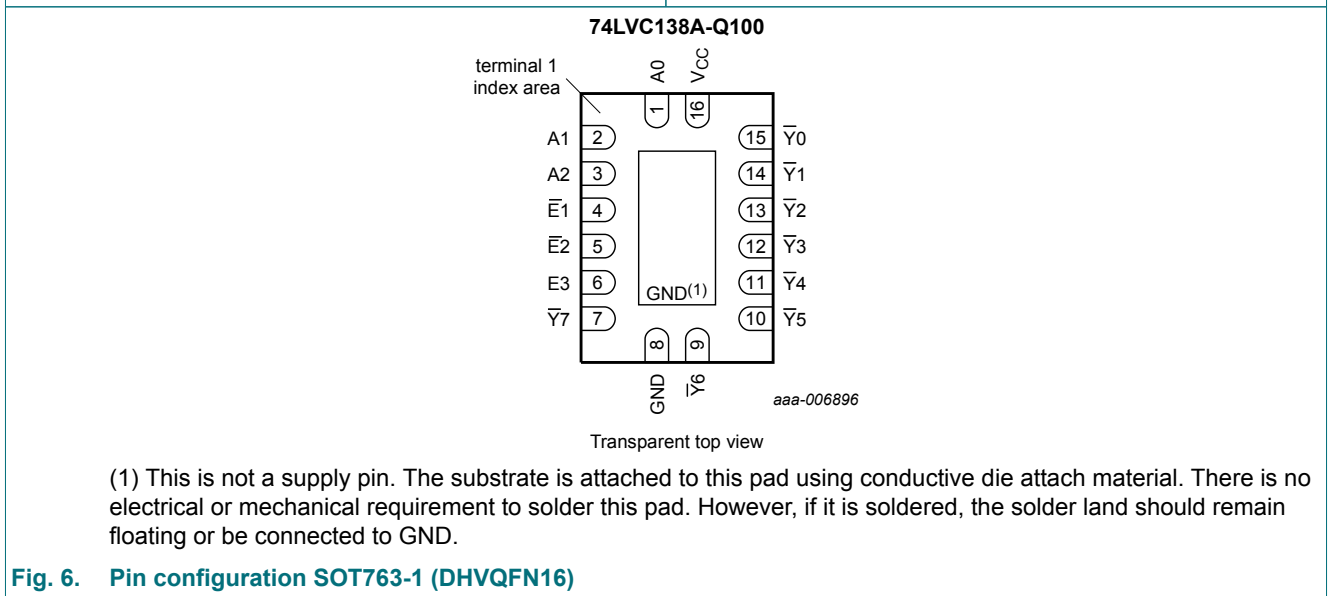


Fig. 6. Pin configuration SOT763-1 (DHVQFN16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
A0, A1, A2	1, 2, 3	address input
$\bar{E}1, \bar{E}2$	4, 5	enable input (active LOW)
E3	6	enable input (active HIGH)
GND	8	ground (0 V)
$\bar{Y}0, \bar{Y}1, \bar{Y}2, \bar{Y}3, \bar{Y}4, \bar{Y}5, \bar{Y}6, \bar{Y}7$	15, 14, 13, 12, 11, 10, 9, 7	output
V _{CC}	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input						Output							
E1	E2	E3	A0	A1	A2	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
			H	L	L	H	L	H	H	H	H	H	H
			L	H	L	H	H	L	H	H	H	H	H
			H	H	L	H	H	H	L	H	H	H	H
			L	L	H	H	H	H	H	L	H	H	H
			H	L	H	H	H	H	H	H	L	H	H
			L	H	H	H	H	H	H	H	H	L	H
			H	H	H	H	H	H	H	H	H	H	H

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
V_I	input voltage		[1] -0.5	+6.5	V
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
V_O	output voltage	output HIGH or LOW state	[2] -0.5	$V_{CC} + 0.5$	V
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[3] -	500	mW

[1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.

[2] The output voltage ratings may be exceeded if the output current ratings are observed.

[3] For SO16 packages: above 70 °C the value of P_D derates linearly with 8 mW/K.

For TSSOP16 packages: above 60 °C the value of P_D derates linearly with 5.5 mW/K.

For DHVQFN16 packages: above 60 °C the value of P_D derates linearly with 4.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage	output HIGH or LOW state	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	0	-	20	ns/V
		V _{CC} = 2.7 V to 3.6 V	0	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	1.08	-	-	1.08	-	V
		V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	0.12	-	0.12	V
		V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = -100 μA; V _{CC} = 1.65 V to 3.6 V	V _{CC} - 0.2	-	-	V _{CC} - 0.3	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	1.05	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.8	-	-	1.65	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	2.05	-	V
		I _O = -18 mA; V _{CC} = 3.0 V	2.4	-	-	2.25	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}						
		I _O = 100 μA; V _{CC} = 1.65 V to 3.6 V	-	-	0.2	-	0.3	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	-	0.65	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.6	-	0.8	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.4	-	0.6	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	-	0.8	V
I _I	input leakage current	V _{CC} = 3.6 V; V _I = 5.5 V or GND	-	±0.1	±5	-	±20	μA
I _{CC}	supply current	V _{CC} = 3.6 V; V _I = V _{CC} or GND; I _O = 0 A	-	0.1	10	-	40	μA

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_{CC} = 2.7 \text{ V to } 3.6 \text{ V};$ $V_I = V_{CC} - 0.6 \text{ V}; I_O = 0 \text{ A}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0 \text{ V to } 3.6 \text{ V};$ $V_I = \text{GND to } V_{CC}$	-	4.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3 \text{ V}$ (unless stated otherwise) and $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$.

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 9.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	An to \bar{Y}_n ; see Fig. 7 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	5.2	11.5	0.5	12.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	3.0	6.5	1.5	7.3	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.2	6.8	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.7	5.8	1.0	7.5	ns
		E3 to \bar{Y}_n ; see Fig. 7 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	14	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.5	11.4	1.0	12.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	3.2	6.5	1.5	7.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.5	3.3	6.8	1.5	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.9	5.8	1.0	7.5	ns
		En to \bar{Y}_n ; see Fig. 8 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	15	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.6	11.5	1.0	12.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.8	3.3	6.5	1.8	7.3	ns
$V_{CC} = 2.7 \text{ V}$	1.5	3.4	6.4	1.5	8.0	ns		
$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.9	5.8	1.0	7.5	ns		
$t_{sk(o)}$	output skew time	[3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	$V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	9.9	-			pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	15.8	-			pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	21.1	-			pF

[1] Typical values are measured at $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ and $V_{CC} = 1.2 \text{ V}, 1.8 \text{ V}, 2.5 \text{ V}, 2.7 \text{ V},$ and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz; f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

N = number of inputs switching

$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

10.1. Waveforms and test circuit

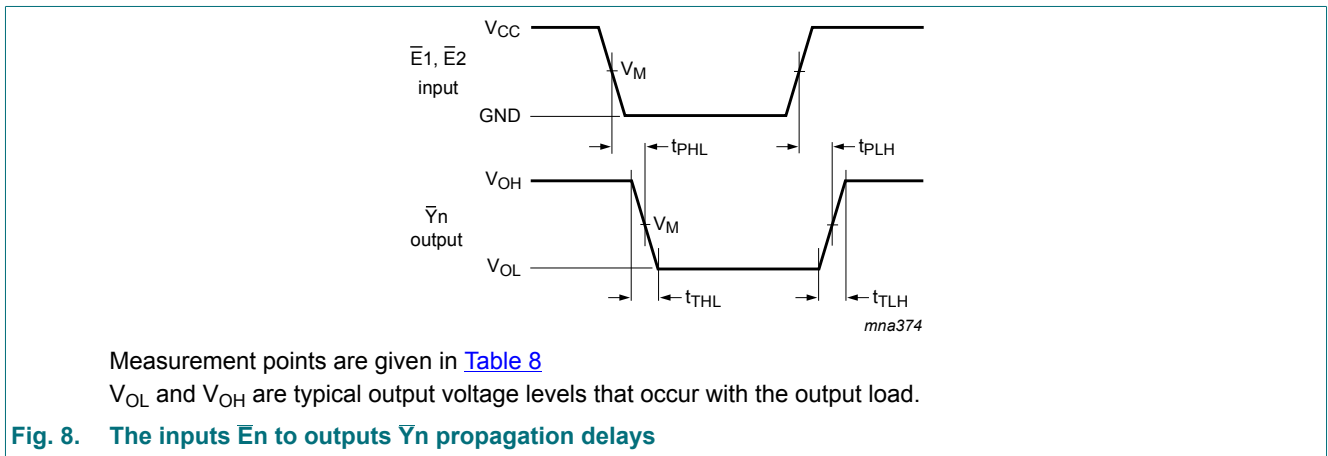
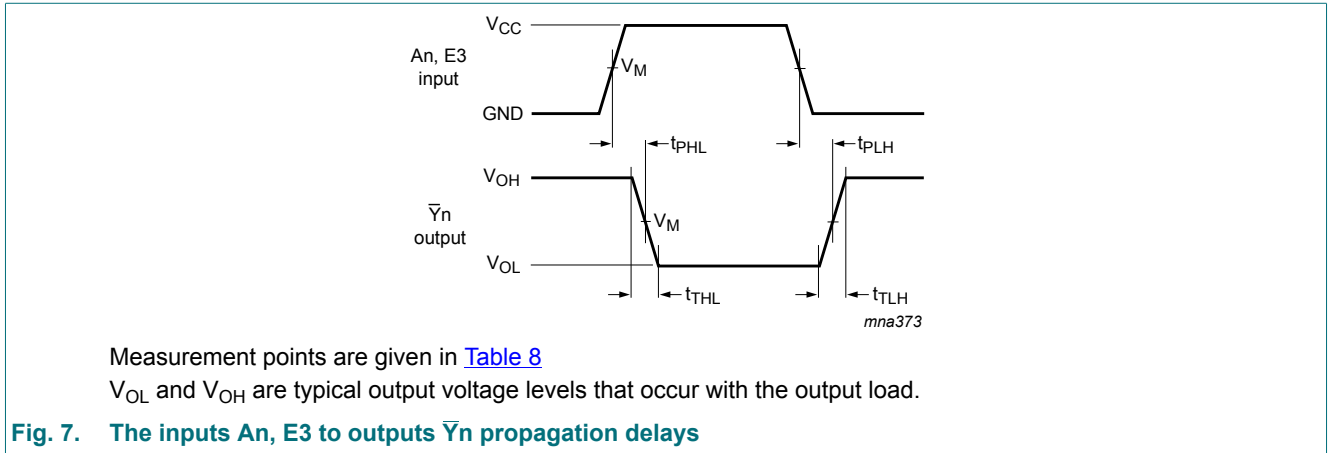
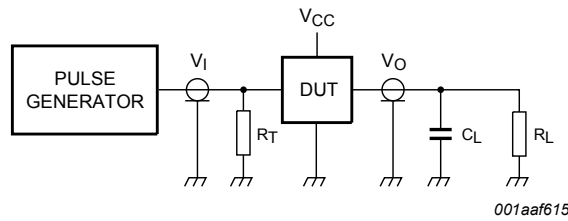
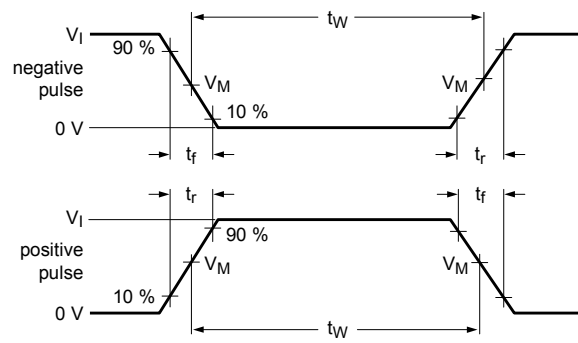


Table 8. Measurement points

Supply voltage	Input		Output
V_{CC}	V_I	V_M	V_M
1.2 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
1.65 V to 1.95 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V



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Test data is given in [Table 9](#). Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

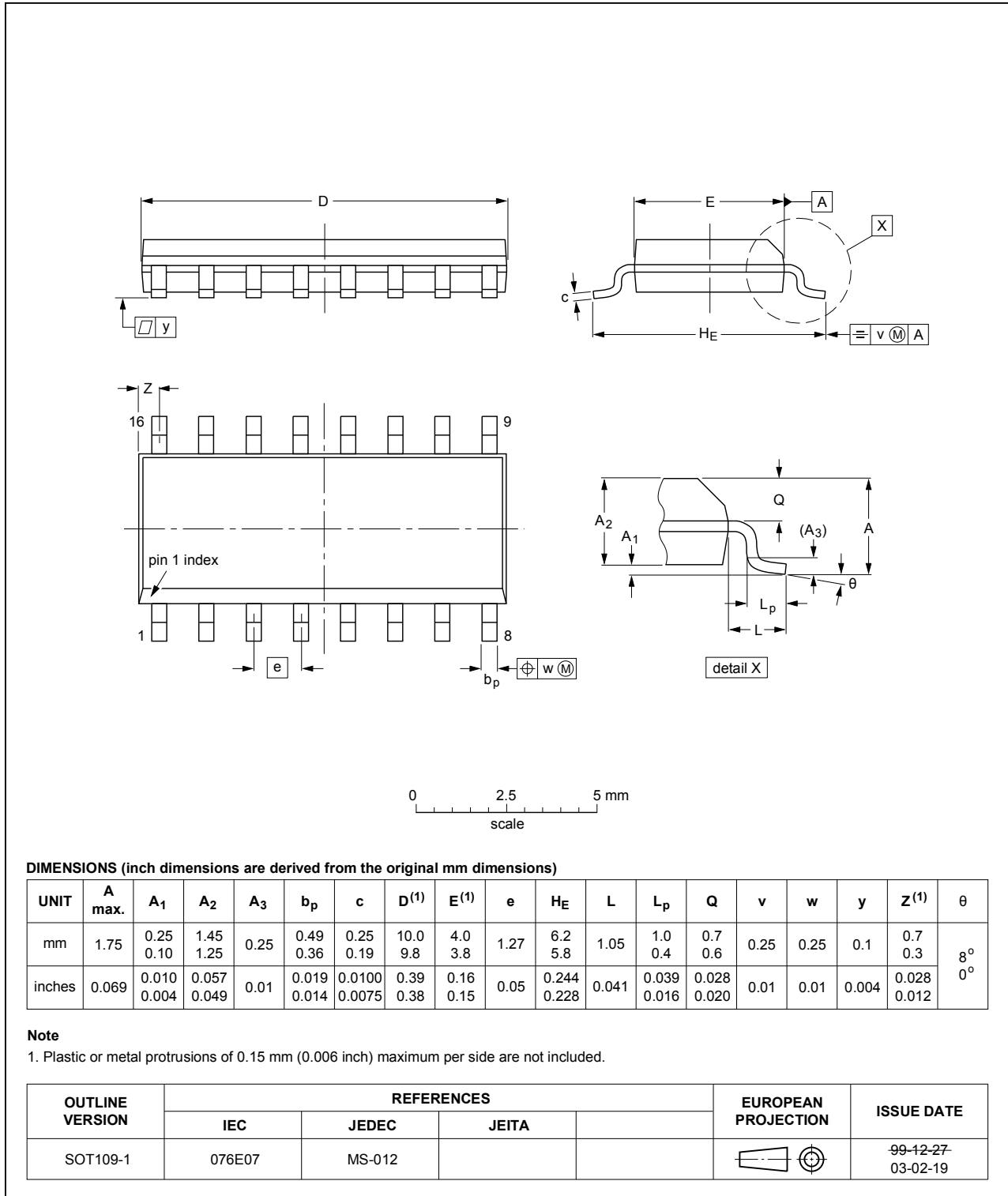


Fig. 10. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

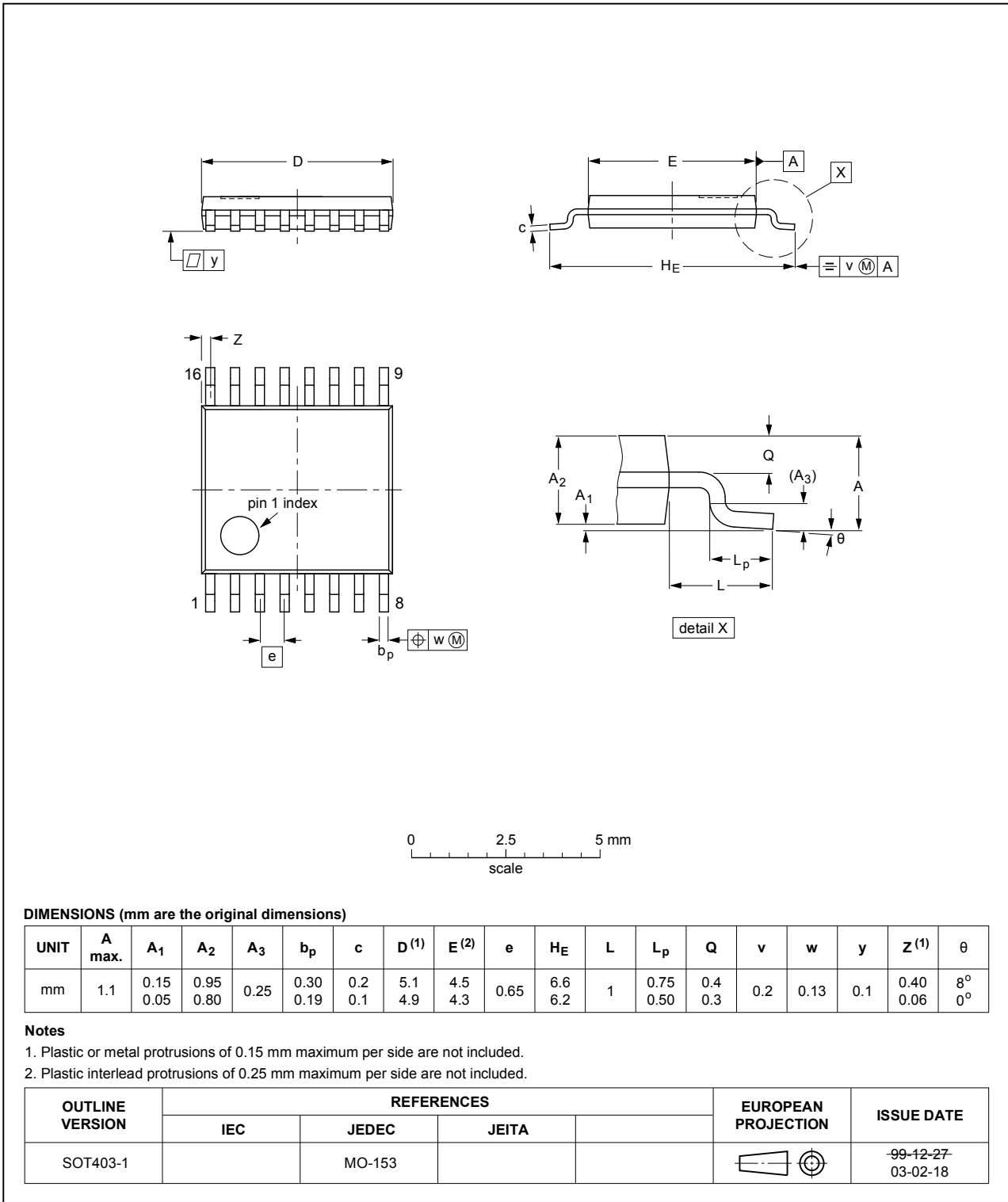


Fig. 11. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

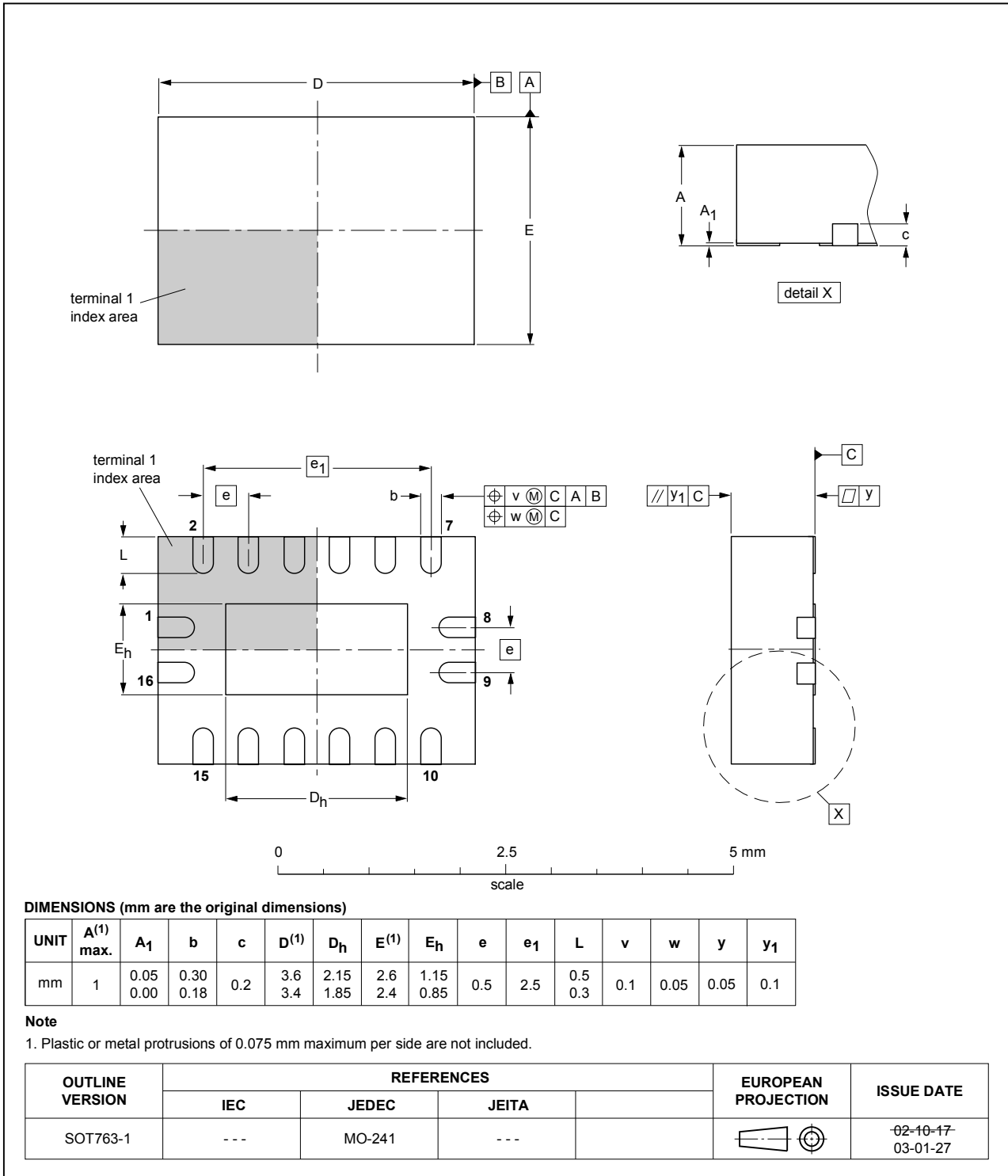


Fig. 12. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC138A_Q100 v.2	20190123	Product data sheet	-	74LVC138A_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74LVC138A_Q100 v.1	20130404	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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