74LVT16244B; 74LVTH16244B

3.3 V 16-bit buffer/driver; 3-state

Rev. 12 — 19 October 2018 Product data sheet

1. General description

The 74LVT16244B; 74LVTH16244B is a high-performance BiCMOS product designed for V_{CC} operation at 3.3 V.

This device is a 16-bit buffer and line driver featuring non-inverting 3-state bus outputs. The device can be used as four 4-bit buffers, two 8-bit buffers, or one 16-bit buffer.

2. Features and benefits

- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus hold data inputs eliminate need for external pull-up resistors to hold unused inputs
- Power-up 3-state
- Live insertion and extraction permitted
- No bus current loading when output is tied to 5 V bus
- Latch-up protection
  - JESD78B Class II exceeds 500 mA
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16244BDL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74LVTH16244BDL				
74LVT16244BDGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74LVTH16244BDGG				

4. Functional diagram

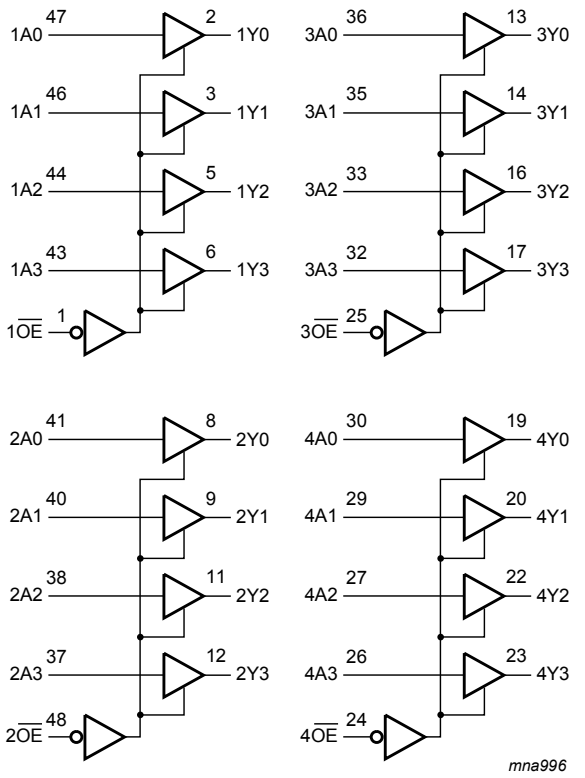


Fig. 1. Logic symbol

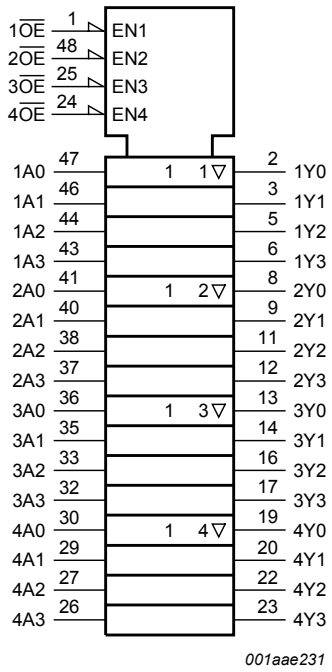


Fig. 2. IEC logic symbol

5. Pinning information

5.1. Pinning

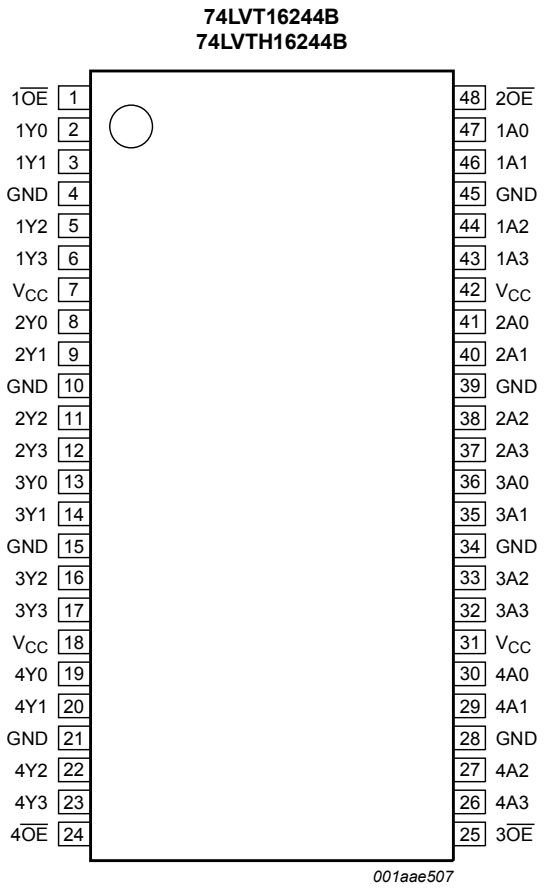


Fig. 3. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$,$3\overline{OE}$, $4\overline{OE}$	1, 48, 25, 24	output enable input (active LOW)
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data output
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data output
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data output
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data input
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data input
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data input
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data input

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Control	Input	Output
$n\overline{OE}$	**nAn**	**nYn**
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+4.6	V
V_I	input voltage		[1]	-0.5	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state	[1]	-0.5	+7.0	V
I_{IK}	input clamping current	V_I < 0 V		-50	-	mA
I_{OK}	output clamping current	V_O < 0 V		-50	-	mA
I_O	output current	output in LOW-state		-	128	mA
		output in HIGH-state		-64	-	mA
T_{stg}	storage temperature			-65	+150	°C
T_j	junction temperature		[2]	-	150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C;	[3]	-	500	mW

[1] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.
[3] Above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.7	-	3.6	V
V_I	input voltage		0	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-32	-	-	mA
I_{OL}	LOW-level output current	none	-	-	32	mA
		current duty cycle ≤ 50 %; f_i ≥ 1 kHz	-	-	64	mA
T_{amb}	ambient temperature	in free-air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	outputs enabled	-	-	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +85 °C.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V_{IK}	input clamping voltage	V_{CC} = 2.7 V; I_{IK} = -18 mA	-1.2	-0.85	-	V
V_{OH}	HIGH-level output voltage	I_{OH} = -100 µA; V_{CC} = 2.7 V to 3.6 V	V_{CC} - 0.2	V_{CC}	-	V
		I_{OH} = -8 mA; V_{CC} = 2.7 V	2.4	2.5	-	V
		I_{OH} = -32 mA; V_{CC} = 3.0 V	2.0	2.3	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 2.7 V				
		I_{OL} = 100 µA	-	0.07	0.2	V
		I_{OL} = 24 mA	-	0.3	0.5	V
		V_{CC} = 3.0 V				
		I_{OL} = 16 mA	-	0.25	0.4	V
		I_{OL} = 32 mA	-	0.3	0.5	V
		I_{OL} = 64 mA	-	0.4	0.55	V
I_I	input leakage current	all input pins; V_{CC} = 0 V or 3.6 V; V_I = 5.5 V	-	0.1	10	µA
		control pins; V_{CC} = 3.6 V; V_I = V_{CC} or GND	-	0.1	±1.0	µA
		data pins; V_{CC} = 3.6 V [2]				
		V_I = V_{CC}	-	0.1	1	µA
		V_I = 0 V	-5	-0.1	-	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or V_O = 0 V to 4.5 V	-	0.1	±100	µA
I_{BHL}	bus hold LOW current	V_{CC} = 3 V; V_I = 0.8 V [3]	75	135	-	µA
I_{BHH}	bus hold HIGH current	V_{CC} = 3 V; V_I = 2.0 V	-	-135	-75	µA
I_{BHLO}	bus hold LOW overdrive current	nAn input; V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	500	-	-	µA
I_{BHHO}	bus hold HIGH overdrive current	nAn input; V_{CC} = 0 V to 3.6 V; V_I = 3.6 V	-	-	-500	µA
I_{LO}	output leakage current	output in HIGH-state when V_O > V_{CC}; V_O = 5.5 V; V_{CC} = 3.0 V	-	50	125	µA
$I_{O(pu/pd)}$	power-up/ power-down output current	V_{CC} ≤ 1.2 V; V_O = 0.5 V to V_{CC}; V_I = GND or V_{CC}; $n\overline{OE}$ = don't care [4]	-	1	±100	µA
I_{OZ}	OFF-state output current	V_{CC} = 3.6 V; V_I = V_{IH} or V_{IL}				
		output HIGH: V_O = 3.0 V	-	0.5	5	µA
		output LOW: V_O = 0.5 V	-5	+0.5	-	µA
I_{CC}	supply current	V_{CC} = 3.6 V; V_I = GND or V_{CC}; I_O = 0 A				
		output HIGH	-	0.07	0.12	mA
		output LOW	-	4.0	6.0	mA
		outputs disabled [5]	-	0.07	0.12	mA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 3.0 V to 3.6 V; one input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND [6]	-	0.1	0.2	mA

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
C_I	input capacitance	V_I = 0 V or 3.0 V	-	3	-	pF
C_O	output capacitance	outputs disabled; V_O = 0 V or 3.0 V	-	9	-	pF

[1] Typical values are measured at V_{CC} = 3.3 V and at T_{amb} = 25 °C.
[2] Unused pins at V_{CC} or GND.
[3] This is the bus hold overdrive current required to force the input to the opposite logic state.
[4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms. From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 µs is permitted. This parameter is valid for T_{amb} = 25 °C only.
[5] I_{CC} is measured with outputs pulled to V_{CC} or GND.
[6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.

10. Dynamic characteristics

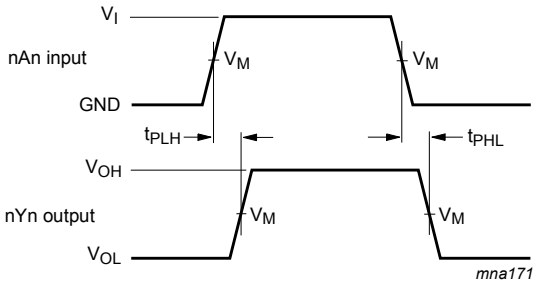
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); T_{amb} = -40 °C to +85 °C; for test circuit see Fig. 6.

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
t_{PLH}	LOW to HIGH propagation delay	nAn to nYn; see Fig. 4				
		V_{CC} = 2.7 V	-	-	4.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	1.8	3.2	ns
t_{PHL}	HIGH to LOW propagation delay	nAn to nYn; see Fig. 4				
		V_{CC} = 2.7 V	-	-	4.0	ns
		V_{CC} = 3.0 V to 3.6 V	0.5	1.7	3.2	ns
t_{PZH}	OFF-state to HIGH propagation delay	$n\overline{OE}$ to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns
t_{PZL}	OFF-state to LOW propagation delay	$n\overline{OE}$ to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.3	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.1	4.0	ns
t_{PHZ}	HIGH to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	5.0	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	3.2	4.5	ns
t_{PLZ}	LOW to OFF-state propagation delay	$n\overline{OE}$ to nYn; see Fig. 5				
		V_{CC} = 2.7 V	-	-	4.4	ns
		V_{CC} = 3.0 V to 3.6 V	1.0	2.9	4.0	ns

[1] Typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

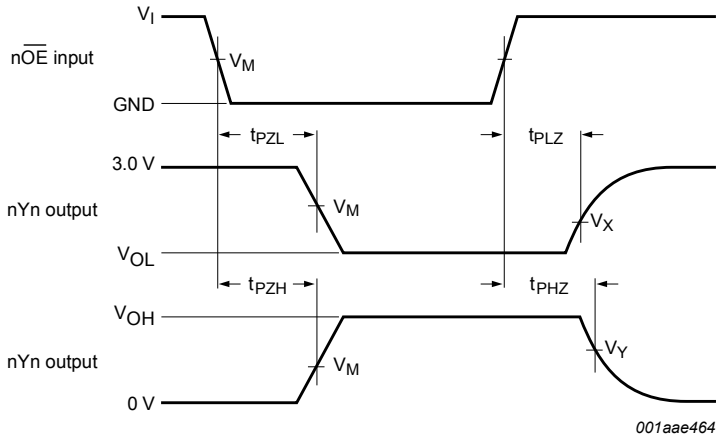
10.1. Waveforms and test circuit



Measurements points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 4. Propagation delay input (nAn) to output (nYn)



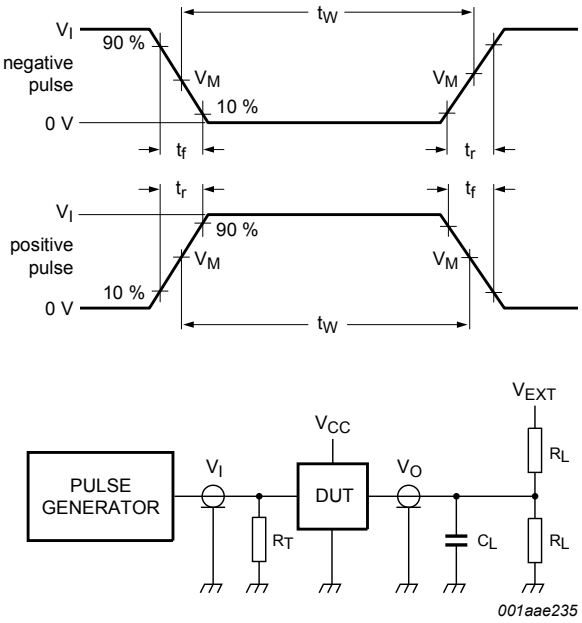
Measurements points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. 3-state output enable and disable times

Table 8. Measurement points

Input	Output		
V_M	V_M	V_X	V_Y
1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 9.

Definitions test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

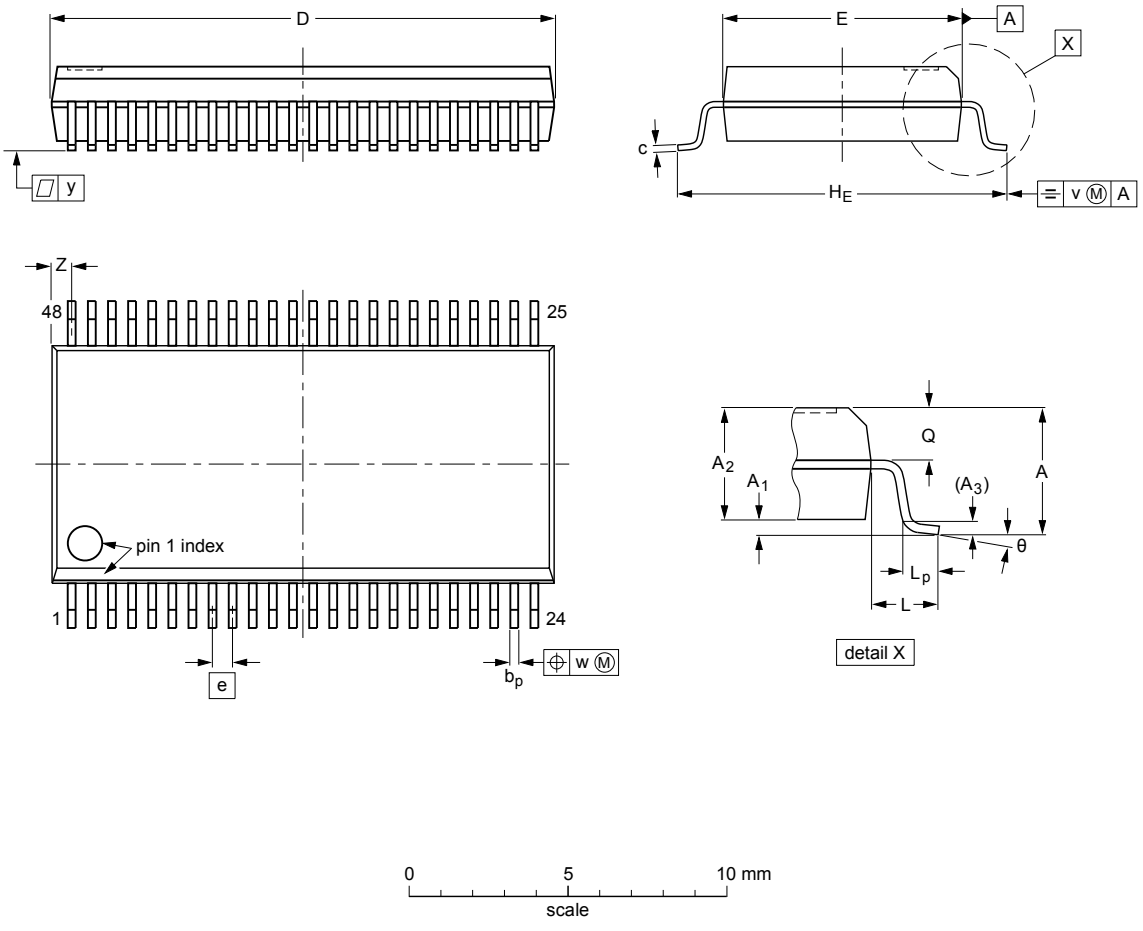
Fig. 6. Test circuit for measuring switching times

Table 9. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHZ}, t_{PZH}	t_{PLZ}, t_{PZL}	t_{PLH}, t_{PHL}
2.7 V	≤ 10 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	GND	6 V	open

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm **SOT370-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

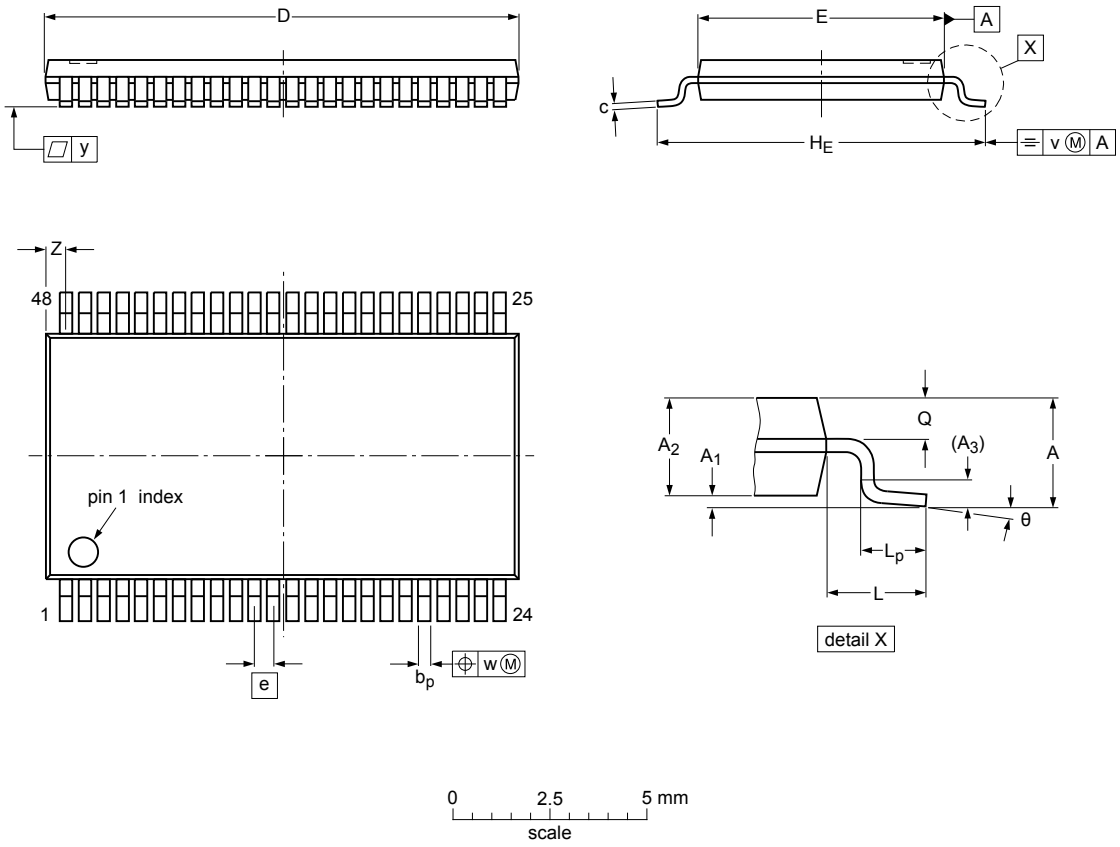
Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				~~99-12-27~~ 03-02-19

Fig. 7. Package outline SOT370-1 (SSOP48)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm **SOT362-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	Z	θ
mm	max	1.2	0.15	1.05	0.25	0.28	0.2	12.6	6.2	0.5	8.3	1	0.8	0.50	0.25	0.08	0.1	0.8	8°
	nom																		
	min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				~~03-02-19~~ 13-08-05

Fig. 8. Package outline SOT362-1 (TSSOP48)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVT_LVTH16244B v.12	20181019	Product data sheet	-	74LVT_LVTH16244B v.11
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type numbers 74LVT16244BEV (SOT702-1), 74LVT16244BBX (SOT1134-2) and 74LVTH16244BBX (SOT1134-2) removed. • Package outline drawing SOT362-1 updated			
74LVT_LVTH16244B v.11	20120301	Product data sheet	-	74LVT_LVTH16244B v.10
Modifications:	• For type number 74LVT16244BBX and 74LVTH16244BBX the sot code has changed to SOT1134-2.			
74LVT_LVTH16244B v.10	20111122	Product data sheet	-	74LVT_LVTH16244B v.9
Modifications:	• Legal pages updated.			
74LVT_LVTH16244B v.9	20110620	Product data sheet	-	74LVT_LVTH16244B v.8
74LVT_LVTH16244B v.8	20100322	Product data sheet	-	74LVT_LVTH16244B v.7
74LVT_LVTH16244B v.7	20090326	Product data sheet	-	74LVT_LVTH16244B v.6
74LVT_LVTH16244B v.6	20081113	Product data sheet	-	74LVT_LVTH16244B v.5
74LVT_LVTH16244B v.5	20060321	Product data sheet	-	74LVT16244B v.4
74LVT16244B v.4	20021031	Product specification	-	74LVT16244B v.3
74LVT16244B v.3	19981007	Product specification	-	74LVT16244B v.2
74LVT16244B v.2	19980219	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 19 October 2018

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