74ABT74

Dual D-type flip-flop with set and reset; positive edge-trigger

Rev. 4 — 23 January 2024 Product data sheet

1. General description

The 74ABT74 is a dual positive edge triggered D-type flip-flop with individual data (D), clock (CP), set ($\overline{SD}$) and reset ($\overline{RD}$) inputs, and complementary Q and $\overline{Q}$ outputs. Data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. This device is fully specified for partial power down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 4.5 V to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 500 mA per JESD78B class II level A
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ABT74D	-40 °C to +85 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74ABT74PW	-40 °C to +85 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4. Functional diagram

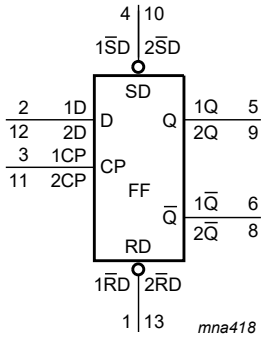


Fig. 1. Logic symbol

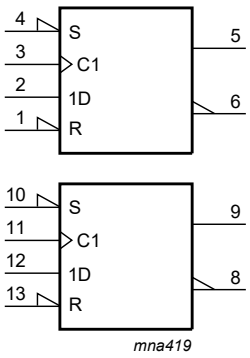


Fig. 2. IEC logic symbol

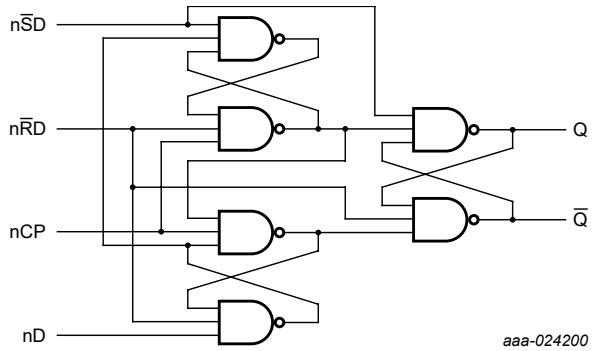


Fig. 3. Logic diagram for one flip-flop

5. Pinning information

5.1. Pinning

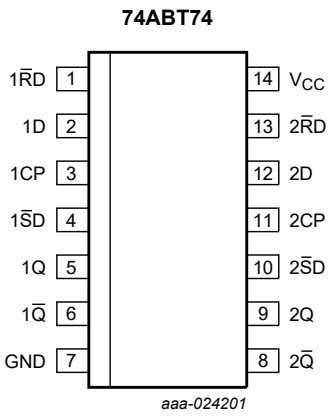


Fig. 4. Pin configuration SOT108-1 (SO14)

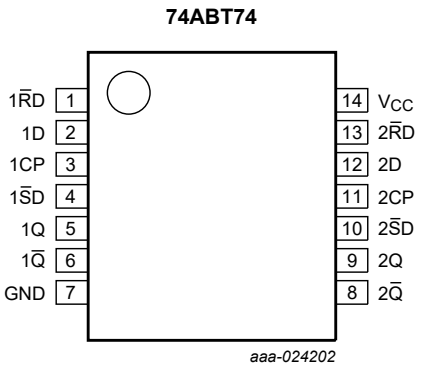


Fig. 5. Pin configuration SOT402-1 (TSSOP14)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1$\overline{RD}$, 2$\overline{RD}$	1, 13	asynchronous reset-direct input (active LOW)
1D, 2D	2, 12	data input
1CP, 2CP	3, 11	clock input (LOW-to-HIGH, edge-triggered)
1$\overline{SD}$, 2$\overline{SD}$	4, 10	asynchronous set-direct input (active LOW)
1Q, 2Q	5, 9	output
1$\overline{Q}$, 2$\overline{Q}$	6, 8	complement output
GND	7	ground (0 V)
V_{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; h = HIGH voltage level one setup time prior to low-to-high clock transition
L = LOW voltage level; l = LOW voltage level one setup time prior to low-to-high clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

Input				Output		Operating mode
n$\overline{SD}$	n$\overline{RD}$	nCP	nD	nQ	n$\overline{Q}$	
L	H	X	X	H	L	Asynchronous set
H	L	X	X	L	H	Asynchronous reset
L	L	X	X	H	H	Undetermined [1]
H	H	↑	h	H	L	Load "1"
H	H	↑	l	L	H	Load "0"

[1] This setup is unstable and changes when either set or reset returns to the high level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-1.2	+7.0	V
V_O	output voltage	output in OFF-state or HIGH-state [1]	-0.5	+5.5	V
I_{IK}	input clamping current	$V_I < 0$ V	-18	-	mA
I_{OK}	output clamping current	$V_O < 0$ V	-50	-	mA
I_O	output current	output in LOW-state	-	40	mA
T_j	junction temperature		-	150	°C
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8. Recommended operating conditions

Table 5. Operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_I	input voltage		0	-	V_{CC}	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
I_{OH}	HIGH-level output current		-15	-	-	mA
I_{OL}	LOW-level output current		-	-	20	mA
$\Delta t/\Delta V$	input transition rise and fall rate		0	-	10	ns/V
T_{amb}	ambient temperature	in free air	-40	-	+85	°C

9. Static characteristics

Table 6. Static characteristics

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_{IK} = -18 mA	-1.2	-0.9	-	-1.2	-	V
V_{OH}	HIGH-level output voltage	V_{CC} = 4.5 V; I_{OH} = -15 mA; $V_I = V_{IL}$ or V_{IH}	2.5	2.9	-	2.5	-	V
V_{OL}	LOW-level output voltage	V_{CC} = 4.5 V; I_{OL} = 20 mA; $V_I = V_{IL}$ or V_{IH}	-	0.35	0.5	-	0.5	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	±0.01	±1.0	-	±1.0	µA
I_{OFF}	power-off leakage current	V_{CC} = 0 V; V_I or $V_O \leq$ 4.5 V	-	±5.0	±100	-	±100	µA
I_{CEX}	output high leakage current	HIGH-state; V_O = 5.5 V; V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	5.0	50	-	50	µA
I_O	output current	V_{CC} = 5.5 V; V_O = 2.5 V [1]	-50	-75	-180	-50	-180	mA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = GND or V_{CC}	-	2	50	-	50	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V; other inputs at V_{CC} or GND [2]	-	0.25	500	-	500	µA
C_I	input capacitance	V_I = 0 V or V_{CC}	-	3	-	-	-	pF

[1] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
[2] This is the increase in supply current for each input at 3.4 V.

10. Dynamic characteristics

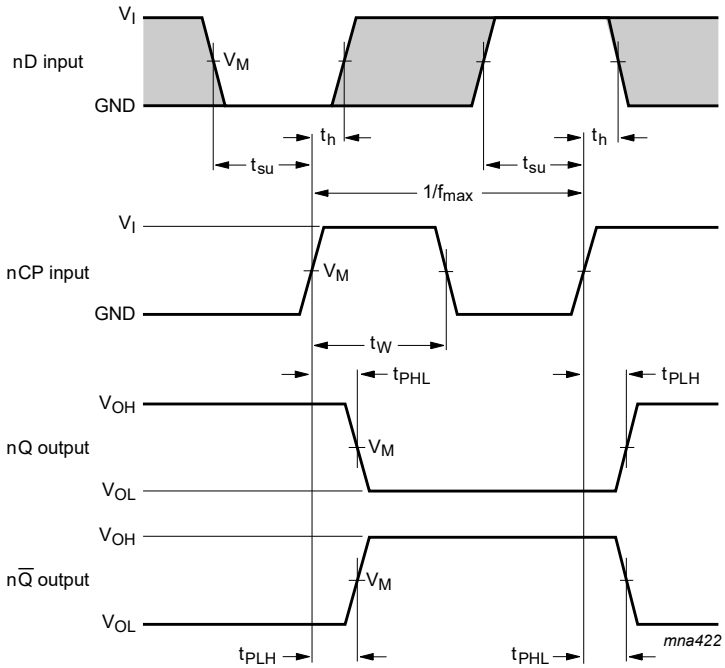
Table 7. Dynamic characteristics

GND = 0 V; for test circuit, see Fig. 9.

Symbol	Parameter	Conditions	25 °C; V_{CC} = 5.0 V			-40 °C to +85 °C; V_{CC} = 5.0 V ± 0.5 V		Unit
			Min	Typ	Max	Min	Max	
f_{max}	maximum frequency	nCP; see Fig. 6	180	250	-	150	-	MHz
t_{PLH}	LOW to HIGH propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 6	1.0	3.0	4.2	1.0	4.7	ns
t_{PHL}	HIGH to LOW propagation delay	nCP to nQ, n$\overline{Q}$; see Fig. 6	1.0	2.5	3.5	1.0	4.0	ns
t_{PLH}	LOW to HIGH propagation delay	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 7	1.0	3.4	4.9	1.0	6.2	ns
t_{PHL}	HIGH to LOW propagation delay	n$\overline{SD}$, n$\overline{RD}$ to nQ, n$\overline{Q}$; see Fig. 7	1.0	2.9	4.5	1.0	5.2	ns
$t_{sk(o)}$	output skew time	[1]	-	0.5	0.6	-	0.6	ns
t_{su}	set-up time	nD to nCP HIGH; see Fig. 6	2.6	1.4	-	2.6	-	ns
		nD to nCP LOW; see Fig. 6	2.4	1.4	-	2.4	-	ns
t_h	hold time	nD to nCP HIGH or LOW; see Fig. 6	0	-1.4	-	0	-	ns
t_W	pulse width	nCP HIGH or LOW; see Fig. 6	1.7	1.0	-	2.1	-	ns
		n$\overline{SD}$, n$\overline{RD}$ LOW; see Fig. 7	2.0	1.3	-	2.2	-	ns
t_{rec}	recovery time	n$\overline{SD}$, n$\overline{RD}$ to nCP; see Fig. 8	2.1	1.4	-	2.4	-	ns

[1] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

10.1. Waveforms and test circuit

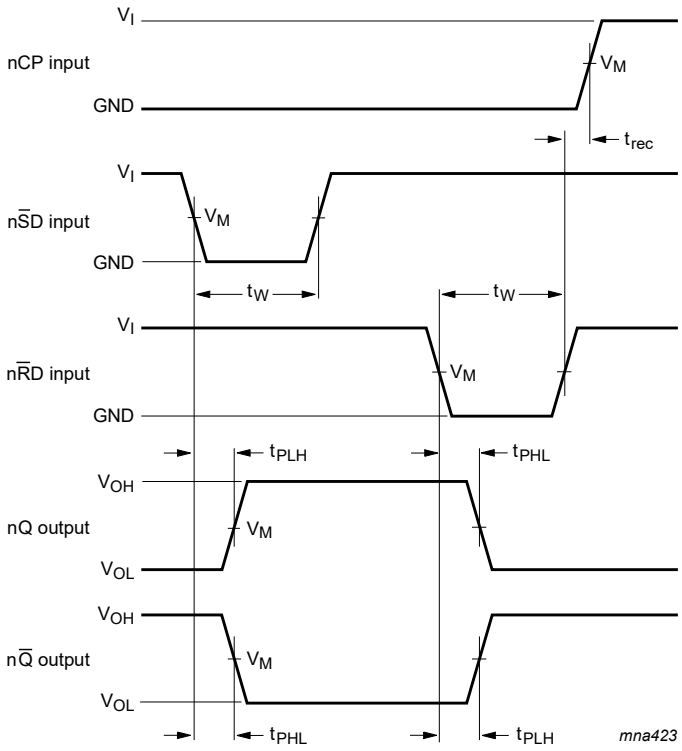


V_M = 1.5 V

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

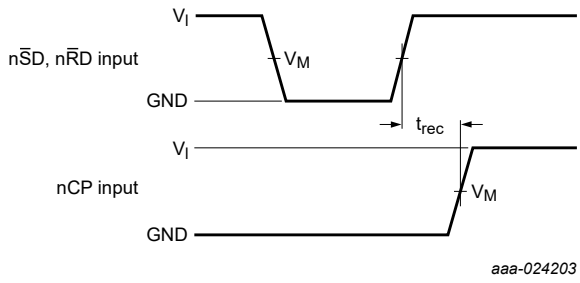
Fig. 6. Propagation delay clock input (nCP) to output (nQ, n$\overline{Q}$), set-up and hold times data input (nD) to clock input, clock pulse width and maximum clock (nCP) frequency



V_M = 1.5 V

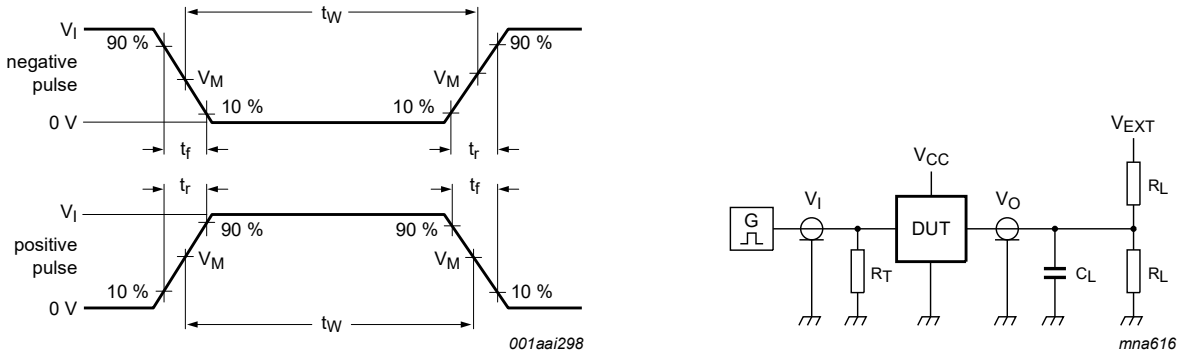
V_{OL} and V_{OH} are typical output voltage levels that occur with the output load

Fig. 7. Propagation delay set (nSD) and reset (nSD) input to output (nQ, nQ), and set (nSD) and reset nRD pulse width.



V_M = 1.5 V

Fig. 8. Recovery time set (nSD) and reset (nRD) to nCP



a. Input pulse definition

b. Test circuit

Test data is given in Table 8.

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

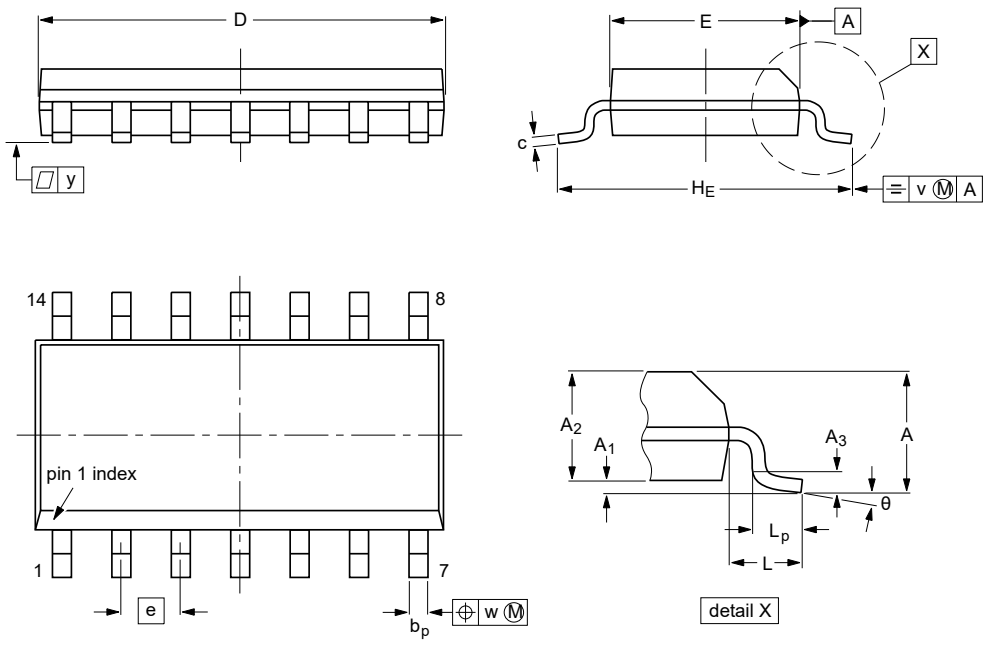
Fig. 9. Test circuit for measuring switching times

Table 8. Test data

Input				Load		V_{EXT}		
V_I	f_i	t_W	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
3.0 V	1 MHz	500 ns	≤ 2.5 ns	50 pF	500 Ω	open	open	7.0 V

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	8.75	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	8.55	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.344	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.337	0.15		0.228		0.016				0°

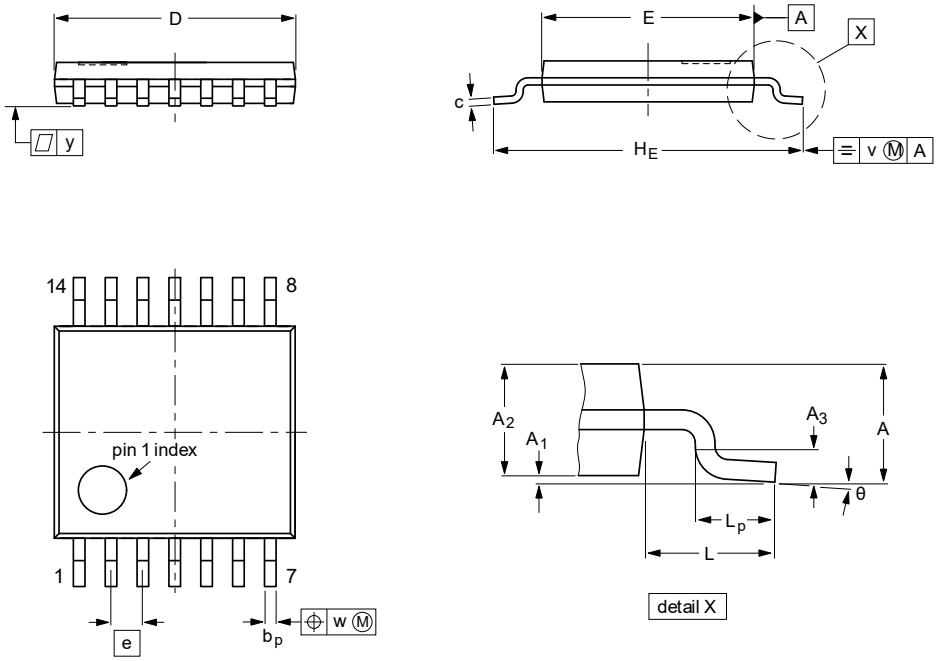
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot108-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT108-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot402-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 11. Package outline SOT402-1 (TSSOP14)

12. Abbreviations

Table 9. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ABT74A v.4	20240123	Product data sheet	-	74ABT74A v.3
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 10, Fig. 11: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74ABT74A v.3	20201012	Product data sheet	-	74ABT74A v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Type number 74ABT74DB (SOT337-1 / SSOP14) removed.			
74ABT74A v.2	20160812	Product data sheet	-	74ABT74A v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate.			
74ABT74A v.1	19950922	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 23 January 2024

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