

74HC109; 74HCT109 Dual JK flip-flop with set and reset; positive-edge-trigger Rev. 6 — 21 February 2024 Product data sheet

1. General description

The 74HC109; 74HCT109 is a dual positive edge triggered JK flip-flop featuring individual J and K inputs, clock (CP) inputs, set (SD) and reset (RD) inputs and complementary Q and \overline{Q} outputs. The set and reset are asynchronous active LOW inputs and operate independently of the clock input. The J and \overline{K} inputs control the state changes of the flip-flops as described in the mode select function table. The J and K inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. The JK design allows operation as a D-type flip-flop by connecting the J and \overline{K} inputs together. This device features reduced input threshold levels to allow interfacing to TTL logic levels. Inputs also include clamp diodes, this enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times

2. Features and benefits

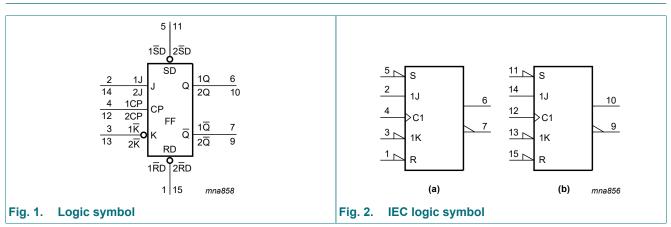
- J and K inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Wide supply voltage range:
 - For 74HC109: from 2.0 V to 6.0 V
 - For 74HCT109: from 4.5 V to 5.5 V •
- CMOS low power dissipation
- High noise immunity
- Input levels:
 - For 74HC109: CMOS level
 - For 74HCT109: TTL level
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- 74HC109 complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- 74HCT109 complies with JEDEC standard JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

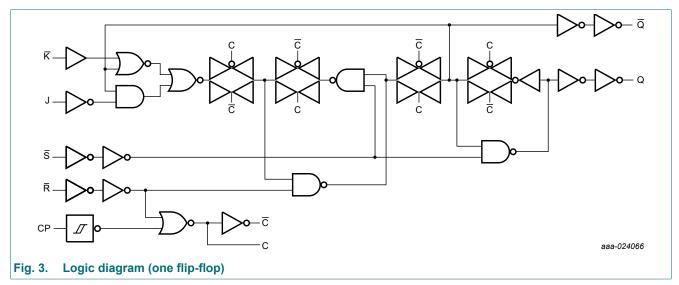
3. Ordering information

Table 1. Ordering	information									
Type number Package										
	Temperature range	Name	Description	Version						
74HC109D 74HCT109D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	<u>SOT109-1</u>						
74HC109PW 74HCT109PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	<u>SOT403-1</u>						



4. Functional diagram





5. Pinning information

5.1. Pinning

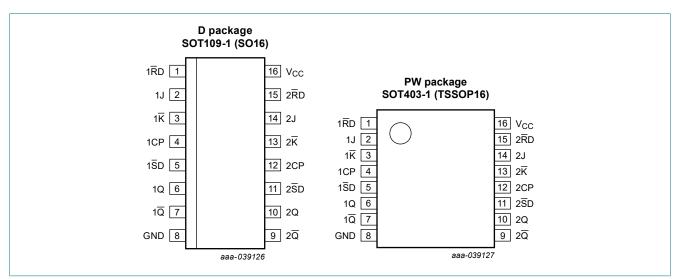


Table 2. Pin descripti	on	
Symbol	Pin	Description
1RD, 2RD	1, 15	asynchronous reset input (active LOW)
1J, 2J	2, 14	synchronous input
1 K , 2 K	3, 13	synchronous input
1CP, 2CP	4, 12	clock input (LOW-to-HIGH; edge-triggered)
1 S D, 2 S D	5, 11	asynchronous set input (active LOW)
1Q, 2Q	6, 10	true flip-flop output
1 <u>Q</u> , 2 <u>Q</u>	7, 9	complement flip-flop output
GND	8	ground (0 V)
V _{CC}	16	supply voltage

5.2. Pin description

6. Functional description

Table 3. Function selection

H = HIGH voltage level; h = HIGH voltage level one set-up time before the LOW-to-HIGH CP transition;

L = LOW voltage level; I = LOW voltage level one set-up time before the LOW-to-HIGH CP transition;

q = lower case letters indicate the state of the referenced output one set-up time before the LOW-to-HIGH CP transition;

 $X = don't care; \uparrow = LOW-to-HIGH CP transition$

Operating modes	Input					Output	
	nSD	nRD	nCP	nJ	nK	nQ	nQ
Asynchronous set	L	Н	Х	Х	Х	Н	L
Asynchronous reset	Н	L	Х	Х	Х	L	Н
Undetermined	L	L	Х	Х	Х	Н	Н
Toggle	Н	Н	1	h	I	q	q
Load 0 (reset)	Н	Н	1	I	I	L	Н
Load 1 (set)	Н	Н	1	h	h	Н	L
Hold no change	Н	Н	1	I	h	q	q

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	$V_{\rm I}$ < -0.5 V or $V_{\rm I}$ > $V_{\rm CC}$ + 0.5 V	-	±20	mA
I _{OK}	output clamping current	$V_{\rm O}$ < -0.5 V or $V_{\rm O}$ > $V_{\rm CC}$ + 0.5 V	-	±20	mA
I _O	output current	$-0.5 V < V_O < V_{CC} + 0.5 V$	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	[1]	-	500	mW

 For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C. For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions		74HC109)		Unit		
			Min	Тур	Max	Min	Тур	Max	1
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
VI	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
Vo	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Мах	Min	Мах	Min	Max	1
74HC10	9									
VIH	HIGH-level	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
	input voltage	V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
	input voltage	V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}$								
	output voltage	I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	4.0	-	40	-	80	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions		25 °C			°C to 5 °C		°C to 5 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
74HCT1	09		I					I		
V _{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I _O = -20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level	$V_{I} = V_{IH} \text{ or } V_{IL}; V_{CC} = 4.5 \text{ V}$								
	output voltage	I_0 = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 5.2 mA; V _{CC} = 5.5 V	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	$V_{I} = V_{CC}$ or GND; $V_{CC} = 5.5$ V	-	-	±0.1	-	±1	-	±1	μA
I _{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 5.5$ V	-	-	4.0	-	40	-	80	μA
ΔI _{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1 V$; other inputs at V_{CC} or GND; $V_{CC} = 4.5 V$ to 5.5 V								
		nJ, nK, nSD, nRD and nCP inputs	-	35	126	-	157.5	-	171.5	μA
CI	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 6.

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	1
74HC10	9	<u> </u>								
t _{pd}	propagation	nCP to nQ, $n\overline{Q}$; see <u>Fig. 4</u> [2]								
	delay	V _{CC} = 2.0 V	-	50	175	-	220	-	265	ns
		V _{CC} = 4.5 V	-	18	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	30	-	37	-	45	ns
t _{PLH}	LOW to HIGH	n S D to nQ, see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 2.0 V	-	30	120	-	150	-	180	ns
	delay	V _{CC} = 4.5 V	-	11	24	-	30	-	36	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	9	20	-	26	-	31	ns

Dual JK flip-flop with set and	d reset; positive-edge-trigger
--------------------------------	--------------------------------

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Мах	Min	Max	1
t _{PHL}	HIGH to LOW	nSD to nQ; see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 2.0 V	-	41	155	-	195	-	235	ns
	uelay	V _{CC} = 4.5 V	-	15	31	-	39	-	47	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	26	-	33	-	40	ns
t _{PHL}		nRD to nQ; see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 2.0 V	-	41	185	-	230	-	280	ns
	uelay	V _{CC} = 4.5 V	-	15	37	-	46	-	56	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	12	31	-	39	-	48	ns
t _{PLH}		nRD to nQ; see <u>Fig. 5</u>								
	propagation	V _{CC} = 2.0 V	-	39	170	-	215	-	255	ns
	delay	V _{CC} = 4.5 V	-	14	34	-	43	-	51	ns
		V _{CC} = 5 V; C _L = 15 pF	-	12	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	11	29	-	37	-	43	ns
t _t	transition time	nQ, nQ; see <u>Fig. 4</u> [3]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _W	pulse width	nCP HIGH or LOW; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	80	19	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
		nSD, nRD HIGH or LOW; see <u>Fig. 5</u>								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
t _{rec}	recovery time	nSD, nRD to nCP; see <u>Fig. 5</u>								
		V _{CC} = 2.0 V	70	19	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	7	-	18	-	21	-	ns
		V _{CC} = 6.0 V	12	6	-	15	-	18	-	ns

6 / 15

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C t	o +125 °C	Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	nJ and nK to nCP; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	70	17	-	90	-	105	-	ns
		V _{CC} = 4.5 V	14	6	-	18	-	21	-	ns
		V _{CC} = 6.0 V	12	5	-	15	-	18	-	ns
t _h	hold time	nJ and nK to nCP; see <u>Fig. 4</u>								
		V _{CC} = 2.0 V	5	0	-	5	-	5	-	ns
		V _{CC} = 4.5 V	5	0	-	5	-	5	-	ns
		V _{CC} = 6.0 V	5	0	-	5	-	5	-	ns
f _{max}	maximum	nCP; see <u>Fig. 4</u>								
	frequency	V _{CC} = 2.0 V	6	22	-	5	-	4	-	MHz
		V _{CC} = 4.5 V	30	68	-	24	-	20	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	75	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	81	-	28	-	24	-	MHz
C _{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}; f = 1 \text{ MHz};$ [4] V ₁ = GND to V _{CC}	-	20	-	-	-	-	-	pF
74HCT1	09			1	I	I	1	1	1	-
t _{pd}	propagation	nCP to nQ, $n\overline{Q}$;see Fig. 4 [2]								
	delay	V _{CC} = 4.5 V	-	20	35	-	44	-	53	ns
		V _{CC} = 5 V; C _L = 15 pF	-	17	-	-		-	-	ns
t _{PLH}		n S D to nQ, see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 4.5 V	-	13	26	-	33	-	39	ns
	delay	V _{CC} = 5 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW	nSD to nQ; see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 4.5 V	-	19	35	-	44	-	53	ns
	uciay	V _{CC} = 5 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
t _{PHL}		nRD to nQ; see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 4.5 V	-	19	35	-	44	-	53	ns
	delay	V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _{PLH}		nRD to nQ; see <u>Fig. 5</u>								
	propagation delay	V _{CC} = 4.5 V	-	16	32	-	40	-	48	ns
	uciay	V _{CC} = 5 V; C _L = 15 pF	-	15	-	-	-	-	-	ns
t _t	transition time	nQ, n \overline{Q} ; V _{CC} = 4.5 V; [3] see <u>Fig. 4</u>	-	7	15	-	19	-	22	ns
t _W	pulse width	nCP HIGH or LOW; V _{CC} = 4.5 V; see <u>Fig. 4</u>	18	9	-	23	-	27	-	ns
		nSD, nRD HIGH or LOW; V _{CC} = 4.5 V; see <u>Fig. 5</u>	16	8	-	20	-	24	-	ns
t _{rec}	recovery time	nSD, nRD to nCP; V _{CC} = 4.5 V; see <u>Fig. 5</u>	16	8	-	20	-	24	-	ns

Dual JK flip-flop with set and reset; positive-edge-trigger

Symbol	Parameter	Conditions		25 °C		-40 °C t	o +85 °C	-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
t _{su}	set-up time	nJ and nK to nCP; V _{CC} = 4.5 V; see <u>Fig. 4</u>	18	8	-	23	-	27	-	ns
t _h	hold time	nJ and nK to nCP; V _{CC} = 4.5 V; see <u>Fig. 4</u>	3	-3	-	3	-	3	-	ns
f _{max}	maximum	nCP; see <u>Fig. 4</u>								
	frequency	V _{CC} = 4.5 V	27	55	-	22	-	18	-	MHz
		V _{CC} = 5 V; C _L = 15 pF	-	61	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	C _L = 50 pF; f = 1 MHz; [2 V ₁ = GND to V _{CC} - 1.5 V	·] -	22	-	-	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] t_t^i is the same as t_{THL} and t_{TLH} .

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

 $P_{D} = C_{PD} \times V_{CC}^{2} \times f_{i} \times N + \Sigma (C_{L} \times V_{CC}^{2} \times f_{o}) \text{ where:}$

f_i = input frequency in MHz;

 f_o = output frequency in MHz;

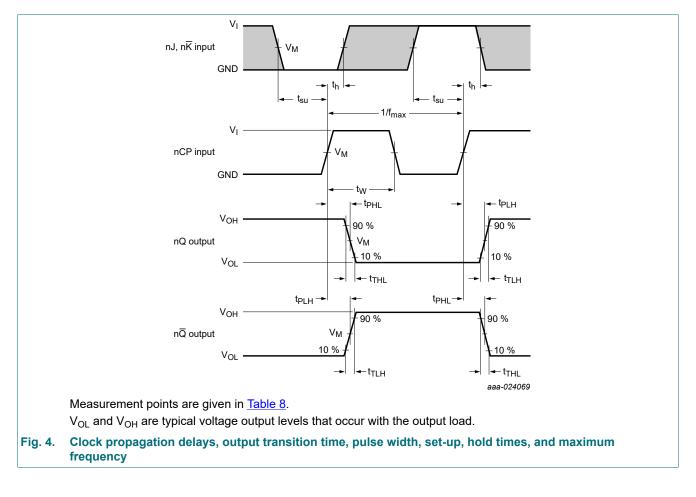
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

 $\Sigma(C_L \times V_{CC}^2 \times f_o) = \text{sum of outputs.}$

10.1. Waveforms and test circuit



74HC_HCT109

All information provided in this document is subject to legal disclaimers. Rev. 6 — 21 February 2024 © Nexperia B.V. 2024. All rights reserved

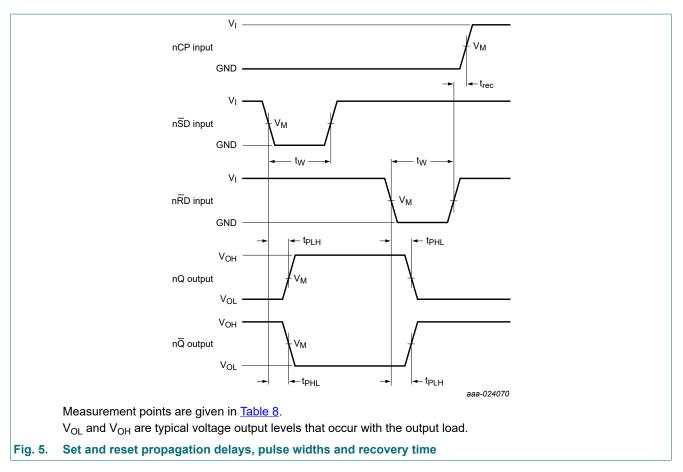
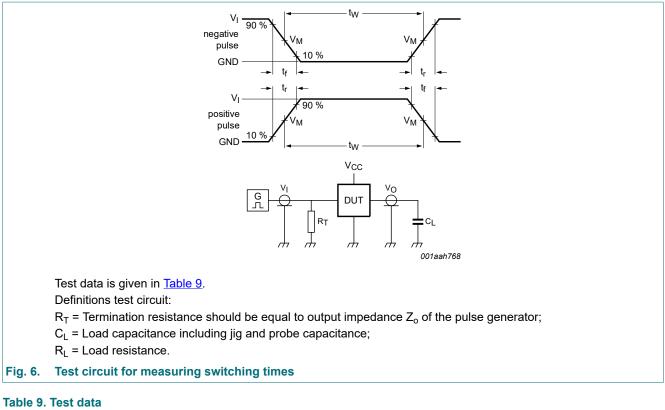


Table 8. Measurement points

Туре	Input	Output
	V _M	V _M
74HC109	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
74HCT109	1.3 V	1.3 V

Dual JK flip-flop with set and reset; positive-edge-trigger

Dual JK flip-flop with set and reset; positive-edge-trigger



Туре	Input		Load	Test
	VI	t _r , t _f	CL	
74HC109	V _{CC}	6 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}
74HCT109	3 V	6 ns	15 pF, 50 pF	t _{PLH} , t _{PHL}

11. Package outline

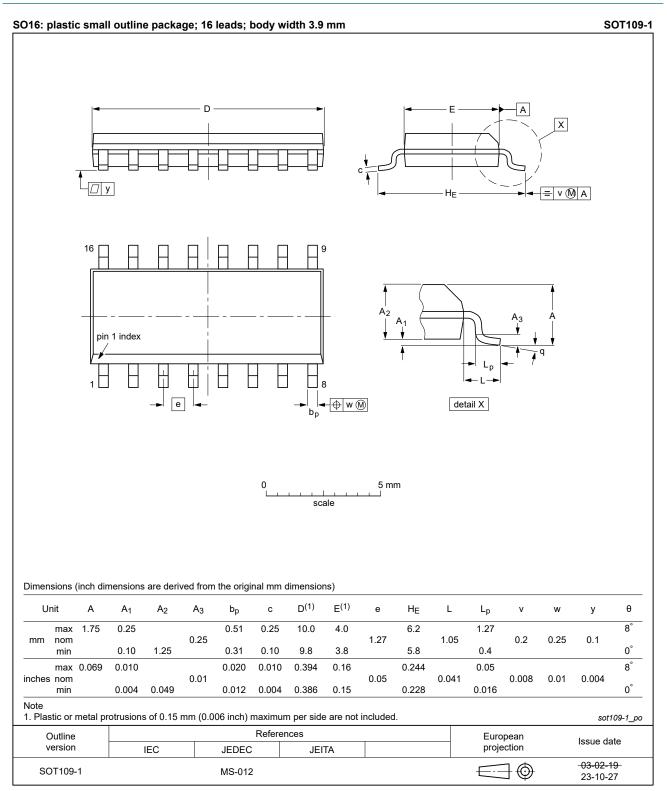


Fig. 7. Package outline SOT109-1 (SO16)

Dual JK flip-flop with set and reset; positive-edge-trigger

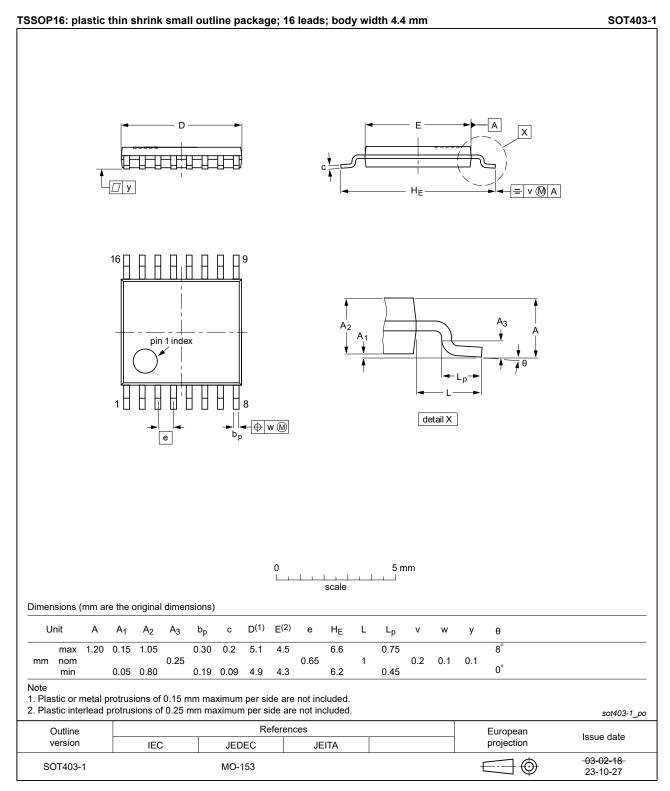


Fig. 8. Package outline SOT403-1 (TSSOP16)

12. Abbreviations

Table 10. Abbreviations		
Acronym	Description	
CDM	Charged Device Model	
CMOS	Complementary Metal Oxide Semiconductor	
DUT	Device Under Test	
ESD	ElectroStatic Discharge	
HBM	Human Body Model	
TTL	Transistor-Transistor Logic	

13. Revision history

Table 11. Revision history					
Document ID	Release date	Data sheet status	Change notice	Supersedes	
74HC_HCT109 v.6	20240221	Product data sheet	-	74HC_HCT109 v.5	
Modifications:		 Fig. 7, Fig. 8: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and 			
74HC_HCT109 v.5	20210805	Product data sheet	-	74HC_HCT109 v.4	
Modifications:	Type number	 Type number 74HC109PW (SOT403-1/TSSOP16) added. Type numbers 74HC109DB and 74HCT109DB (SOT338-1/SSOP16) removed. <u>Section 1</u> and <u>Section 2</u> updated. 			
74HC_HCT109 v.4	20200401	Product data sheet	-	74HC_HCT109 v.3	
Modifications:	guidelines c Legal texts	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. <u>Table 4</u>: Derating values for P_{tot} total power dissipation updated. 			
74HC_HCT109 v.3	20160801	Product data sheet	-	74HC_HCT109_CNV v.2	
Modifications:	guidelines o	 The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. 			
74HC_HCT109_CNV v.2	19971125	Product specification	-	-	

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

 Please consult the most recently issued document before initiating or completing a design.

- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <u>https://www.nexperia.com</u>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <u>http://www.nexperia.com/profile/terms</u>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Product data sheet

Rev. 6 — 21 February 2024

Contents

1. General description	1
2. Features and benefits	1
3. Ordering information	1
4. Functional diagram	2
5. Pinning information	2
5.1. Pinning	2
5.2. Pin description	3
6. Functional description	3
7. Limiting values	
8. Recommended operating conditions	4
9. Static characteristics	4
10. Dynamic characteristics	
10.1. Waveforms and test circuit	8
11. Package outline	11
12. Abbreviations	13
13. Revision history	13
14. Legal information	14

© Nexperia B.V. 2024. All rights reserved

For more information, please visit: http://www.nexperia.com For sales office addresses, please send an email to: salesaddresses@nexperia.com Date of release: 21 February 2024

74HC_HCT109

单击下面可查看定价,库存,交付和生命周期等信息

>>Nexperia(安世)