



# PESD2ETHX-Q

Ultra low capacitance double rail-to-rail ESD protection diode

3 May 2022

Product data sheet

## 1. General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT143B Surface-Mounted Device (SMD) plastic package.

The device is designed to protect two high-speed data lines or high-frequency signal lines from the damage caused by ESD and other transients.

The device integrates two ultra low capacitance rail-to-rail diodes and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

## 2. Features and benefits

- ESD protection of two high-speed data lines
- Ultra low capacitance:  $C_d = 1$  pF
- IEC 61000-4-2 up to 8 kV
- Very low reverse current
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- 100BASE-T1 / OPEN Alliance BroadR-Reach automotive Ethernet
- Low-Voltage Differential Signaling (LVDS) automotive
- USB 2.0 automotive

## 4. Quick reference data

Table 1. Quick reference data

| Symbol    | Parameter                | Conditions                                  |     | Min | Typ | Max | Unit |
|-----------|--------------------------|---|-----|-----|-----|-----|------|
| $V_{RWM}$ | reverse standoff voltage | $T_{amb} = 25$ °C                           |     | -   | -   | 5.5 | V    |
| $C_d$     | diode capacitance        | $f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C | [1] | -   | 1   | 1.5 | pF   |
|           |                          |   | [2] | -   | 0.6 | -   | pF   |
|           |                          |   | [3] | -   | 16  | -   | pF   |

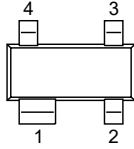
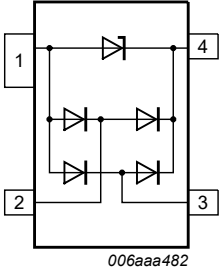
[1] Measured from pin 2 and 3 to ground.

[2] Measured from pin 2 to pin 3.

[3] Measured from pin 4 to ground.

## 5. Pinning information

Table 2. Pinning information

| Pin | Symbol          | Description    | Simplified outline  | Graphic symbol   |
|-----|-----------------|----------------|---|--|
| 1   | GND             | ground         |  <p><b>SOT143B</b></p> |  <p>006aaa482</p> |
| 2   | I/O 1           | input/output 1 |   |  |
| 3   | I/O 2           | input/output 2 |   |  |
| 4   | V <sub>CC</sub> | supply line    |   |  |

## 6. Ordering information

Table 3. Ordering information

| Type number | Package |  |         |
|-------------|---------|--|---------|
|             | Name    | Description  | Version |
| PESD2ETHX-Q | SOT143B | plastic, surface-mounted package; 4 leads; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body | SOT143B |

## 7. Marking

Table 4. Marking codes

| Type number | Marking code <sup>[1]</sup> |
|-------------|-----------------------------|
| PESD2ETHX-Q | 2B%                         |

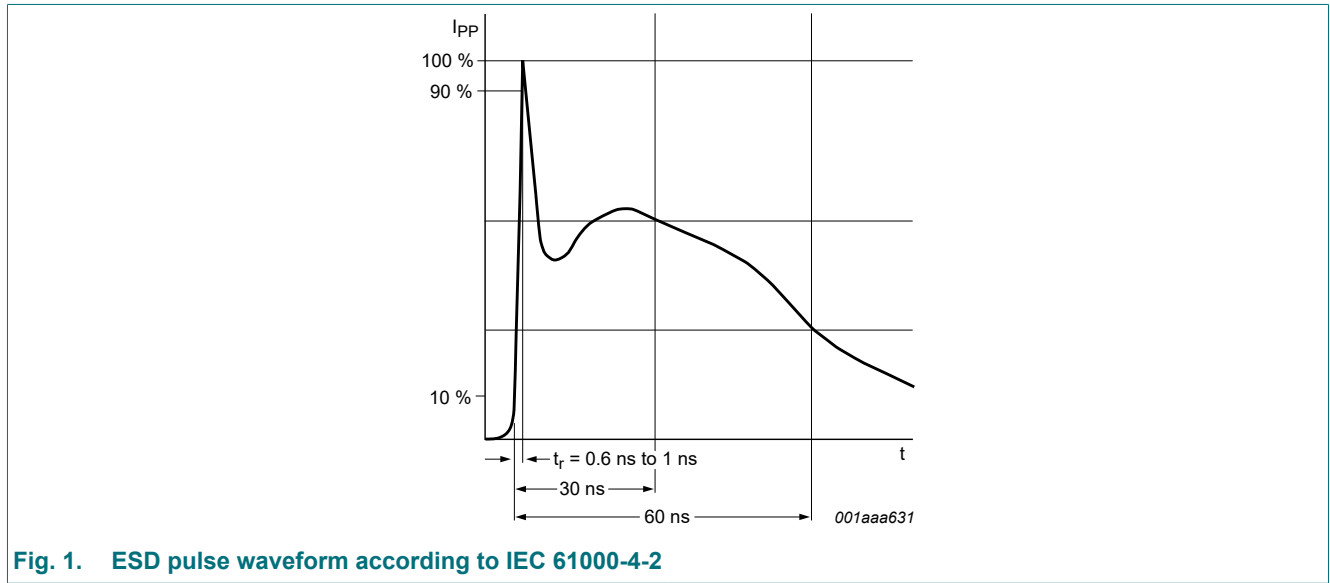
[1] % = placeholder for manufacturing site code

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol                     | Parameter                       | Conditions                                | Min | Max | Unit |
|----------------------------|---------------------------------|---|-----|-----|------|
| $T_{amb}$                  | ambient temperature             |   | -40 | 125 | °C   |
| $T_{stg}$                  | storage temperature             |   | -55 | 125 | °C   |
| <b>ESD maximum ratings</b> |                                 |   |     |     |      |
| $V_{ESD}$                  | electrostatic discharge voltage | IEC 61000-4-2; level 4; contact discharge | -   | 8   | kV   |



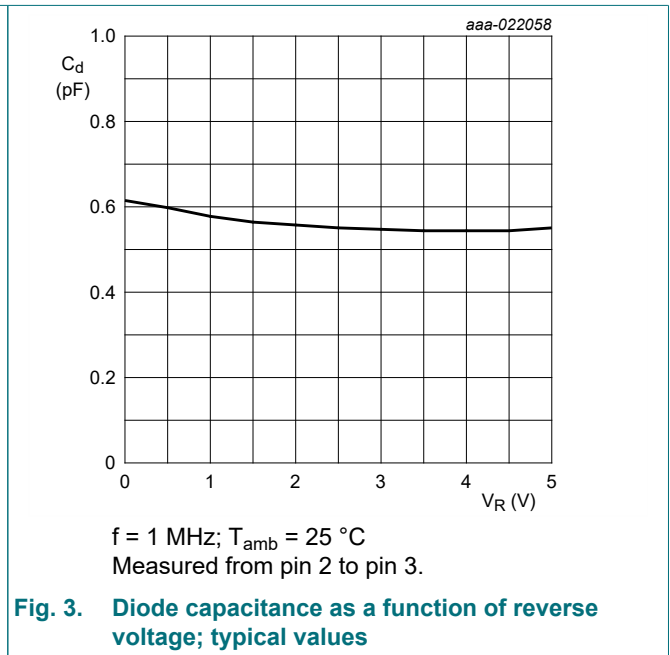
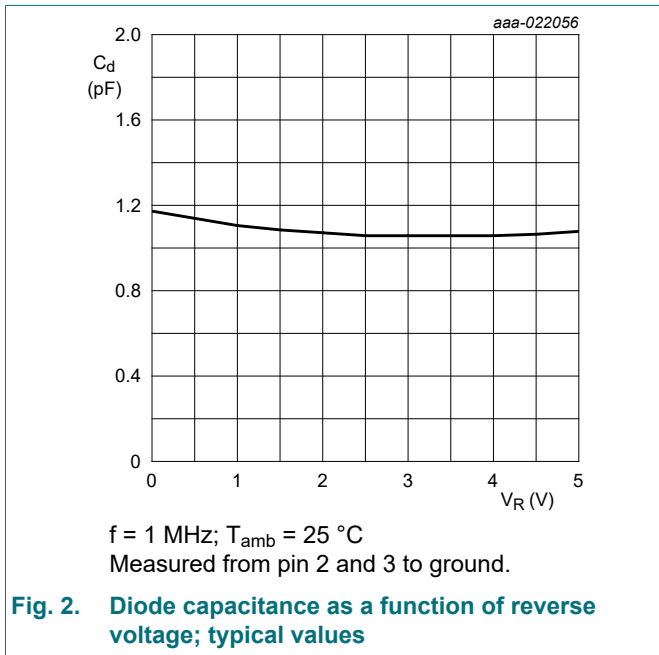
**Fig. 1. ESD pulse waveform according to IEC 61000-4-2**

## 9. Characteristics

Table 6. Characteristics

| Symbol    | Parameter                | Conditions   |     | Min | Typ | Max | Unit |
|-----------|--------------------------|--|-----|-----|-----|-----|------|
| $V_F$     | forward voltage          | $I_F = 1 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$                   | [1] | -   | 0.7 | -   | V    |
| $V_{RWM}$ | reverse standoff voltage | $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$                                       |     | -   | -   | 5.5 | V    |
| $V_{BR}$  | breakdown voltage        | $I_R = 1 \text{ mA}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$                   | [2] | 6   | -   | 9   | V    |
| $I_R$     | reverse current          | $V_R = 3 \text{ V}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$                    | [3] | -   | 1   | 100 | nA   |
| $C_d$     | diode capacitance        | $f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ | [1] | -   | 1   | 1.5 | pF   |
|           |                          |  | [4] | -   | 0.6 | -   | pF   |
|           |                          |  | [2] | -   | 16  | -   | pF   |

- [1] Measured from pin 2 and 3 to ground.
- [2] Measured from pin 4 to ground.
- [3] Measured from pin 2, 3 and 4 to ground.
- [4] Measured from pin 2 to pin 3.



Ultra low capacitance double rail-to-rail ESD protection diode



Fig. 4. ESD clamping test setup and waveforms

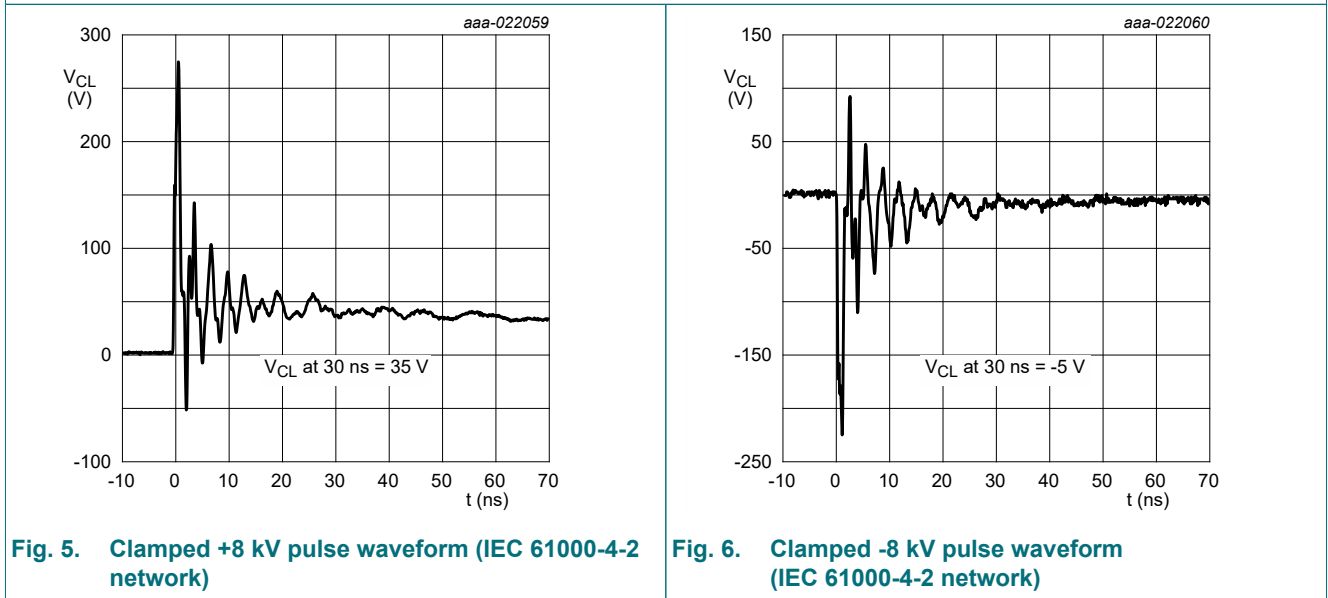


Fig. 5. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

Fig. 6. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)

## 10. Application information

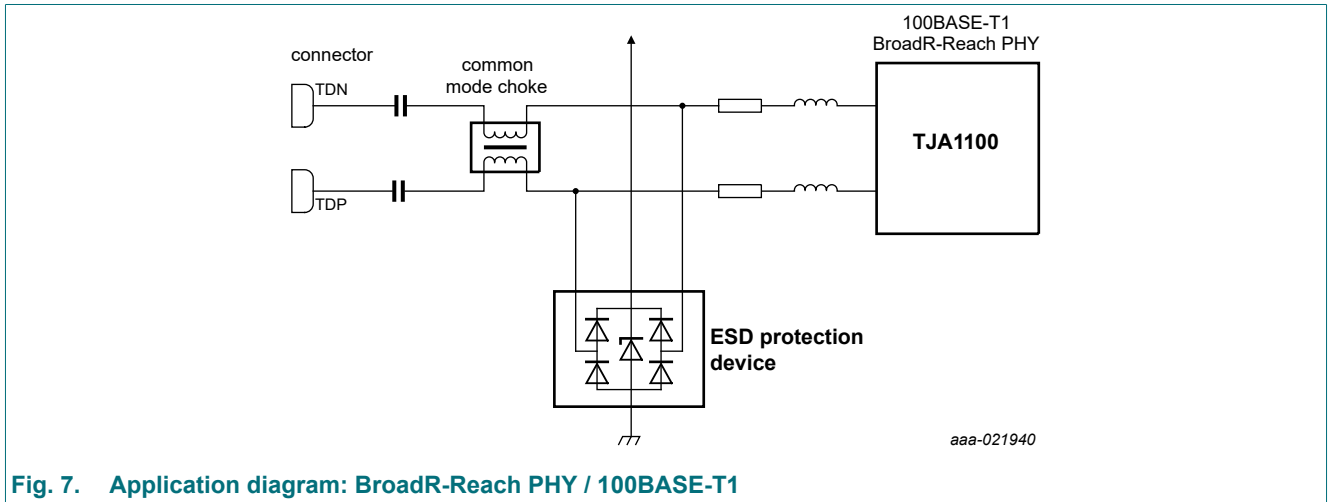


Fig. 7. Application diagram: BroadR-Reach PHY / 100BASE-T1

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

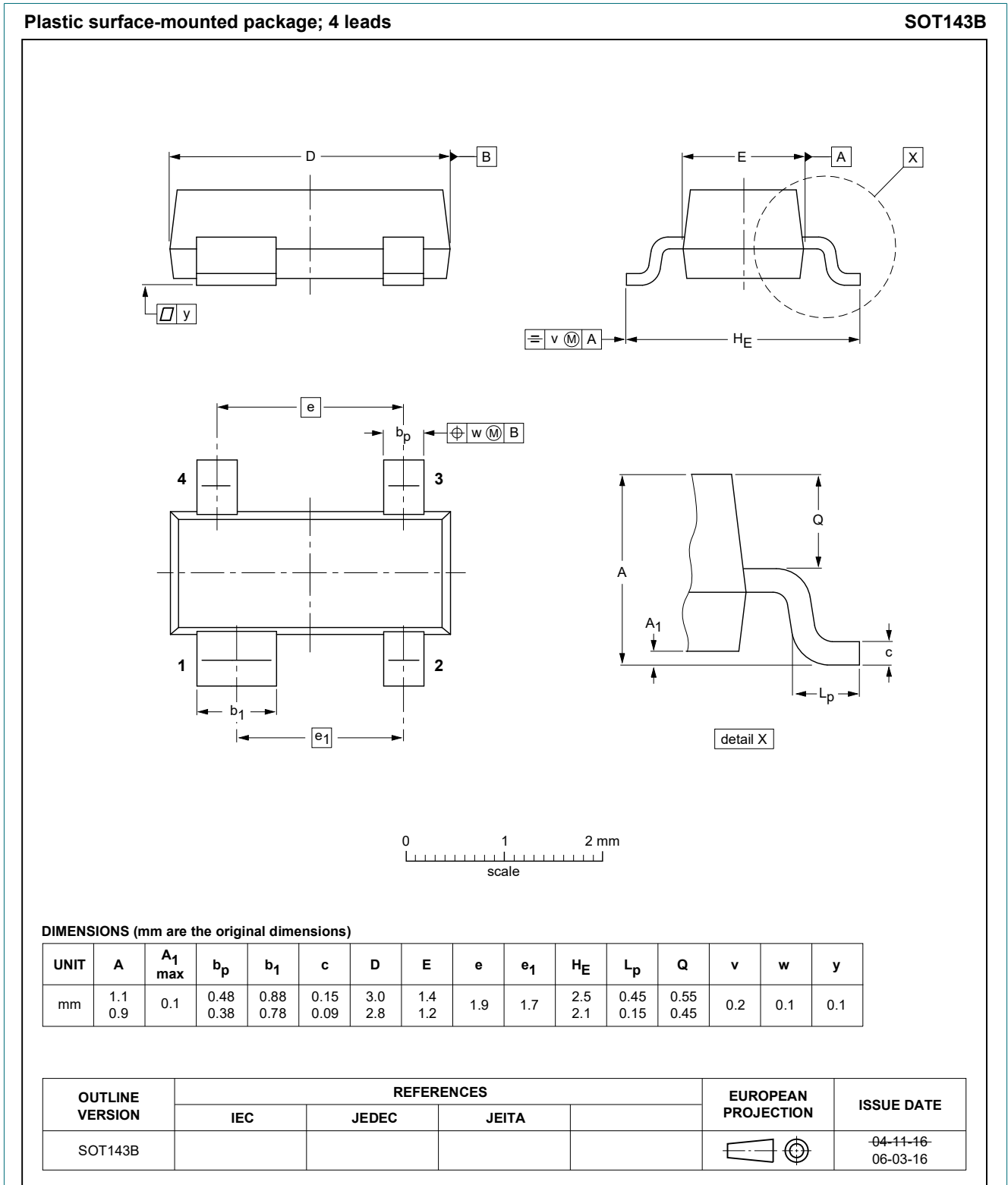


Fig. 8. Package outline SOT143B

### 13. Soldering

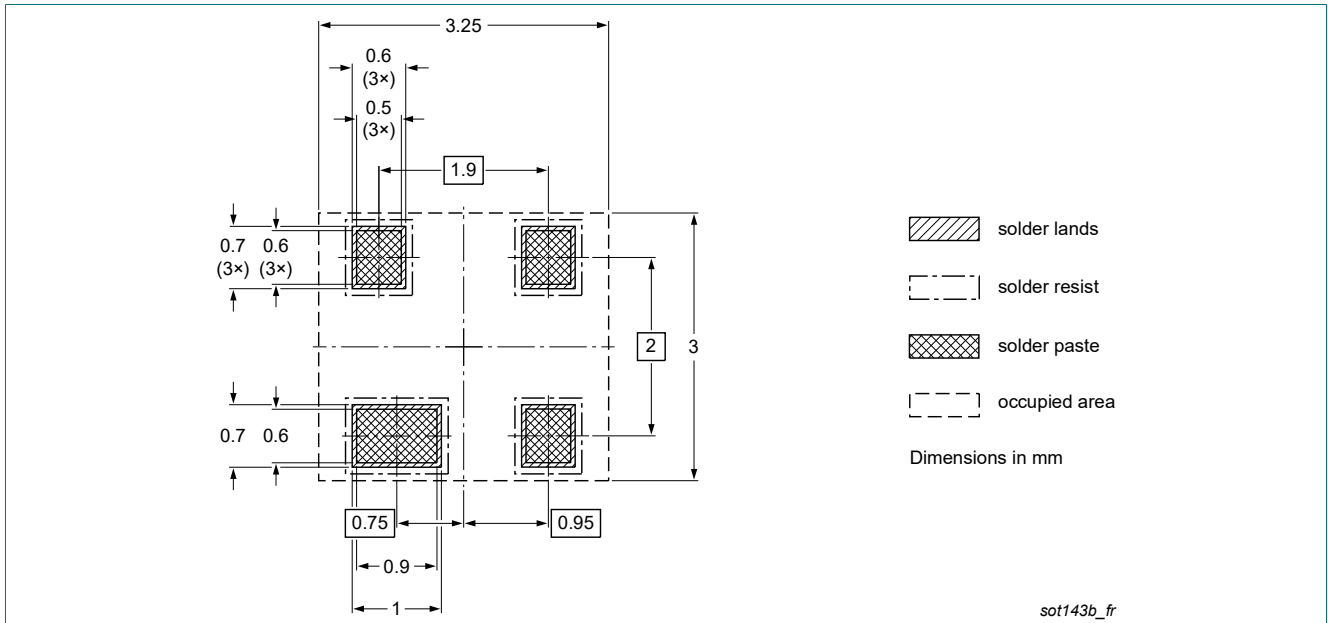


Fig. 9. Reflow soldering footprint for SOT143B

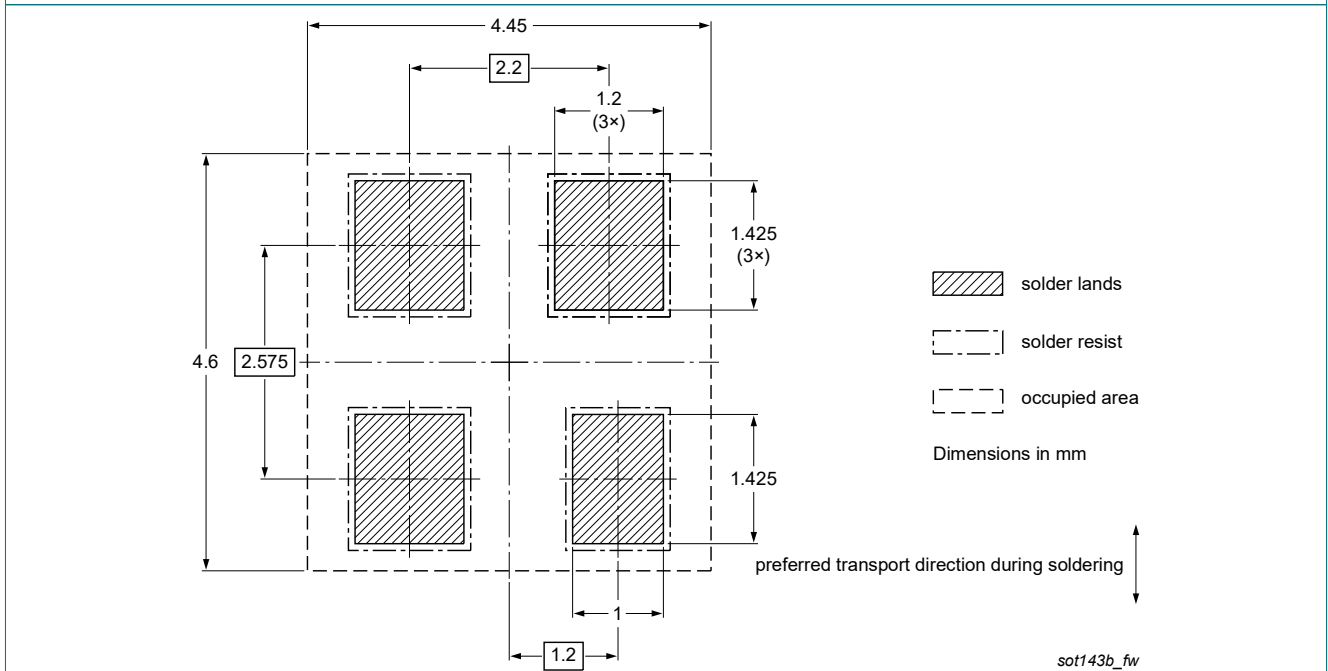


Fig. 10. Wave soldering footprint for SOT143B



## 14. Revision history

Table 7. Revision history

| Data sheet ID   | Release date | Data sheet status  | Change notice | Supersedes |
|-----------------|--------------|--------------------|---------------|------------|
| PESD2ETHX-Q v.1 | 20220503     | Product data sheet | -             | -          |

## 15. Legal information

### Data sheet status

| Document status [1][2]         | Product status [3] | Definition  |
|--------------------------------|--------------------|---|
| Objective [short] data sheet   | Development        | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification      | This document contains data from the preliminary specification.                       |
| Product [short] data sheet     | Production         | This document contains the product specification.                                     |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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