



PDTD113ET

50 V, 500 mA NPN resistor-equipped transistor;
R1 = 1 k Ω , R2 = 1 k Ω

26 March 2025

Product data sheet

1. General description

500 mA NPN Resistor-Equipped Transistor (RET) in a small SOT23 Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- Built-in bias resistors
- Reduces component count
- Simplifies circuit design
- Reduces pick and place costs
- 500 mA output current capability
- 10 % resistor ratio tolerance
- AEC-Q101 qualified

3. Applications

- Digital application in automotive and industrial segments
- Controlling IC inputs
- Cost saving alternative for BC817 series in digital applications
- Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base	-	-	50	V
I _O	output current		-	-	500	mA
R1	bias resistor 1 (input)	T _{amb} = 25 °C	0.7	1	1.3	k Ω
R2/R1	bias resistor ratio		0.9	1	1.1	

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	<p>SOT23</p>	<p>sym007</p>
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTD113ET	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PDTD113ET	% 7R

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
V _I	input voltage			-10	10	V
I _O	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	250	mW
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

9. Thermal characteristics

Table 6. Thermal characteristics

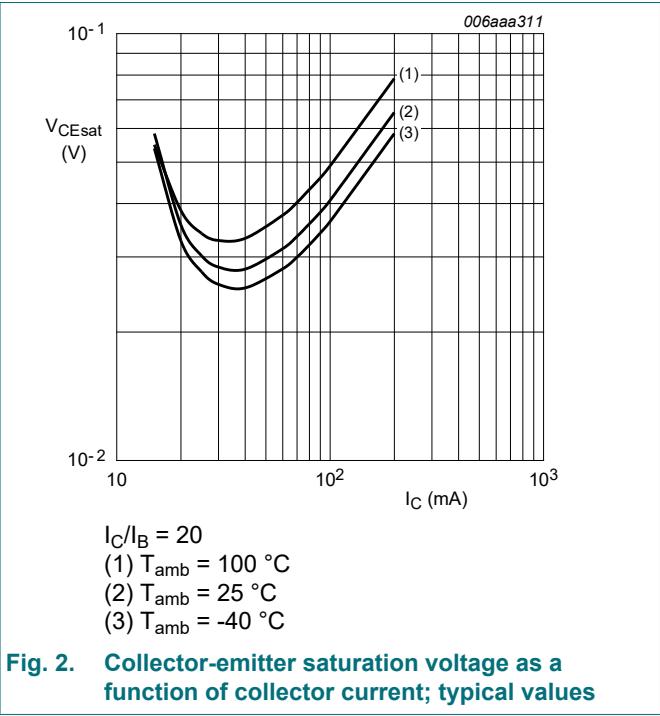
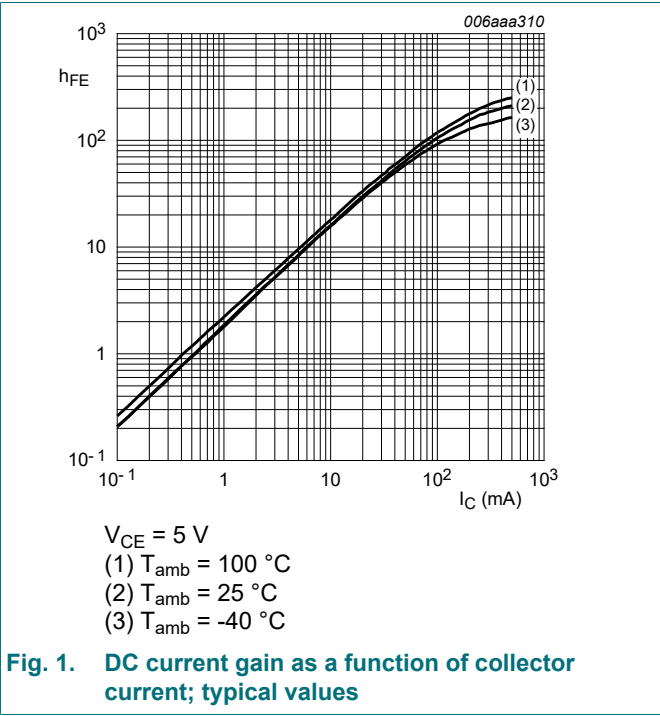
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1]	-	-	500	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{CBO}	collector-base cut-off current	V _{CB} = 40 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
		V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C	-	-	100	nA
I _{CEO}	collector-emitter cut-off current	V _{CE} = 50 V; I _B = 0 A; T _{amb} = 25 °C	-	-	0.5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C	-	-	4	mA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 50 mA; T _{amb} = 25 °C	33	-	-	
V _{CEsat}	collector-emitter saturation voltage	I _C = 50 mA; I _B = 2.5 mA; T _{amb} = 25 °C	-	-	0.3	V
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C	0.6	1.1	1.5	V
V _{I(on)}	on-state input voltage	V _{CE} = 0.3 V; I _C = 20 mA; T _{amb} = 25 °C	1	1.4	1.8	V
R1	bias resistor 1 (input)	T _{amb} = 25 °C	0.7	1	1.3	kΩ
R2/R1	bias resistor ratio		0.9	1	1.1	
C _c	collector capacitance	V _{CB} = 10 V; I _E = 0 A; i _e = 0 A; f = 100 MHz; T _{amb} = 25 °C	-	7	-	pF



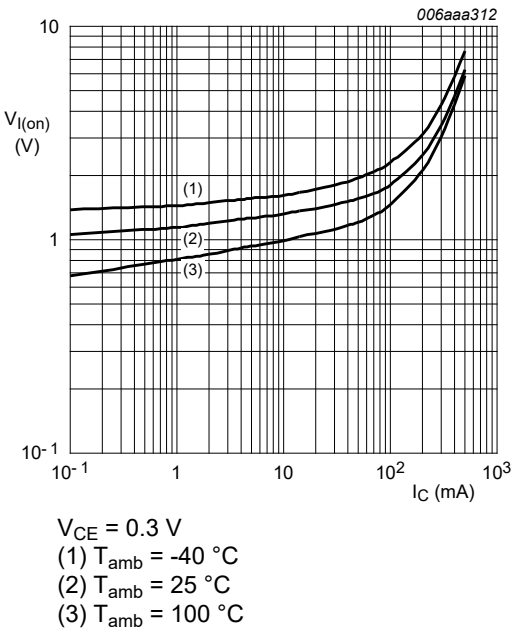


Fig. 3. On-state input voltage as a function of collector current; typical values

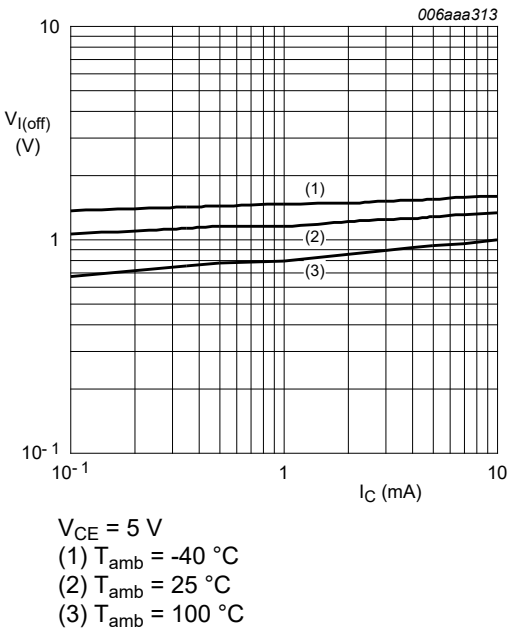


Fig. 4. Off-state input voltage as a function of collector current; typical values

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

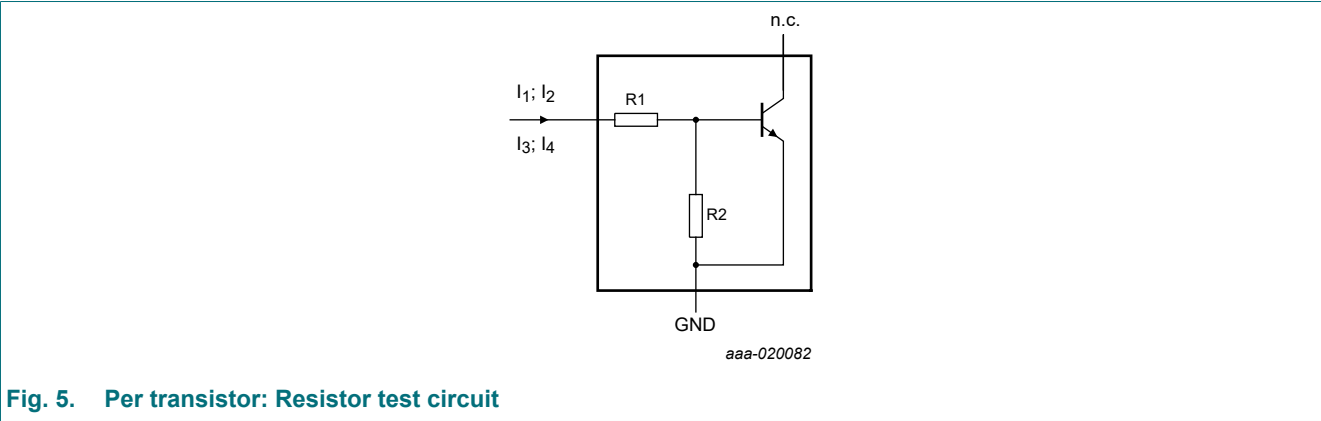
Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

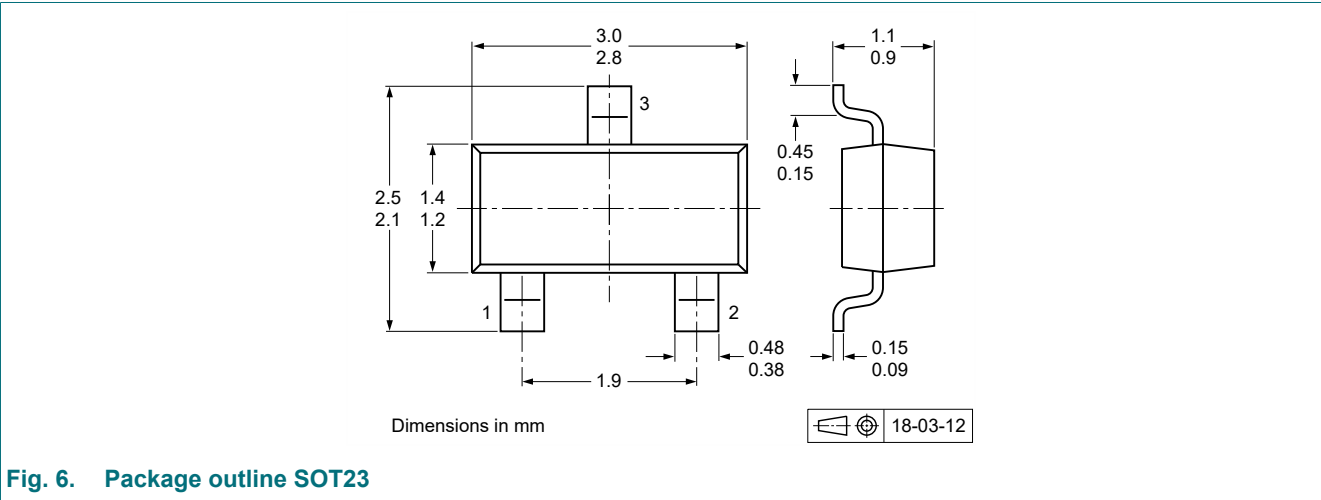


Resistor test conditions

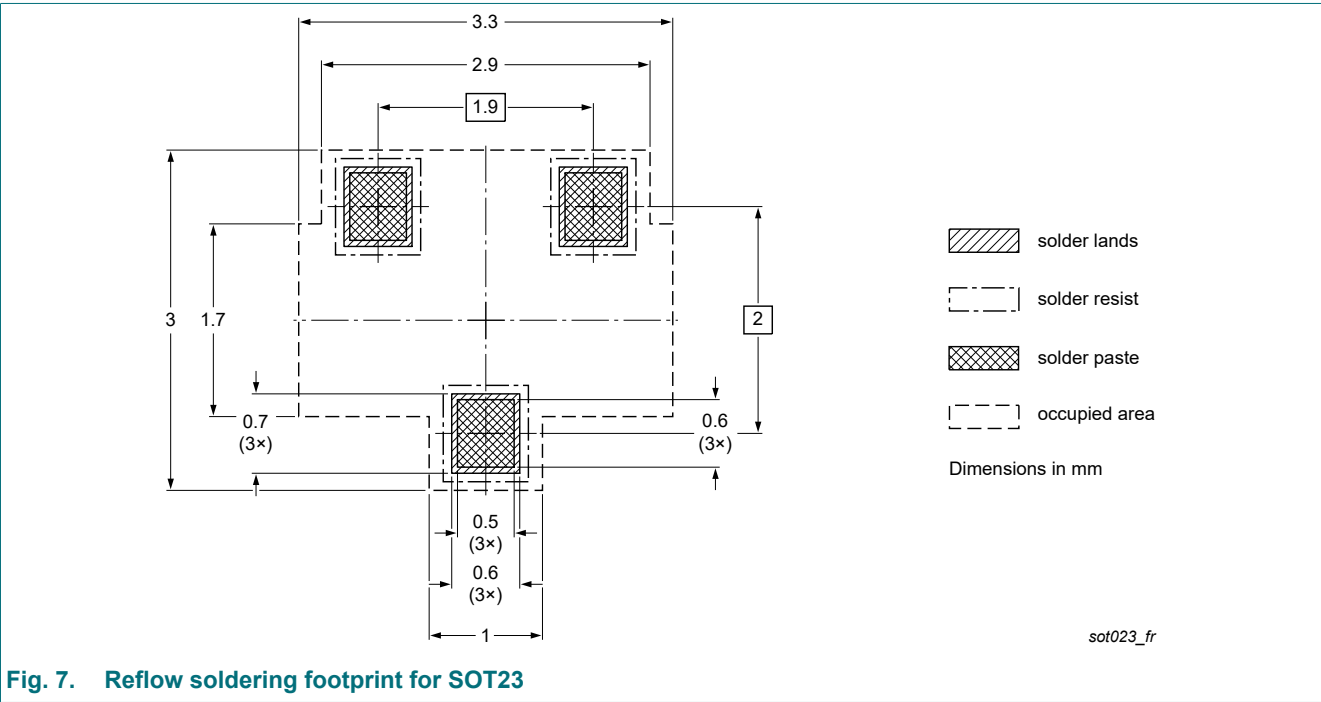
Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTD113ET	1	1	1.5 mA	1.9 mA	-2.0 mA	-2.4 mA

12. Package outline



13. Soldering



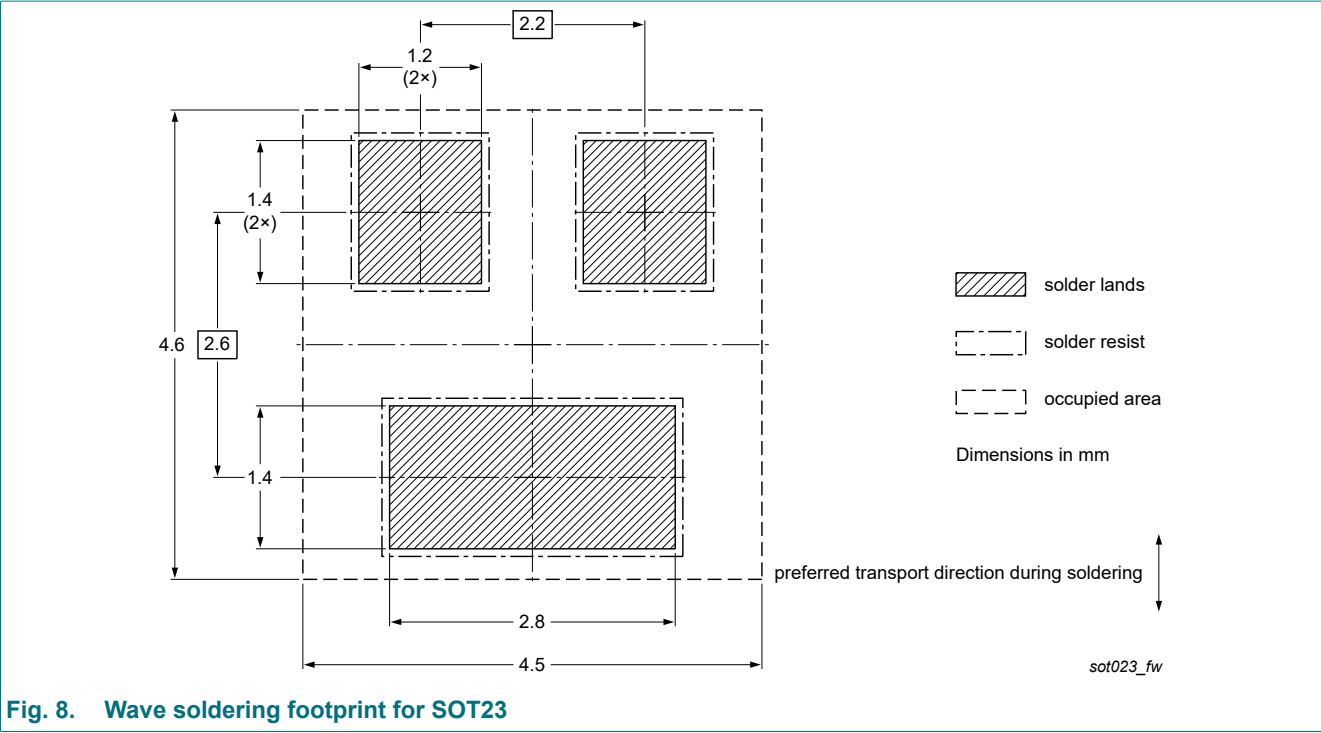


Fig. 8. Wave soldering footprint for SOT23

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTD113ET v.3	20250326	Product data sheet	-	PDTD113E_SER_2
Modifications:	<ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Family data sheet splitted to single type data sheet. Obsolete products are removed.• Section "Packing information" removed.• Test information extended.			
PDTD113E_SER_2	20091116	Product data sheet	-	PDTD113E_SER_1
PDTD113E_SER_1	20050414	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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