CBT3306

Dual bus switch

Rev. 9 — 18 March 2021 Product data sheet

1. General description

The CBT3306 dual FET bus switch features independent line switches. Each switch is disabled when the associated output enable ($n\overline{OE}$) input is HIGH.

2. Features and benefits

- 5 Ω switch connection between two ports
- Direct interface with TTL levels
- Overvoltage tolerant control inputs to 5.5 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up protection exceeds 100 mA per JESD78B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - CDM JESD22-C101D exceeds 1000 V
- Specified from -40 °C to +85 °C

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
CBT3306PW	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 4.4 mm	SOT530-1
CBT3306GT	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1

4. Marking

Table 2. Marking codes

Type number	Marking code
CBT3306PW	3306
CBT3306GT	F06

5. Functional diagram

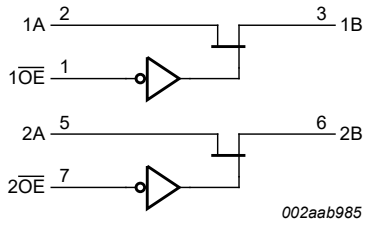


Fig. 1. Logic diagram

6. Pinning information

6.1. Pinning

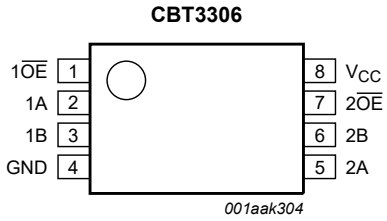
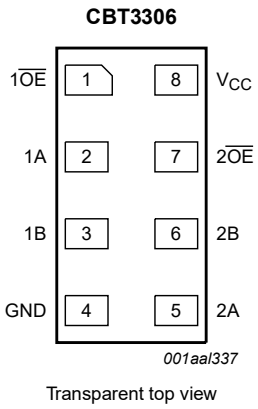


Fig. 2. Pin configuration SOT530-1 (TSSOP8)



Transparent top view

Fig. 3. Pin configuration SOT833-1 (XSON8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$	1, 7	output enable input
1A, 2A	2, 5	data input/output (A port)
1B, 2B	3, 6	data input/output (B port)
GND	4	ground (0 V)
V_{CC}	8	positive supply voltage

7. Functional description

Table 4. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input	Input/output
n$\overline{OE}$	**nA, nB**
L	nA = nB
H	Z

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	T_{amb} = -40 °C to +85 °C		Unit
			Min	Max	
V_{CC}	supply voltage		-0.5	+7.0	V
V_I	input voltage	[1]	-0.5	+7.0	V
I_O	output current		-	128	mA
I_{IK}	input clamping current	$V_{I/O}$ = 0 V	-50	-	mA
T_{stg}	storage temperature		-65	+150	°C

[1] The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

9. Recommended operating conditions

Table 6. Operating conditions

All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		4.5	-	5.5	V
V_{IH}	HIGH-level input voltage		2.0	-	-	V
V_{IL}	LOW-level input voltage		-	-	0.8	V
T_{amb}	ambient temperature	operating in free air	-40	-	+85	°C

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ[1]	Max	
V_{IK}	input clamping voltage	V_{CC} = 4.5 V; I_I = -18 mA	-	-	-1.2	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = GND or 5.5 V	-	-	±1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; I_O = 0 mA; V_I = V_{CC} or GND	-	-	3	µA
V_{pass}	pass voltage	output HIGH; V_I = V_{CC} = 5.0 V; I_O = -100 µA	3.6	3.9	4.2	V
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 5.5 V; one input at 3.4 V, other inputs at V_{CC} or GND [2]	-	-	2.5	mA
C_I	input capacitance	control pin; V_I = 3 V or 0 V	-	3.15	-	pF
$C_{io(off)}$	off-state input/output capacitance	port off; V_I = 3 V or 0 V; $n\overline{OE}$ = V_{CC}	-	6.45	-	pF
R_{ON}	ON resistance	V_{CC} = 4.5 V; V_I = 0 V; I_I = 64 mA [3]	-	3.4	5	Ω
		V_{CC} = 4.5 V; V_I = 0 V; I_I = 30 mA [3]	-	3.4	5	Ω
		V_{CC} = 4.5 V; V_I = 2.4 V; I_I = 15 mA [3]	-	6.8	15	Ω

[1] All typical values are measured at V_{CC} = 5 V, T_{amb} = 25 °C.
[2] This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.
[3] Measured by the voltage drop between the nA and the nB terminals at the indicated current through the switch. ON resistance is determined by the lowest voltage of the two (nA, nB) terminals.

11. Dynamic characteristics

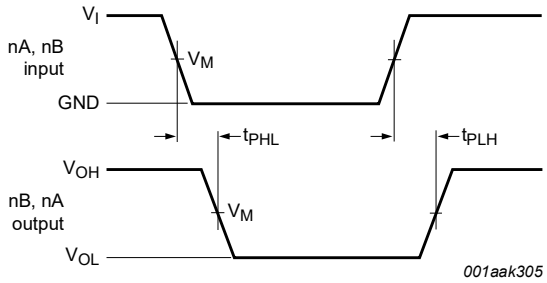
Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			Unit
			Min	Typ	Max	
t_{pd}	propagation delay	nA, nB to nB, nA; see Fig. 4 [1] [2]	-	-	0.25	ns
		V_{CC} = 5.0 V ± 0.5 V				
t_{en}	enable time	$n\overline{OE}$ to nA, nB; see Fig. 5 [2]	1.0	-	5.0	ns
		V_{CC} = 5.0 V ± 0.5 V				
t_{dis}	disable time	$n\overline{OE}$ to nA, nB; see Fig. 5 [2]	1.0	-	5.0	ns
		V_{CC} = 5.0 V ± 0.5 V				

[1] The propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
[2] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

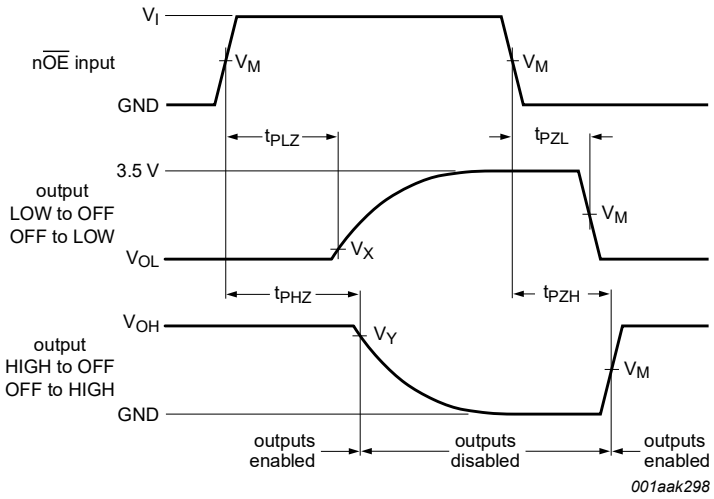
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 4. The data input (nA, nB) to output (nB, nA) propagation delay times



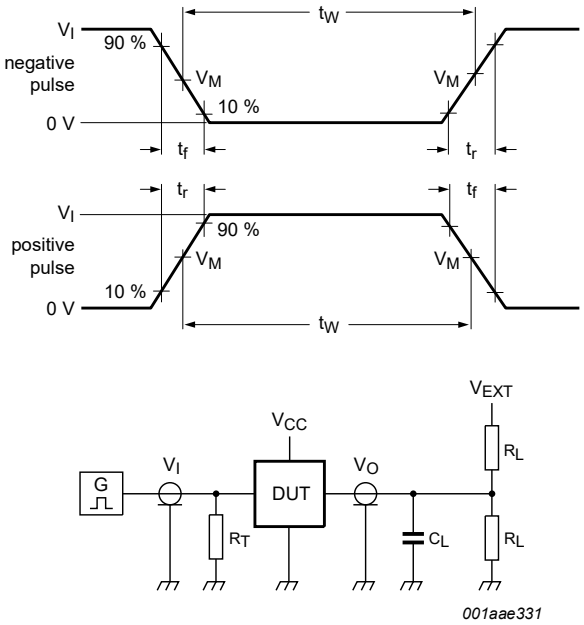
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 5. Enable and disable times

Table 9. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	1.5 V	1.5 V	V_{OL} + 0.3 V	V_{OH} - 0.3 V



Test data is given in Table 10.

All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω.

The outputs are measured one at a time with one transition per measurement.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

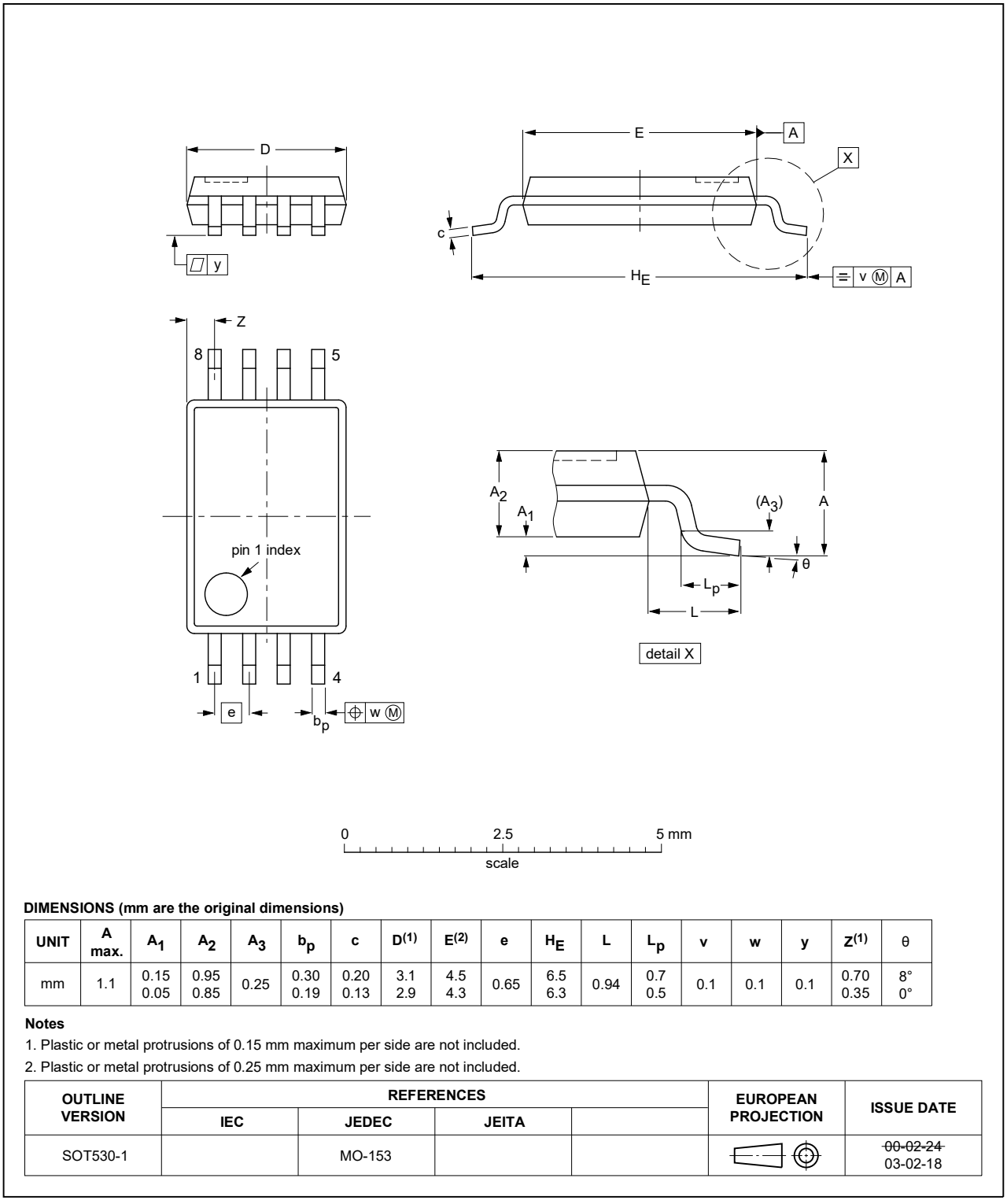
Fig. 6. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
V_{CC} = 5.0 V ± 0.5 V	GND to 3.0 V	≤ 2.5 ns	50 pF	500 Ω	open	7.0 V	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.85	0.25	0.30 0.19	0.20 0.13	3.1 2.9	4.5 4.3	0.65	6.5 6.3	0.94	0.7 0.5	0.1	0.1	0.1	0.70 0.35	8° 0°

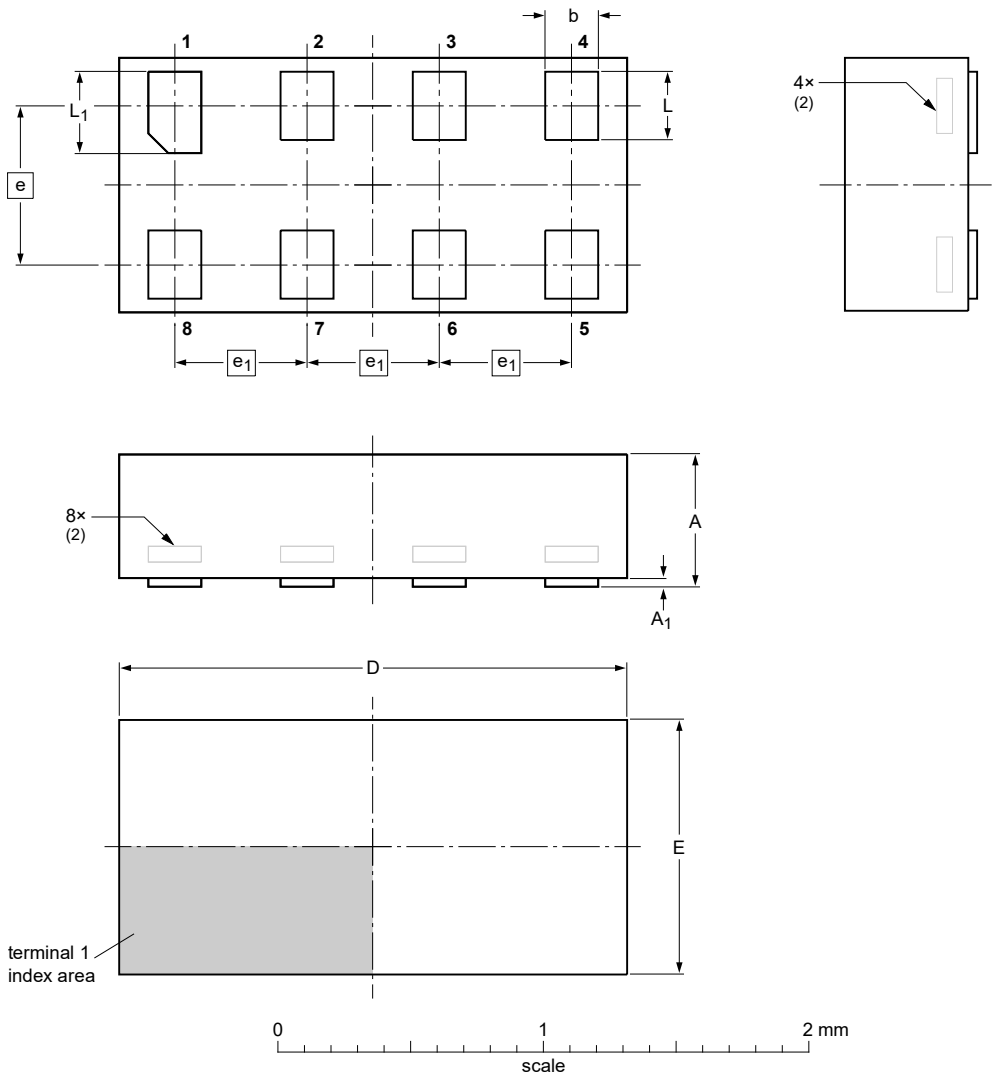
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT530-1		MO-153				~~00-02-24~~ 03-02-18

Fig. 7. Package outline sot530-1 (TSSOP8)

XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm **SOT833-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A_1 max	b	D	E	e	e_1	L	L_1
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig. 8. Package outline SOT833-1 (XSON8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CDM	Charged Device Model
ESD	ElectroStatic Discharge
FET	Field Effect Transistor
HBM	Human Body Model
PRR	Pulse Rate Repetition
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
CBT3306 v.9	20210318	Product data sheet	-	CBT3306 v.8
Modifications:	• Section 2 updated. • Type number CBT3306GM (SOT902-2 / XQFN8) removed.			
CBT3306 v.8	20190306	Product data sheet	-	CBT3306 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number CBT3306D (SOT96-1) removed. • Package outline drawing SOT902-2 (XQFN8) updated.			
CBT3306 v.7	20120501	Product data sheet	-	CBT3306 v.6
Modifications:	• For type number CBT3306GM the sot code has changed to SOT902-2.			
CBT3306 v.6	20111122	Product data sheet	-	CBT3306 v.5
Modifications:	• Legal pages updated.			
CBT3306 v.5	20100325	Product data sheet	-	CBT3306 v.4
CBT3306 v.4	20100218	Product data sheet	-	CBT3306 v.3
CBT3306 v.3	20091014	Product data sheet	-	CBT3306 v.2
CBT3306 v.2	20051117	Product data sheet	-	CBT3306 v.1
CBT3306 v.1	20011108	Product data	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 18 March 2021

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