



# PXN012-60QL

N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

31 July 2023

Product data sheet

## 1. General description

General purpose, 42 A rated, logic level N-channel enhancement mode Power MOSFET in MLPAK33 package.

## 2. Features and benefits

- Logic level compatibility
- Trench MOSFET technology
- Thermally efficient package in a small form factor (3.3 mm x 3.3 mm footprint)

## 3. Applications

- Secondary side synchronous rectification
- DC-to-DC converters
- Motor drive
- LED lighting
- Load switching
- Auxiliary control
- Fan control

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 150 °C		-	-	60	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C; <a href="#">Fig. 2</a>		-	-	42	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	34.7	W
T <sub>j</sub>	junction temperature			-55	-	150	°C
Static characteristics							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>		-	9.8	11.5	mΩ
Dynamic characteristics							
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	4.3	-	nC
Q <sub>G(tot)</sub>	total gate charge			-	9.64	-	nC
Avalanche ruggedness							
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 3.5 A; T <sub>j(init)</sub> = 25 °C; unclamped	<a href="#">[1]</a>	-	-	90	mJ

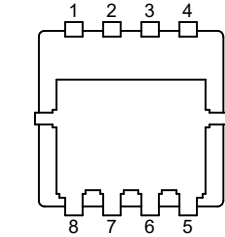
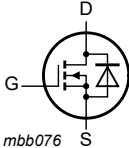
N-channel 60 V, 11.5 mOhm, logic level Trench MOSFET in MLPAK33

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q <sub>r</sub>	recovered charge	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; T <sub>J</sub> = 25 °C; <a href="#">Fig. 15</a>	[2]	-	13	-	nC

[1] Protected by 100% test  
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 MLPAK33 (SOT8002-1)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXN012-60QL	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-1

7. Marking

Table 4. Marking codes

Type number	Marking code
PXN012-60QL	7AB

8. Limiting values

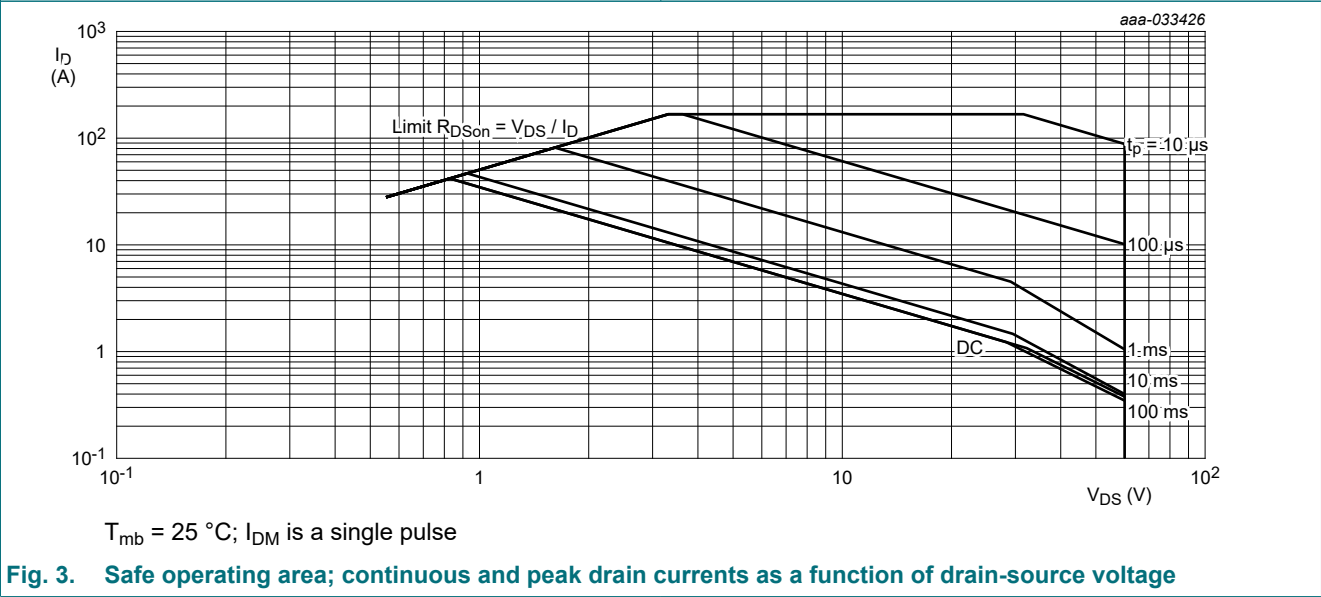
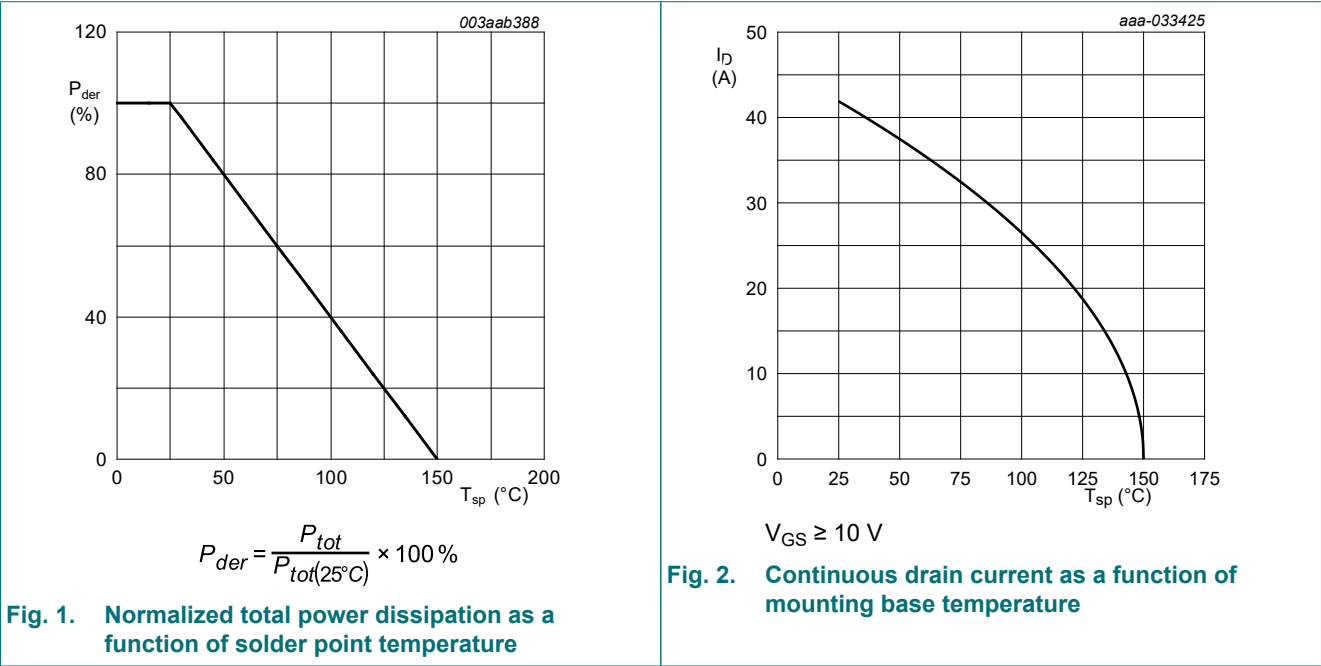
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>J</sub> ≤ 150 °C		-	60	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; <a href="#">Fig. 1</a>		-	34.7	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 25 °C; <a href="#">Fig. 2</a>		-	42	A
		V <sub>GS</sub> = 10 V; T <sub>sp</sub> = 100 °C; <a href="#">Fig. 2</a>		-	26	A
I <sub>DM</sub>	peak drain current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C; <a href="#">Fig. 3</a>		-	168	A
T <sub>stg</sub>	storage temperature			-55	150	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain diode						
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C		-	29	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>sp</sub> = 25 °C		-	168	A
Avalanche ruggedness						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 3.5 A; T <sub>j(init)</sub> = 25 °C; unclamped	[1]	-	90	mJ
I <sub>AS</sub>	non-repetitive avalanche current	T <sub>j(init)</sub> = 25 °C	[1]	-	3.5	A

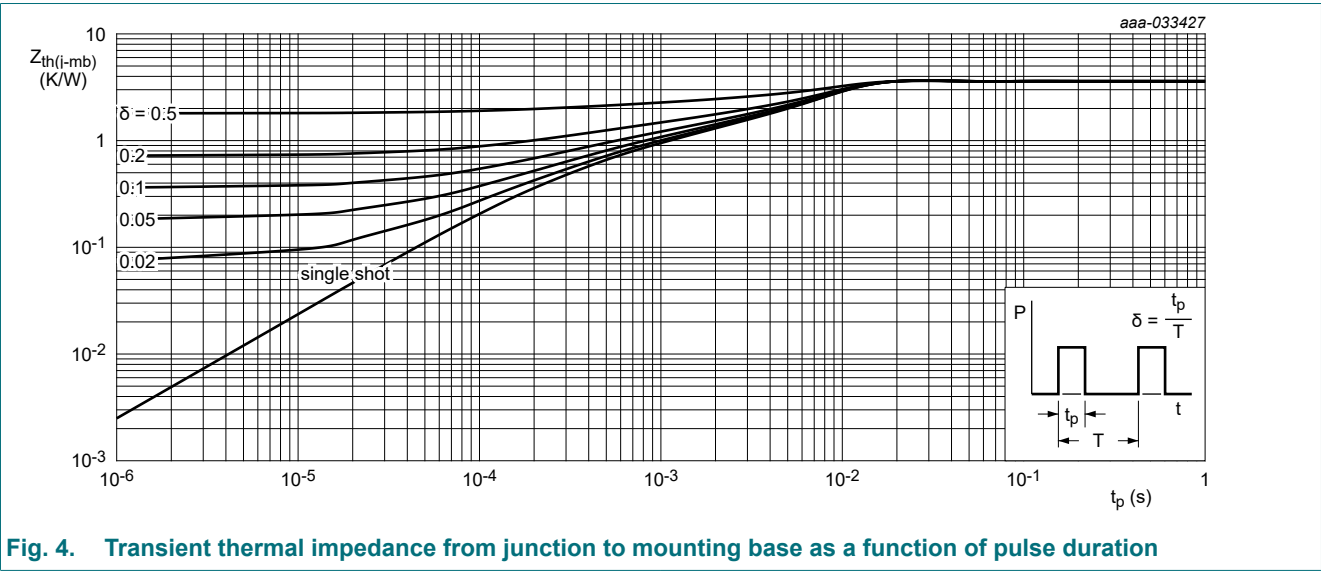
[1] Protected by 100% test



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 4		-	3	3.6	K/W



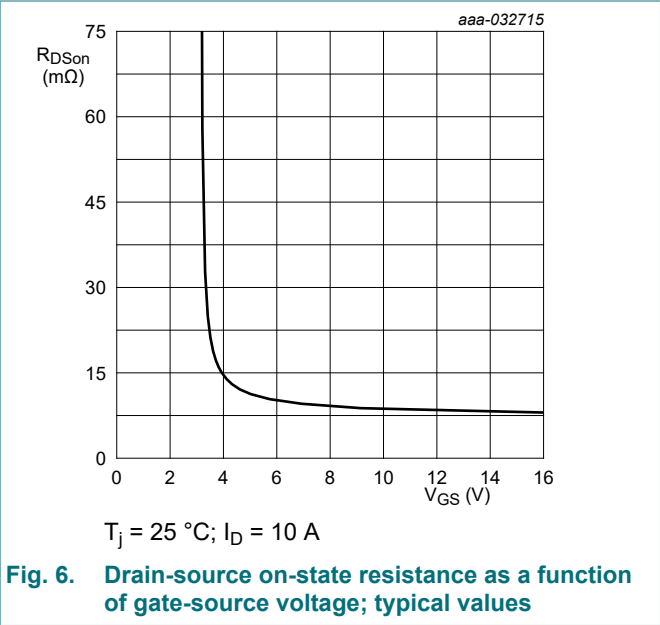
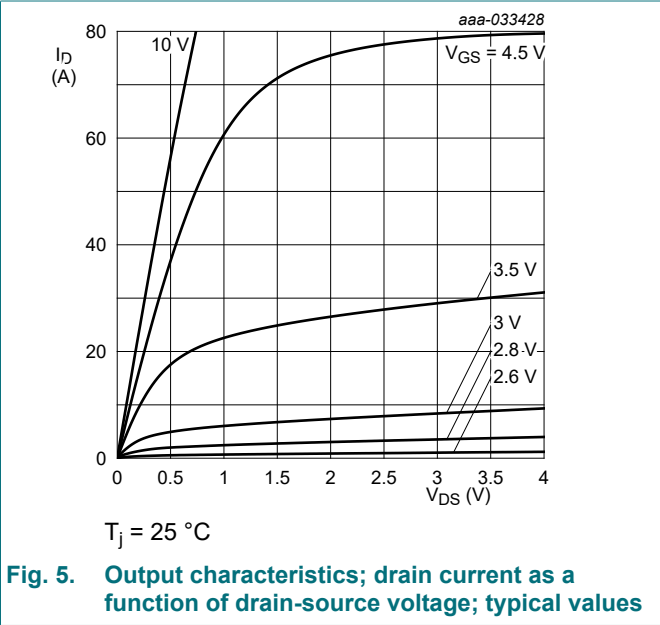
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$		60	70	-	V
		$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = -55\text{ }^\circ\text{C}$		-	64	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS}=V_{GS}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; Fig. 8		1.5	1.9	2.5	V
		$I_D = 1\text{ mA}$ ; $V_{DS}=V_{GS}$ ; $T_J = 150\text{ }^\circ\text{C}$		0.9	-	-	V
		$I_D = 1\text{ mA}$ ; $V_{DS}=V_{GS}$ ; $T_J = -55\text{ }^\circ\text{C}$		-	-	2.9	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\text{ }^\circ\text{C} \leq T_J \leq 150\text{ }^\circ\text{C}$		-	-4.7	-	mV/K
$I_{DSS}$	drain leakage current	$V_{DS} = 60\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$		-	0.01	1	$\mu\text{A}$
		$V_{DS} = 60\text{ V}$ ; $V_{GS} = 0\text{ V}$ ; $T_J = 150\text{ }^\circ\text{C}$		-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA
		$V_{GS} = -20\text{ V}$ ; $V_{DS} = 0\text{ V}$ ; $T_J = 25\text{ }^\circ\text{C}$		-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; Fig. 9		-	9.8	11.5	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; Fig. 10		-	-	20	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_J = 25\text{ }^\circ\text{C}$ ; Fig. 9		-	14	17.6	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ ; $I_D = 10\text{ A}$ ; $T_J = 150\text{ }^\circ\text{C}$ ; Fig. 10		-	-	30	m $\Omega$
$R_G$	gate resistance	$f = 1\text{ MHz}$ ; $T_J = 25\text{ }^\circ\text{C}$		-	1.66	-	$\Omega$

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12		-	9.64	-	nC
		I <sub>D</sub> = 10 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12		-	18.77	-	nC
		I <sub>D</sub> = 0 A; V <sub>DS</sub> = 0 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12		-	9.54	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 4.5 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12		-	3	-	nC
Q <sub>GS(th)</sub>	pre-threshold gate-source charge			-	1.6	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate-source charge			-	1.4	-	nC
Q <sub>GD</sub>	gate-drain charge			-	4.3	-	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C; Fig. 11; Fig. 12		-	3.1	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 30 V; V <sub>GS</sub> = 0 V; f = 1 MHz; T <sub>j</sub> = 25 °C; Fig. 13		-	957	-	pF
C <sub>oss</sub>	output capacitance			-	386	-	pF
C <sub>rss</sub>	reverse transfer capacitance			-	31	-	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DS</sub> = 30 V; R <sub>L</sub> = 3 Ω; V <sub>GS</sub> = 4.5 V; R <sub>G(ext)</sub> = 5 Ω; T <sub>j</sub> = 25 °C		-	8.8	-	ns
t <sub>r</sub>	rise time			-	18.5	-	ns
t <sub>d(off)</sub>	turn-off delay time			-	12.2	-	ns
t <sub>f</sub>	fall time			-	10.9	-	ns
Q <sub>oss</sub>	output charge	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; f = 1 MHz; T <sub>j</sub> = 25 °C		-	18	-	nC
Source-drain diode							
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 10 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; Fig. 14		-	0.82	1.2	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 10 A; dI <sub>S</sub> /dt = -100 A/μs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 30 V; T <sub>j</sub> = 25 °C; Fig. 15		-	22.1	-	ns
Q <sub>r</sub>	recovered charge		[1]	-	13	-	nC

[1] includes capacitive recovery



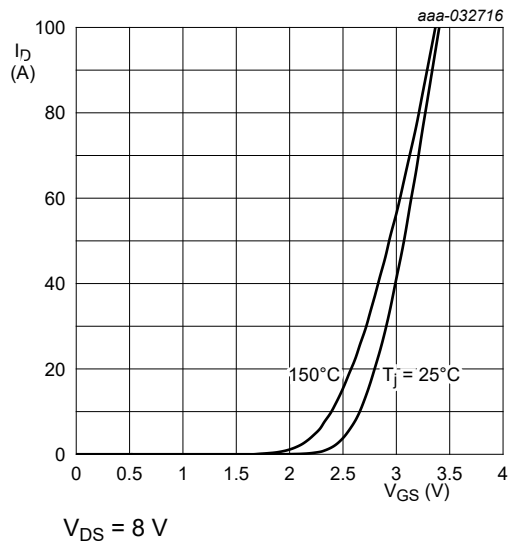


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

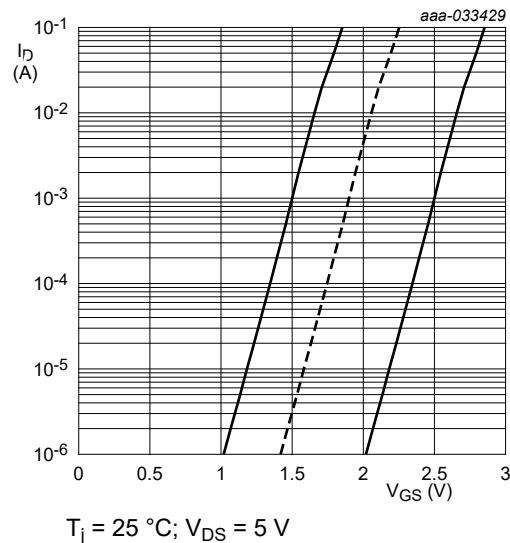


Fig. 8. Sub-threshold drain current as a function of gate-source voltage

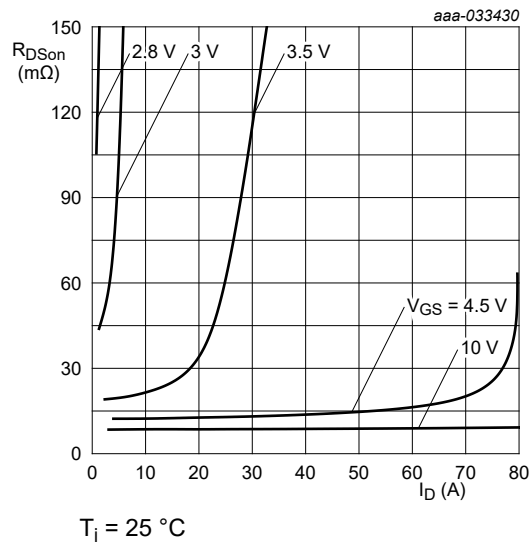


Fig. 9. Drain-source on-state resistance as a function of drain current; typical values

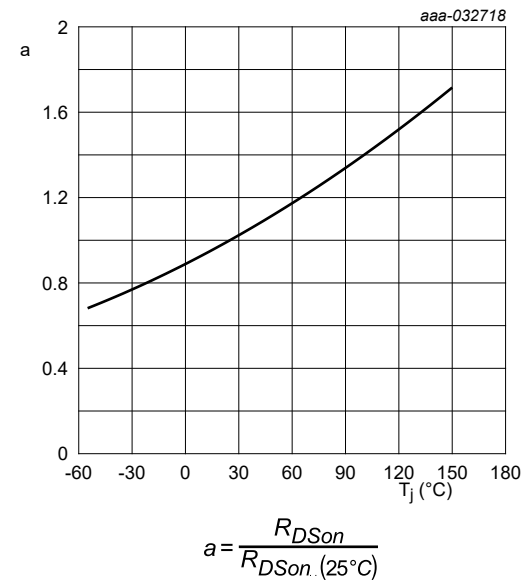


Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature

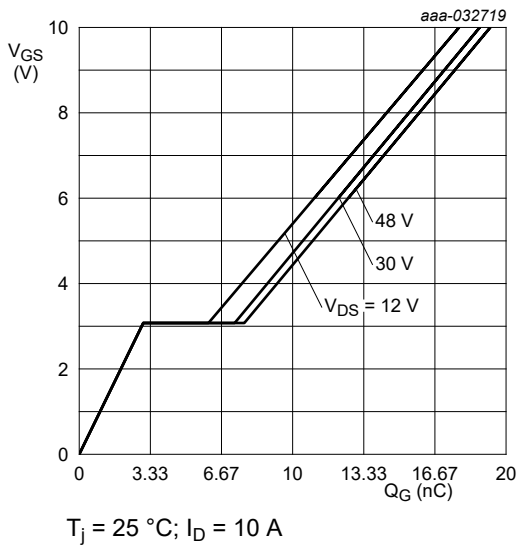


Fig. 11. Gate-source voltage as a function of gate charge; typical values

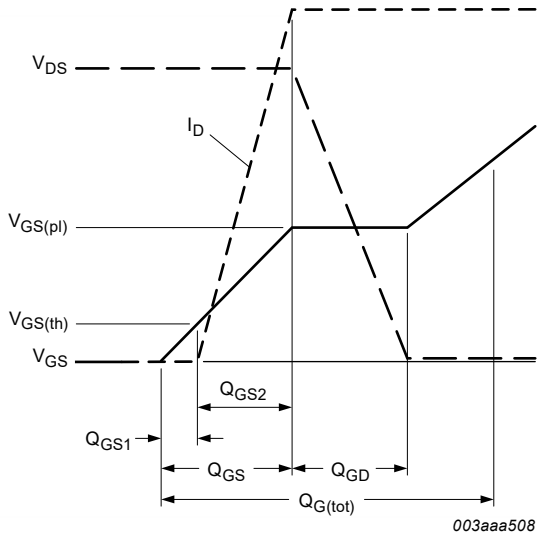


Fig. 12. Gate charge waveform definitions

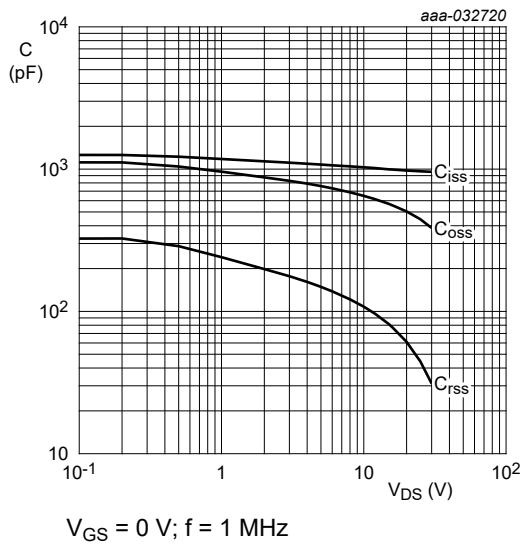


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

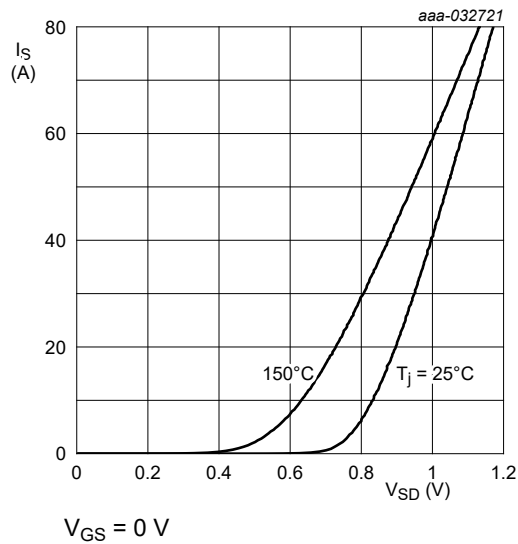


Fig. 14. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

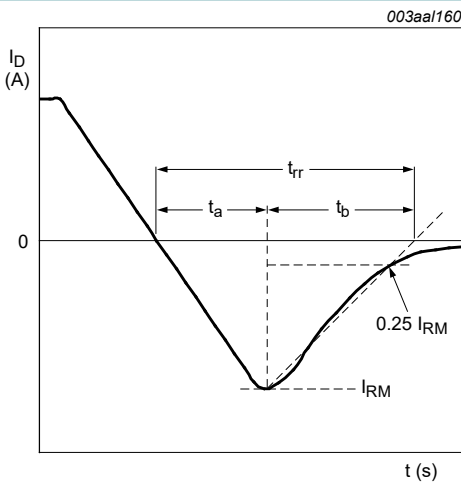


Fig. 15. Reverse recovery timing definition

11. Package outline

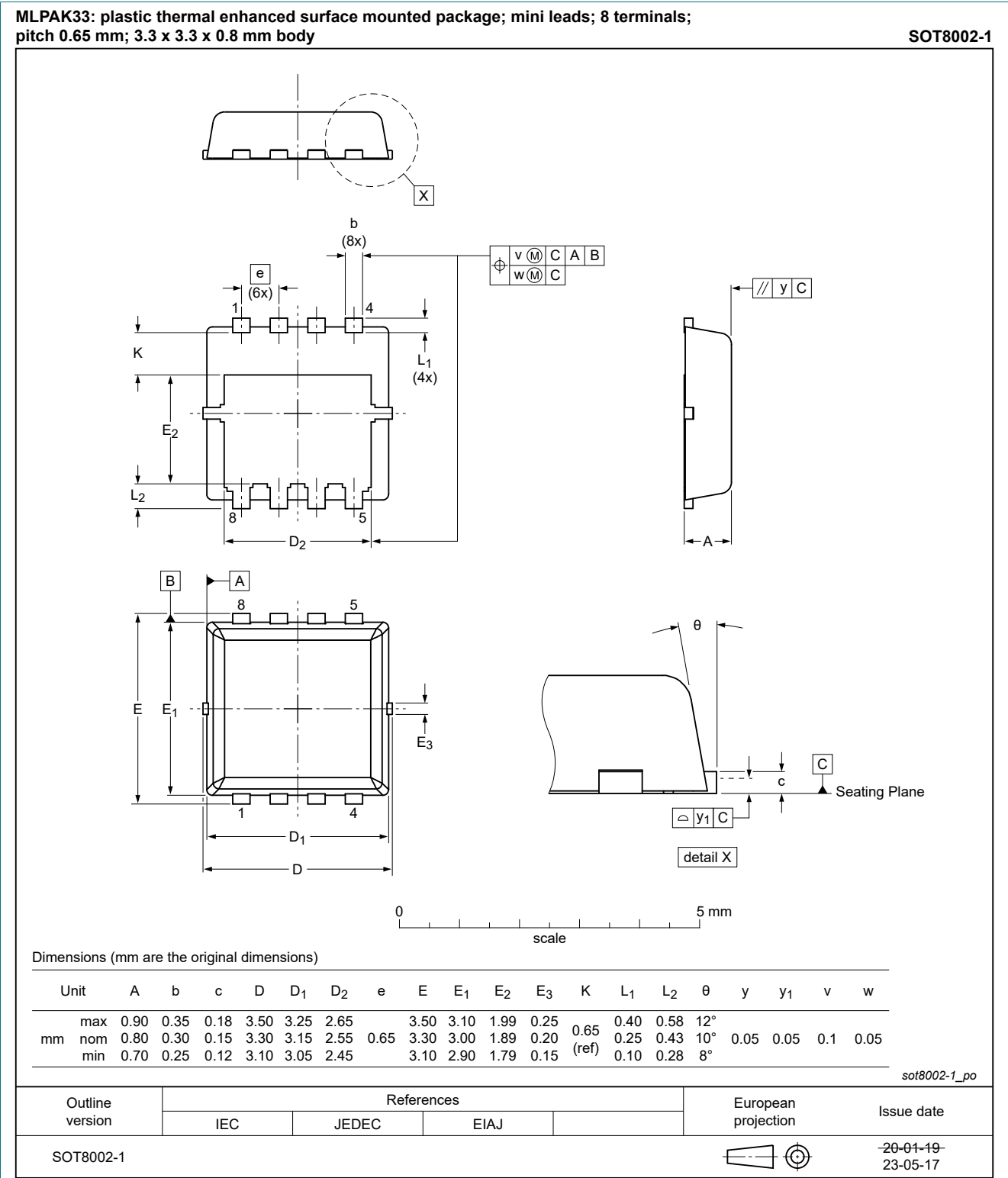


Fig. 16. Package outline MLPAK33 (SOT8002-1)



12. Soldering

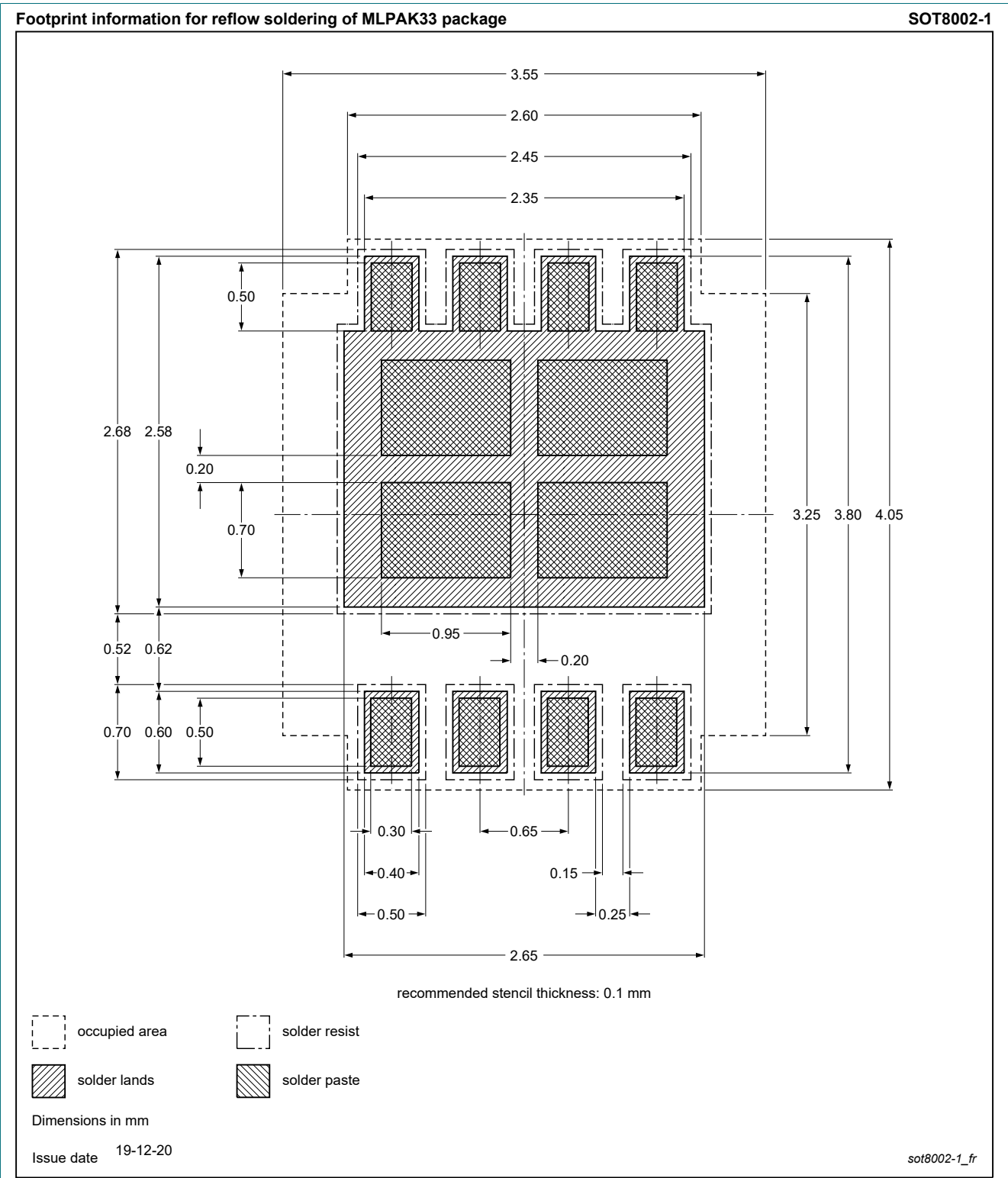


Fig. 17. Reflow soldering footprint for MLPAK33 (SOT8002-1)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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