

PUMH13-Q

NPN/NPN double Resistor-Equipped Transistor (RET); R1= 4.7 k Ω , R2 = 47 k Ω

15 May 2023

Product data sheet

1. General description

NPN/NPN double Resistor-Equipped Transistor (RET) in a SOT363 (SC-88) very small Surface-Mounted Device (SMD) plastic package.

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- · Simplifies circuit design
- · Reduces component count
- Reduces pick and place costs
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Applications

- Low current peripheral driver
- · Control of IC inputs
- · Replaces general-purpose transistors in digital applications

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit	
Per transistor	Per transistor							
V _{CEO}	collector-emitter voltage	open base		-	-	50	V	
Io	output current			-	-	100	mA	
R1	bias resistor 1 (input)		[1]	3.3	4.7	6.1	kΩ	
R2/R1	bias resistor ratio		[1]	8	10	12		

[1] See section "Test information" for resistor calculation and test conditions.



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		O1 I2 GND2
2	I1	input (base) TR1		
3	O2	output (collector) TR2	6 5 4	R1 R2
4	GND2	GND (emitter) TR2		TR2
5	12	input (base) TR2		TR1
6	01	output (collector) TR1	□1 □2 □3	
			TSSOP6 (SOT363)	
				GND1 I1 O2 sym063

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PUMH13-Q		plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	<u>SOT363</u>

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMH13-Q	но%

[1] % = placeholder for manufacturing site code

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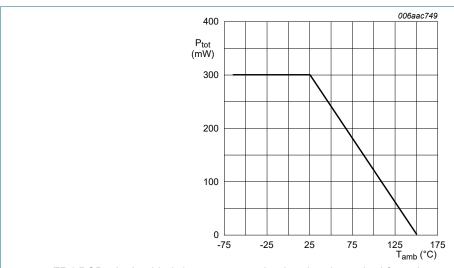
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transiste	or					
V _{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	5	V
VI	input voltage			-5	30	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	200	mW
Per device						
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	300	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.



FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 1. Per device: Power derating curve

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9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transistor	Per transistor						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

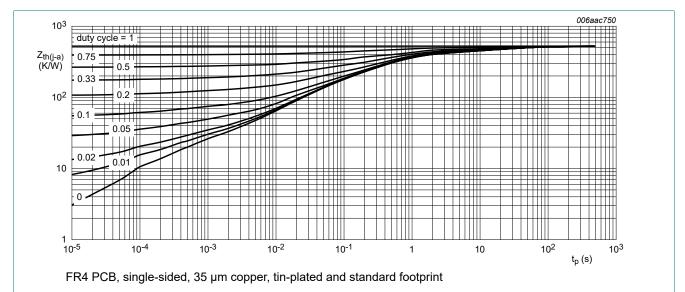


Fig. 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Per transist	or						
V _{(BR)CBO}	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
V _{(BR)CEO}	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 ^{\circ}\text{C}$		50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	100	nA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μA
I _{EBO}	emitter-base cut-off current	V _{EB} = 5 V; I _C = 0 A; T _{amb} = 25 °C		-	-	170	μΑ
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 10 mA; T _{amb} = 25 °C		100	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 5 \text{ mA}; I_B = 0.25 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
V _{I(off)}	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	0.6	0.5	V
V _{I(on)}	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		1.3	0.9	-	V
R1	bias resistor 1 (input)		[1]	3.3	4.7	6.1	kΩ
R2/R1	bias resistor ratio		[1]	8	10	12	
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; $ $T_{amb} = 25 \text{ °C}$		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I_{C} = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See section "Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor

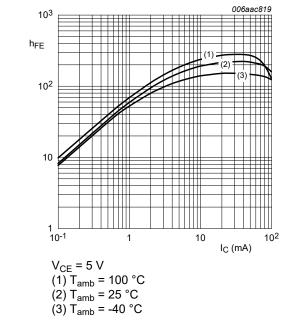


Fig. 3. DC current gain as a function of collector current; typical values

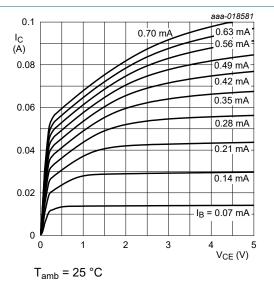
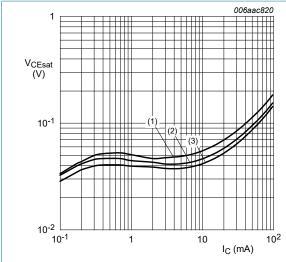


Fig. 4. Collector current as a function of collectoremitter voltage; typical values

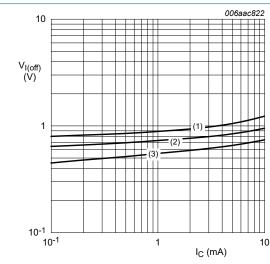
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 $I_{\rm C}/I_{\rm B} = 20$

(1) T_{amb} = 100 °C (2) T_{amb} = 25 °C (3) T_{amb} = -40 °C

Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values

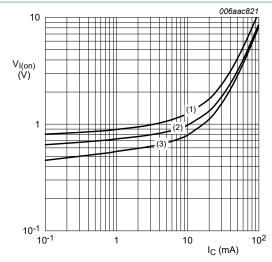


 $V_{CE} = 5 V$

(1) $T_{amb} = -40 \, ^{\circ}C$ (2) $T_{amb} = 25 \, ^{\circ}C$

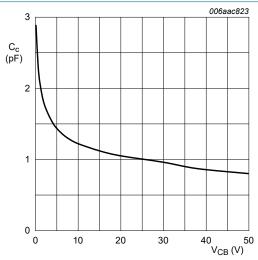
(3) $T_{amb} = 100 \, ^{\circ}C$

Fig. 7. Off-state input voltage as a function of collector current; typical values



V_{CE} = 0.3 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

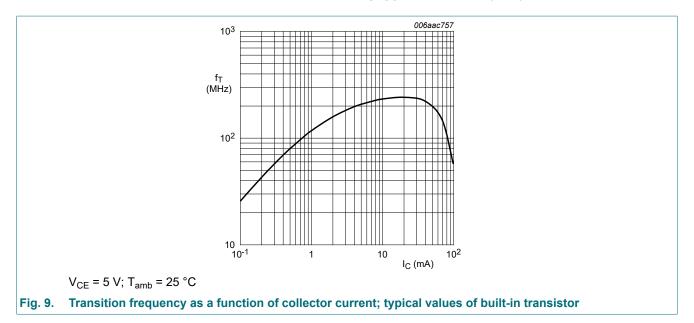
Fig. 6. On-state input voltage as a function of collector current; typical values



 $f = 1 MHz; T_{amb} = 25 °C$

Fig. 8. Collector capacitance as a function of collectorbase voltage; typical values

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11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

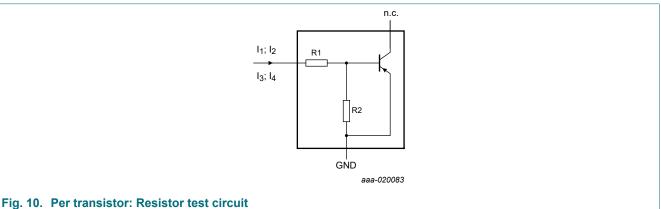
Resistor calculation

Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{I})}{I_{2} - I_{I}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I4) - V(I3)}{R1 \cdot (I4 - I3)} - 1$$



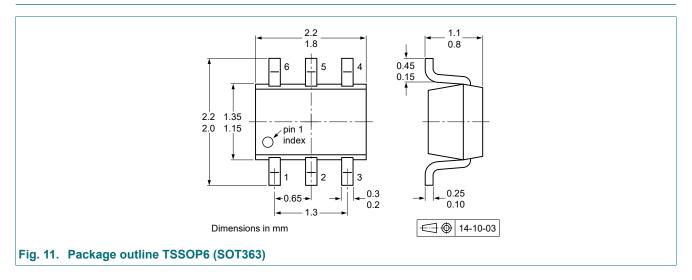
Resistor test conditions

Table 8. Resistor test conditions

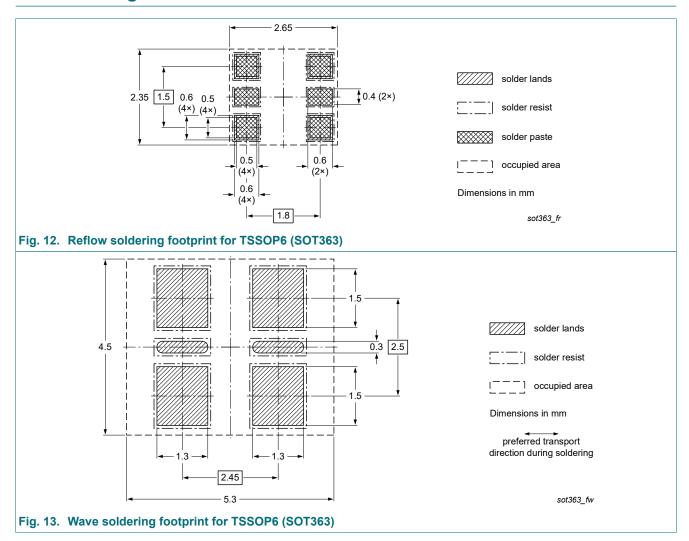
Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	l ₂	l ₃	14
PUMH13-Q	4.7	47	90 μΑ	140 µA	-55 µA	-105 µA

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12. Package outline



13. Soldering



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14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes			
PUMH13-Q v.2	20230515	Product data sheet	-	PUMH13-Q v.1			
Modifications:	Characteristics: I _C	Characteristics: I _{CEO} value corrected					
PUMH13-Q v.1	20220128	Product data sheet	-	-			

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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