

74HC4040; 74HCT4040

12-stage binary ripple counter

Rev. 8 — 16 February 2024

Product data sheet

1. General description

The 74HC4040; 74HCT4040 is a 12-stage binary ripple counter with a clock input (\overline{CP}), an overriding asynchronous master reset input (MR) and twelve parallel outputs (Q0 to Q11). The counter advances on the HIGH-to-LOW transition of \overline{CP} . A HIGH on MR clears all counter stages and forces all outputs LOW, independent of the state of \overline{CP} . Each counter stage is a static toggle flip-flop. Inputs include clamp diodes that enable the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- Input levels:
 - For 74HC4040: CMOS level
 - For 74HCT4040: TTL level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Applications

- Frequency dividing circuits
- Time delay circuits
- Control counters

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC4040D 74HCT4040D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC4040PW 74HCT4040PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HC4040BQ 74HCT4040BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

5. Functional diagram

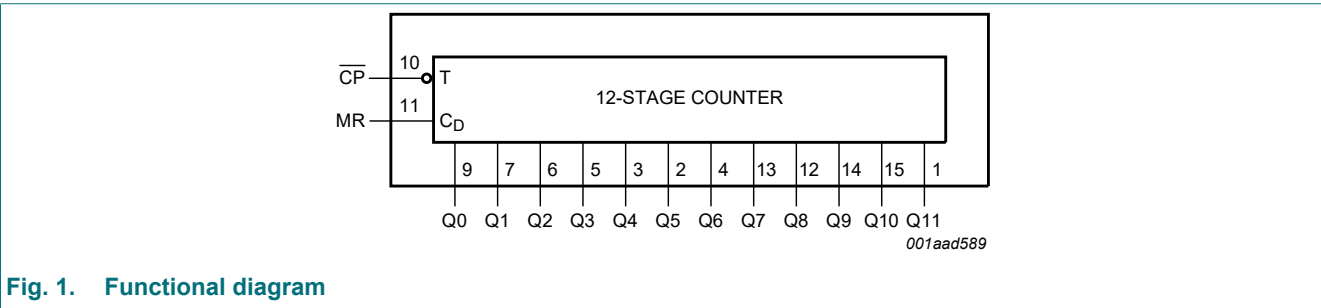
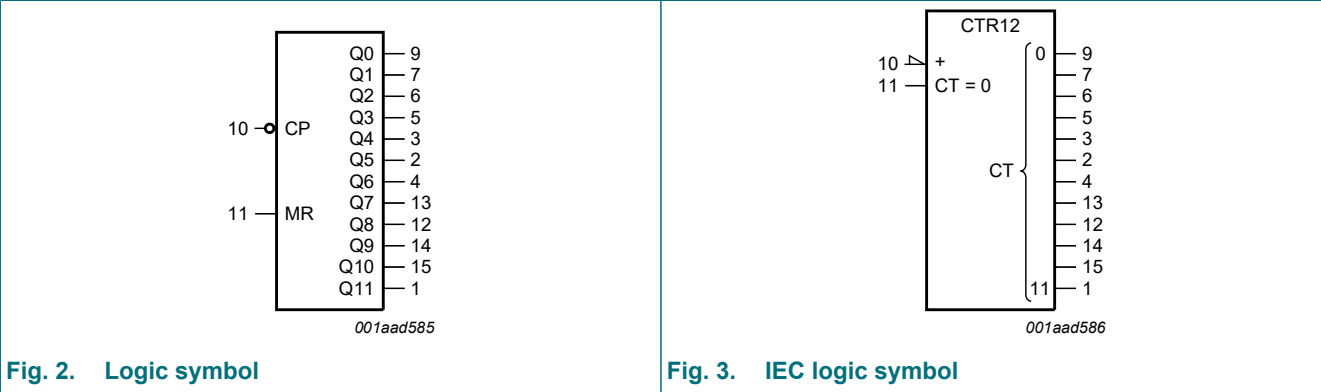


Fig. 1. Functional diagram



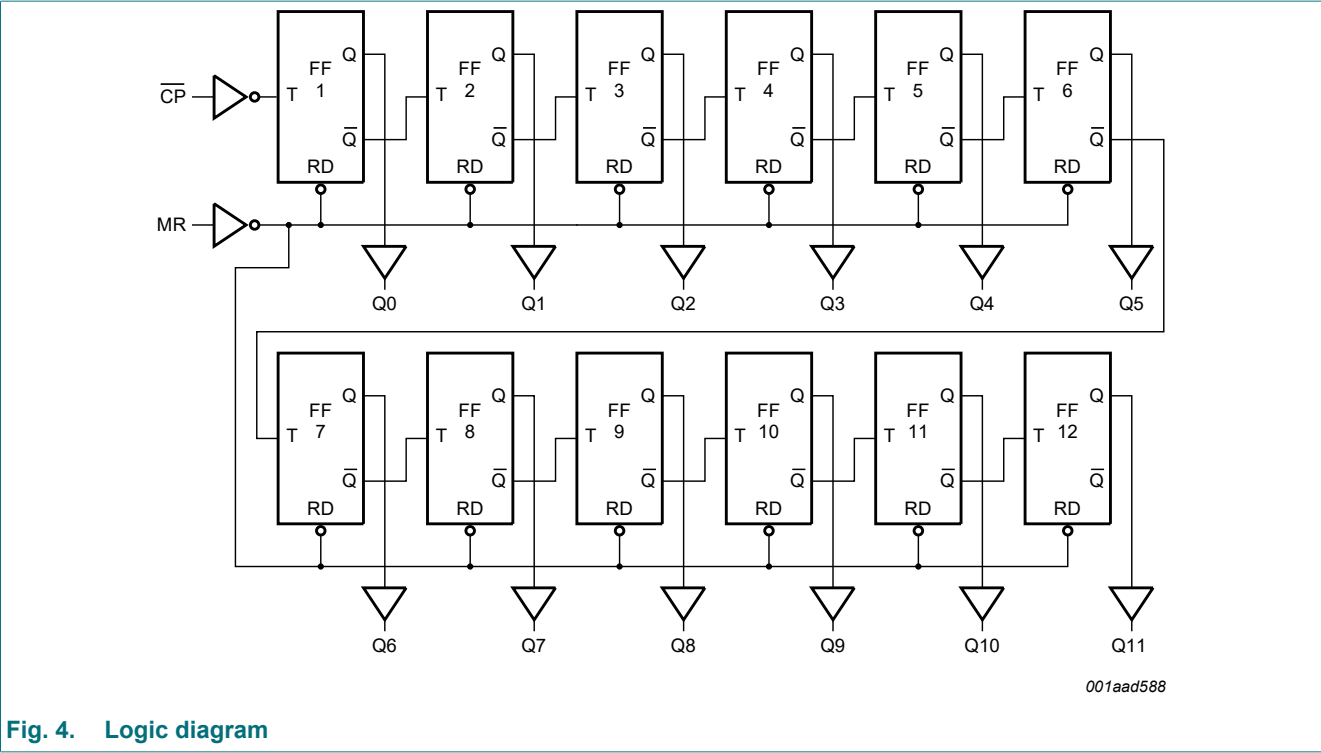
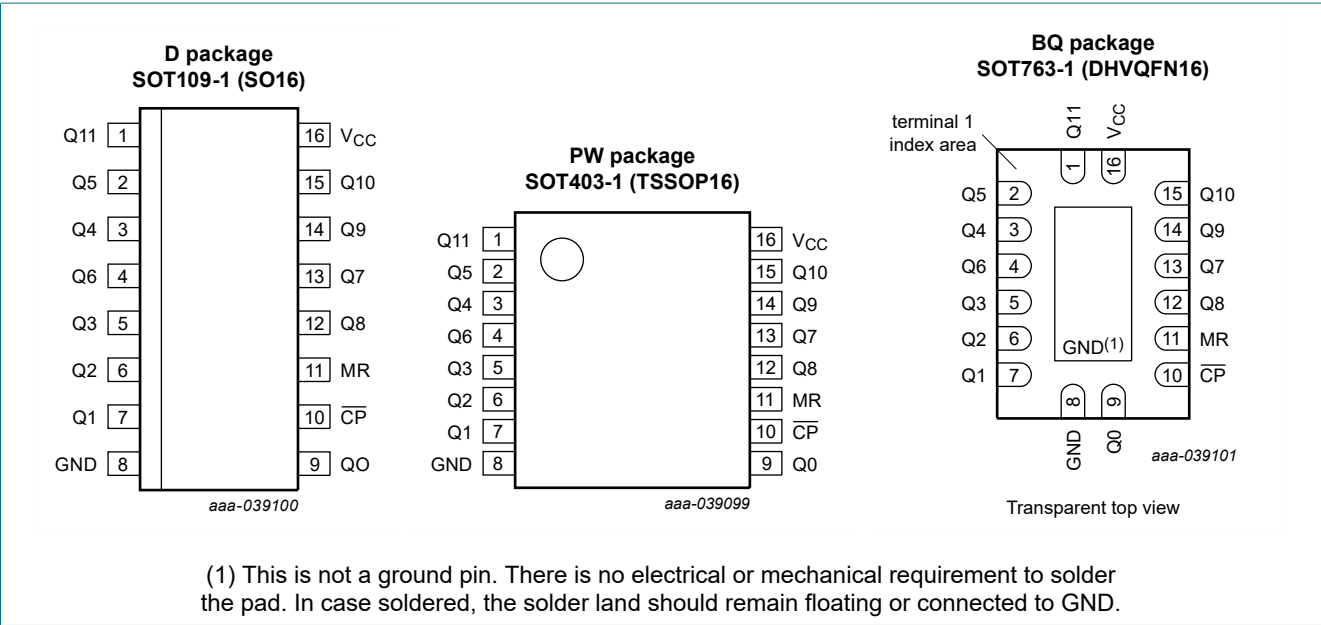


Fig. 4. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
Q11	1	output 11
Q5	2	output 5
Q4	3	output 4
Q6	4	output 6
Q3	5	output 3
Q2	6	output 2
Q1	7	output 1
GND	8	ground (0 V)
Q0	9	output 0
$\overline{\text{CP}}$	10	clock input (HIGH-to-LOW, edge-triggered)
MR	11	master reset input (active HIGH)
Q8	12	output 8
Q7	13	output 7
Q9	14	output 9
Q10	15	output 10
V _{CC}	16	positive supply voltage

7. Functional description

7.1. Function table

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = LOW-to-HIGH clock transition; ↓ = HIGH-to-LOW clock transition.

Input		Output
CP	MR	Q0 to Q11
↑	L	no change
↓	L	count
X	H	L

7.2. Timing diagram

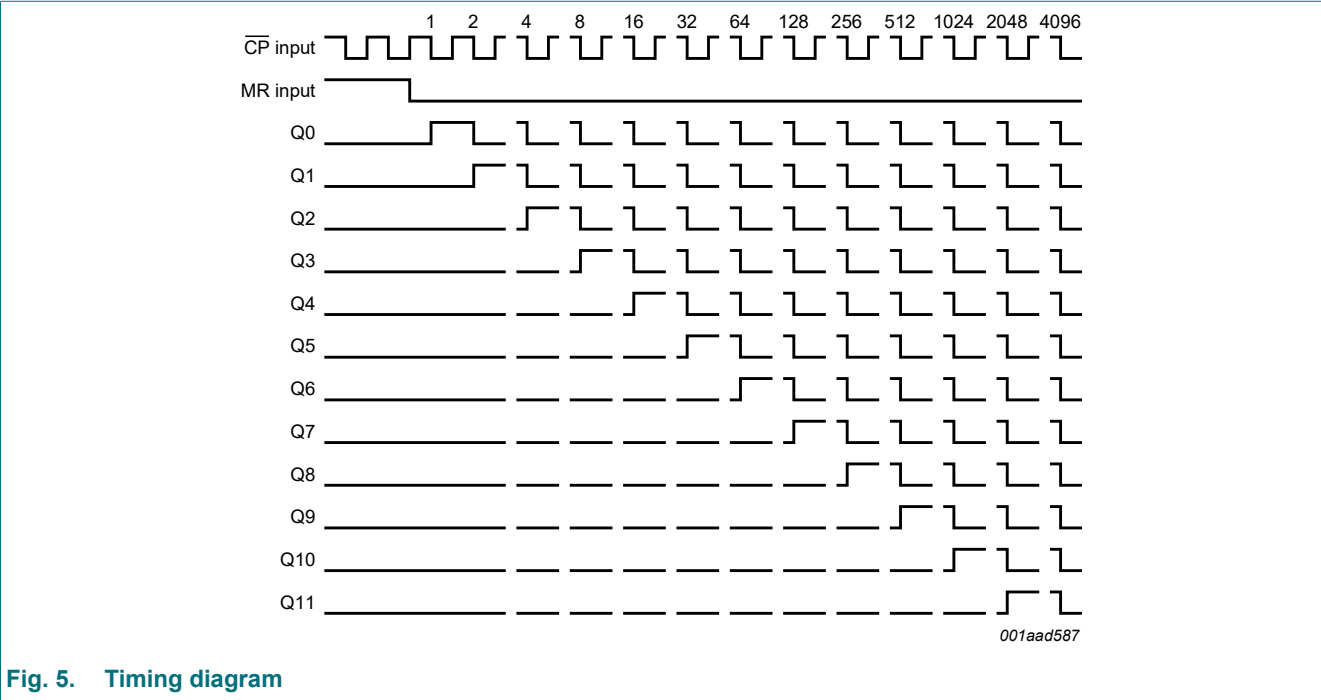


Fig. 5. Timing diagram

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_{OK}	output clamping current	$V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ [1]	-	±20	mA
I_O	output current	$-0.5\text{ V} < V_O < V_{CC} + 0.5\text{ V}$	-	±25	mA
I_{CC}	supply current		-	±50	mA
I_{GND}	ground current		-	±50	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40\text{ °C}$ to $+125\text{ °C}$ [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC4040			74HCT4040			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V _I	input voltage		0	-	V _{CC}	0	-	V _{CC}	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V _{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V _{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4040										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	1.2	-	1.5	-	1.5	-	V
		V _{CC} = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V _{CC} = 6.0 V	4.2	3.2	-	4.2	-	4.2	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	0.8	0.5	-	0.5	-	0.5	V
		V _{CC} = 4.5 V	-	2.1	1.35	-	1.35	-	1.35	V
		V _{CC} = 6.0 V	-	2.8	1.8	-	1.8	-	1.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -20 μA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -20 μA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -20 μA; V _{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I _O = -4.0 mA; V _{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I _O = -5.2 mA; V _{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 20 μA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 20 μA; V _{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I _O = 5.2 mA; V _{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C _I	input capacitance		-	3.5	-					pF

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HCT4040										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -20 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4 mA	3.98	4.32	-	3.84	-	3.7	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 20 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA	-	0.15	0.26	-	0.33	-	0.4	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	8.0	-	80	-	160	µA
ΔI _{CC}	additional supply current	per input pin; V _I = V _{CC} - 2.1 V; I _O = 0 A; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V								
		pin \overline{CP}	-	85	306	-	383	-	417	µA
		pin MR	-	110	396	-	495	-	539	µA
C _I	input capacitance		-	3.5	-	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC4040										
t _{pd}	propagation delay	CP to Q0; see Fig. 6 [1]								
		V _{CC} = 2.0 V	-	47	150	-	190	-	225	ns
		V _{CC} = 4.5 V	-	17	30	-	38	-	45	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	14	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	14	26	-	33	-	38	ns
		Qn to Qn+1; see Fig. 6								
		V _{CC} = 2.0 V	-	28	100	-	125	-	150	ns
		V _{CC} = 4.5 V	-	10	20	-	25	-	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	8	-	-	-	-	-	ns
		V _{CC} = 6.0 V	-	8	17	-	21	-	26	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V _{CC} = 2.0 V	-	61	185	-	230	-	280	ns
		V _{CC} = 4.5 V	-	22	37	-	46	-	56	ns
		V _{CC} = 6.0 V	-	18	31	-	39	-	48	ns
t _t	transition time	Qn; see Fig. 6 [2]								
		V _{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V _{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t _w	pulse width	CP input, HIGH or LOW; see Fig. 6								
		V _{CC} = 2.0 V	80	14	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	5	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	4	-	17	-	20	-	ns
		MR input, HIGH; see Fig. 6								
		V _{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V _{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V _{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t _{rec}	recovery time	MR to CP; see Fig. 6								
		V _{CC} = 2.0 V	50	8	-	65	-	75	-	ns
		V _{CC} = 4.5 V	10	3	-	13	-	15	-	ns
		V _{CC} = 6.0 V	9	2	-	11	-	13	-	ns
f _{max}	maximum frequency	CP input; see Fig. 6								
		V _{CC} = 2.0 V	6	27	-	4.8	-	4	-	MHz
		V _{CC} = 4.5 V	30	82	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	90	-	-	-	-	-	MHz
		V _{CC} = 6.0 V	35	98	-	28	-	24	-	MHz

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [3]	-	20	-	-	-	-	-	pF
74HCT4040										
t _{pd}	propagation delay	CP̄ to Q0; see Fig. 6 [1]								
		V _{CC} = 4.5 V	-	19	40	-	50	-	60	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	16	-	-	-	-	-	ns
		Qn to Qn+1; see Fig. 6								
		V _{CC} = 4.5 V	-	10	20	-	25	-	30	ns
		V _{CC} = 5.0 V; C _L = 15 pF	-	8	-	-	-	-	-	ns
t _{PHL}	HIGH to LOW propagation delay	MR to Qn; see Fig. 6								
		V _{CC} = 4.5 V	-	23	45	-	56	-	68	ns
t _t	transition time	Qn; see Fig. 6 [2]								
		V _{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t _W	pulse width	CP̄ input, HIGH or LOW; see Fig. 6								
		V _{CC} = 4.5 V	16	7	-	20	-	24	-	ns
		MR input, HIGH; see Fig. 6								
		V _{CC} = 4.5 V	16	6	-	20	-	24	-	ns
t _{rec}	recovery time	MR to CP̄; see Fig. 6								
		V _{CC} = 4.5 V	10	2	-	13	-	15	-	ns
f _{max}	maximum frequency	CP̄ input; see Fig. 6								
		V _{CC} = 4.5 V	30	72	-	24	-	20	-	MHz
		V _{CC} = 5.0 V; C _L = 15 pF	-	79	-	-	-	-	-	MHz
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} [3]	-	20	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL}, t_{PLH}.

[2] t_t is the same as t_{THL}, t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11.1. Waveforms and test circuit

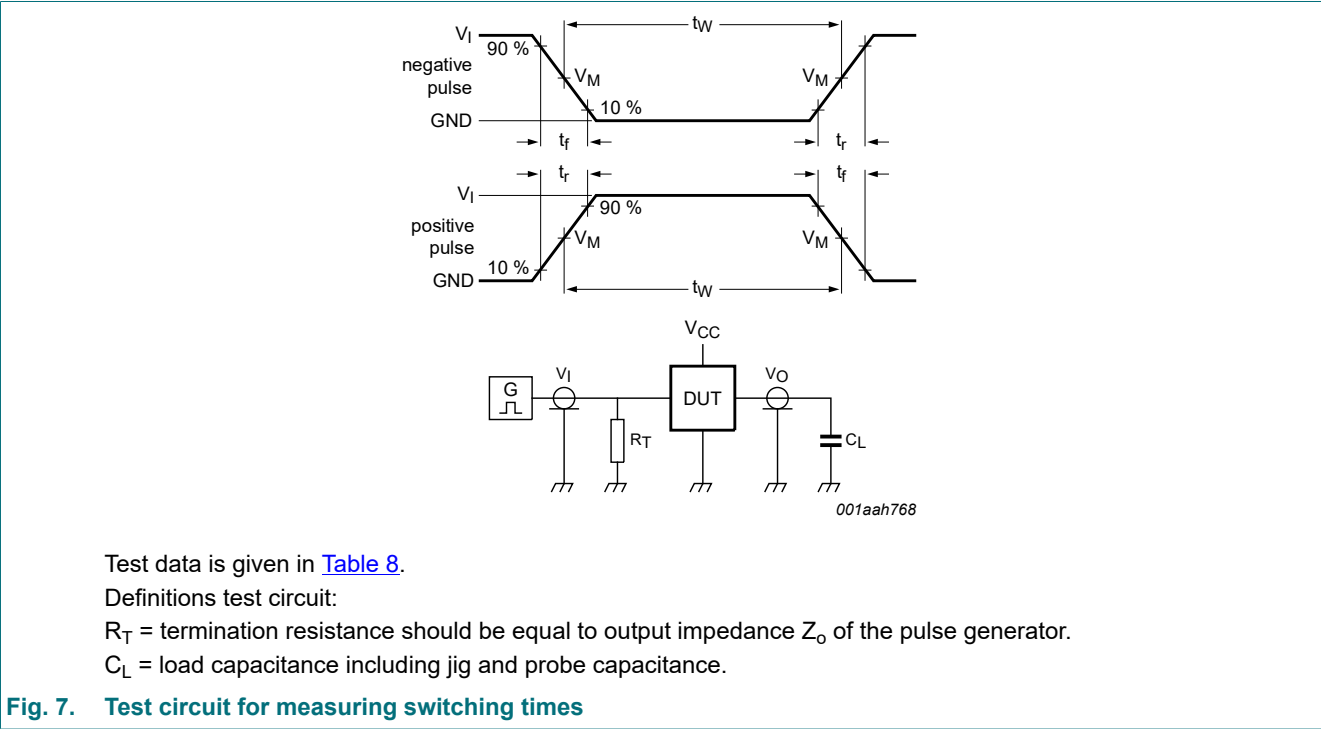
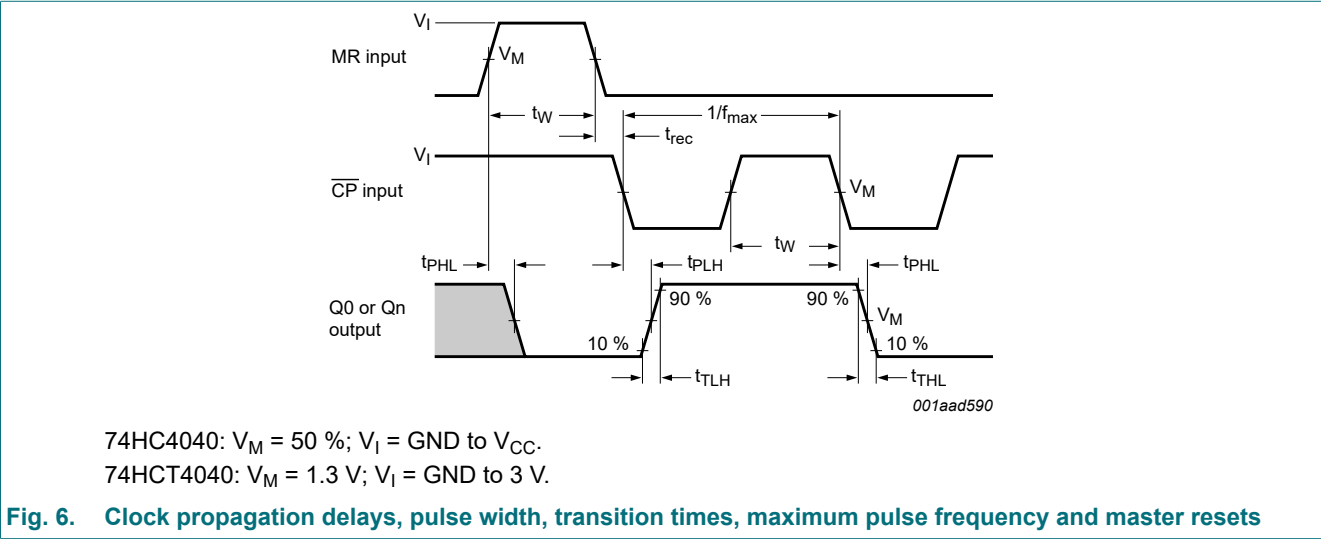


Table 8. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74HC4040	V_{CC}	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}
74HCT4040	3.0 V	6.0 ns	15 pF, 50 pF	t_{PLH}, t_{PHL}

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

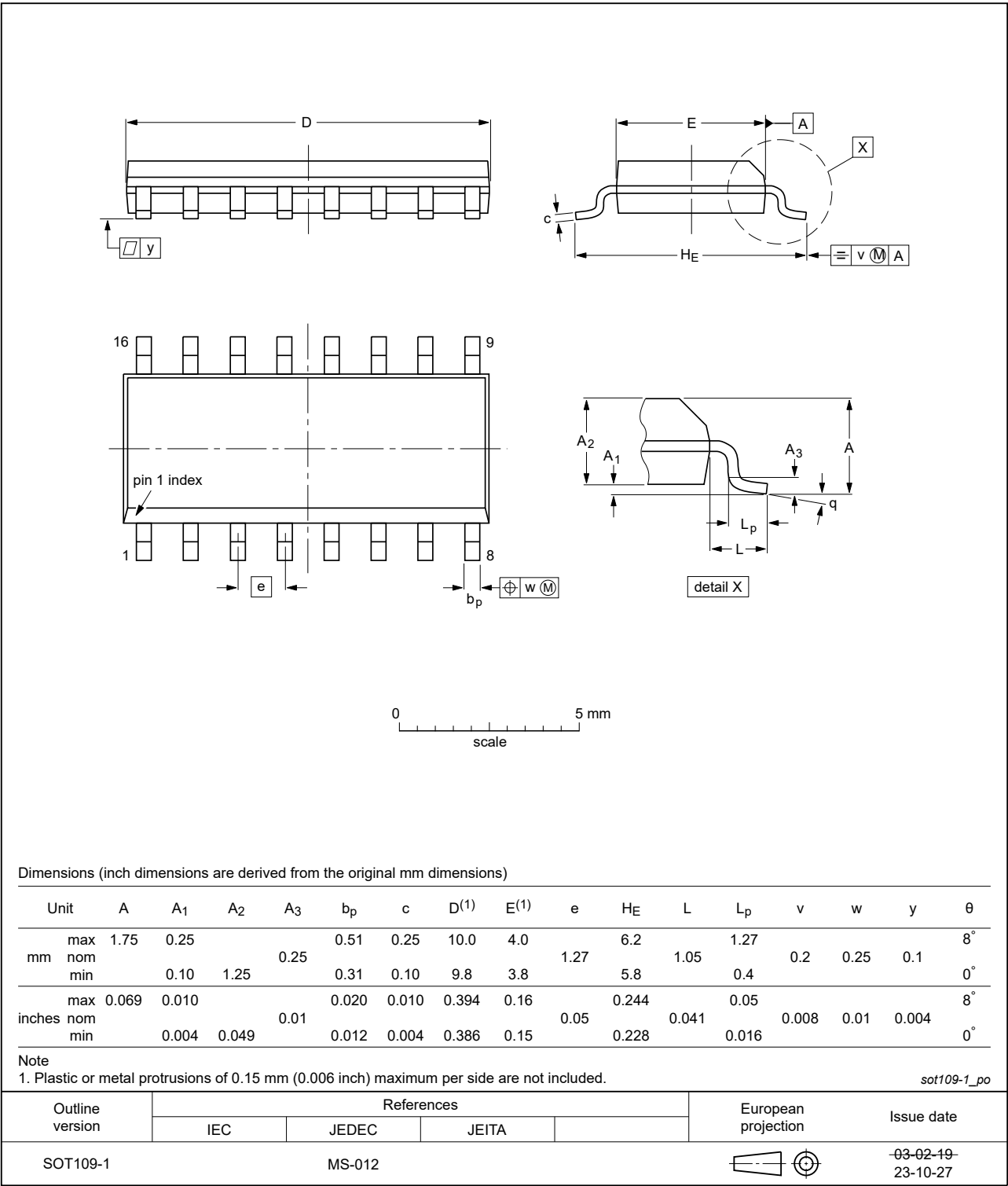


Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

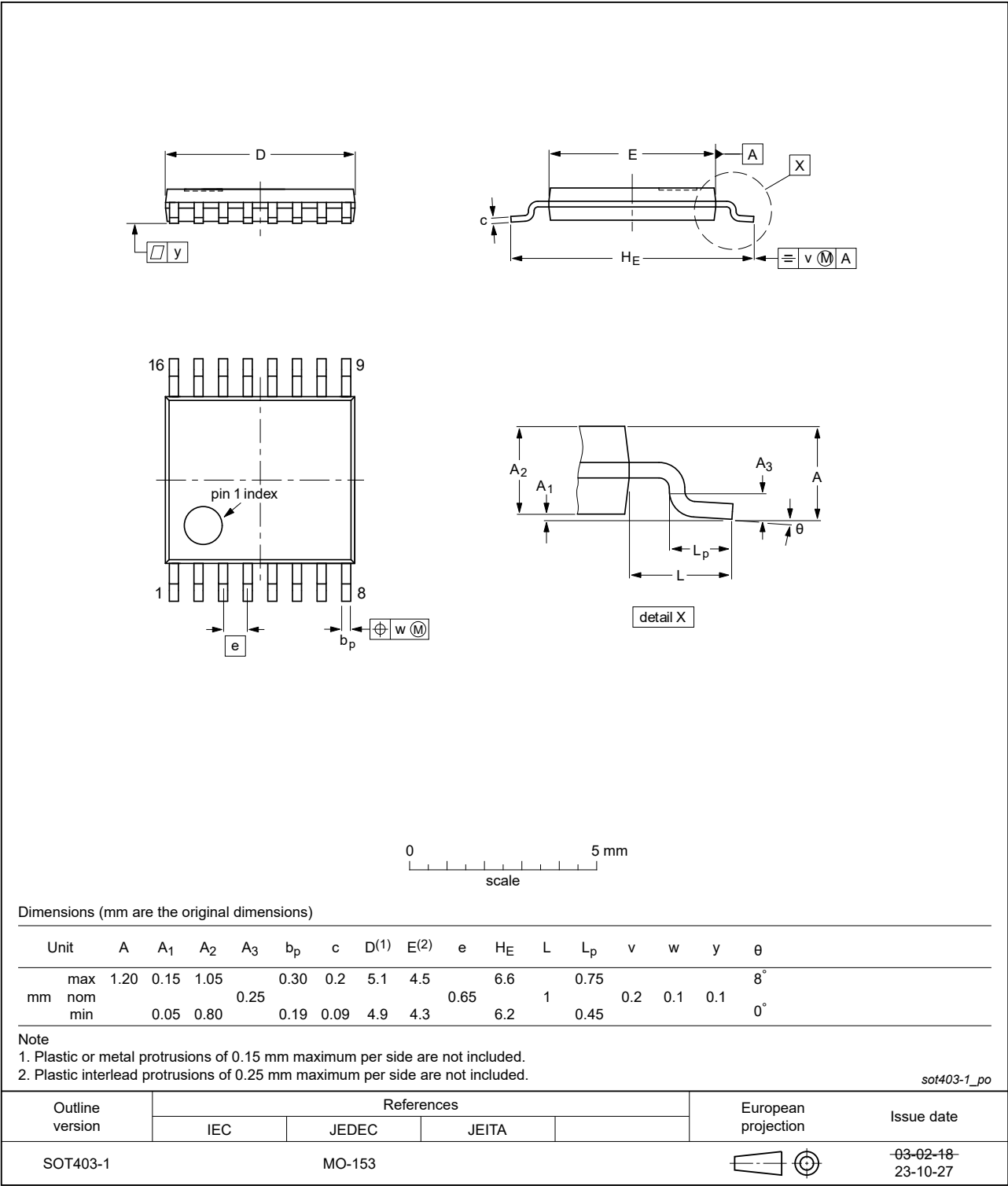


Fig. 9. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

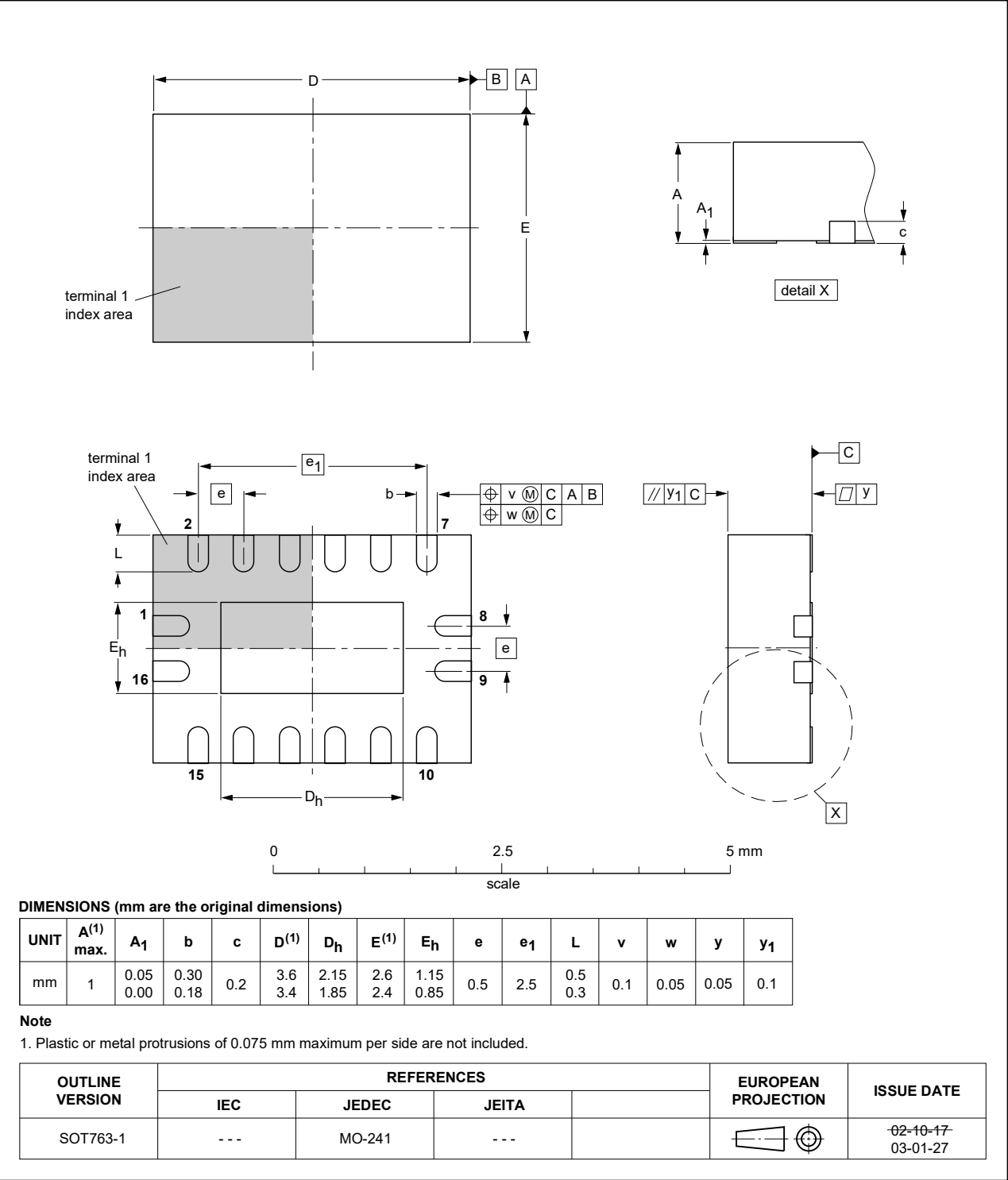


Fig. 10. Package outline SOT763-1 (DHVQFN16)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT4040 v.8	20240216	Product data sheet	-	74HC_HCT4040 v.7
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.Fig. 8 and Fig. 9: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74HC_HCT4040 v.7	20210526	Product data sheet	-	74HC_HCT4040 v.6
Modifications:	<ul style="list-style-type: none">Type number 74HCT4040DB (SOT338-1 / SSOP16) removed.			
74HC_HCT4040 v.6	20200608	Product data sheet	-	74HC_HCT4040 v.5
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Type number 74HC4040DB (SOT338-1/SSOP16) removed.Section 2 updated.Table 4: Derating values for P_{tot} total power dissipation have been updated.			
74HC_HCT4040 v.5	20160203	Product data sheet	-	74HC_HCT4040 v.4
Modifications:	<ul style="list-style-type: none">Type numbers 74HC4040N and 74HCT4040N (SOT38-4) removed.			
74HC_HCT4040 v.4	20140320	Product data sheet	-	74HC_HCT4040 v.3
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.Legal texts have been adapted to the new company name where appropriate.			
74HC_HCT4040 v.3	20050914	Product data sheet	-	74HC_HCT4040_CNV v.2
74HC_HCT4040_CNV v.2	19901231	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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