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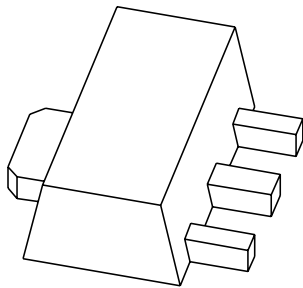
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Kind regards,

Team Nexperia

DATA SHEET



PBSS4480X

80 V, 4 A

NPN low V_{CEsat} (BISS) transistor

Product data sheet
Supersedes data of 2004 Aug 5

2004 Oct 25

80 V, 4 A

NPN low V_{CEsat} (BISS) transistor

PBSS4480X**FEATURES**

- High h_{FE} and low V_{CEsat} at high current operation
- High collector current capability: I_C maximum 4 A
- High efficiency leading to less heat generation.

APPLICATIONS

- Medium power peripheral drivers; e.g. fan, motor
- Strobe flash units for DSC and mobile phones
- Inverter applications; e.g. TFT displays
- Power switch for LAN and ADSL systems
- Medium power DC-to-DC conversion
- Battery chargers.

DESCRIPTION

NPN low V_{CEsat} transistor in a SOT89 (SC-62) plastic package.

PNP complement: PBSS5480X.

MARKING

TYPE NUMBER	MARKING CODE ⁽¹⁾
PBSS4480X	*1Y

Note

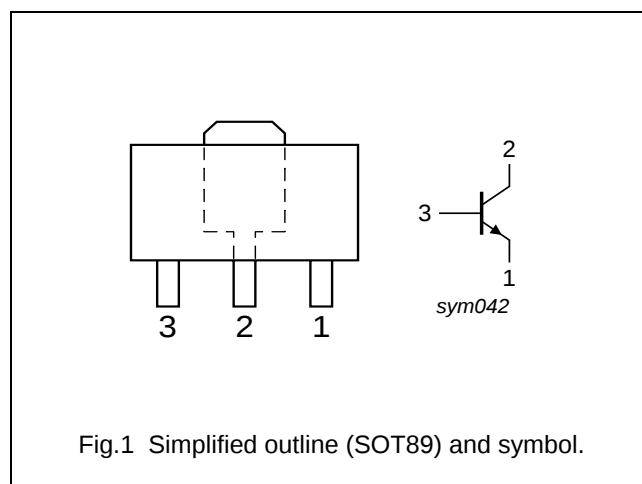
- * = p: made in Hong Kong.
* = t: made in Malaysia.
* = W: made in China.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{CEO}	collector-emitter voltage	80	V
I_C	collector current (DC)	4	A
I_{CM}	peak collector current	10	A
R_{CEsat}	equivalent on-resistance	54	mΩ

PINNING

PIN	DESCRIPTION
1	emitter
2	collector
3	base

**ORDERING INFORMATION**

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PBSS4480X	—	plastic surface mounted package; collector pad for good heat transfer; 3 leads	SOT89

80 V, 4 A NPN low V_{CEsat} (BISS) transistor

PBSS4480X

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

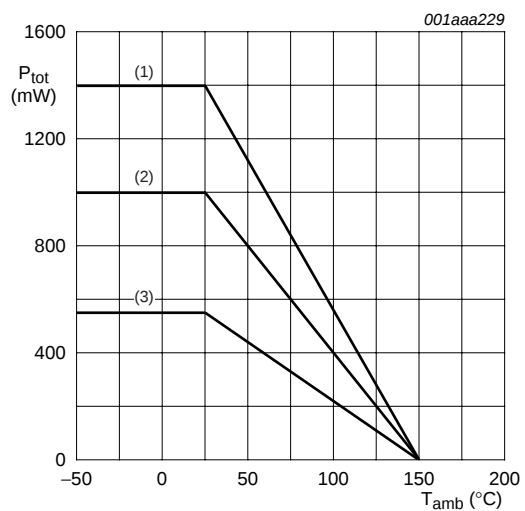
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	80	V
V_{CEO}	collector-emitter voltage	open base	–	80	V
V_{EBO}	emitter-base voltage	open collector	–	5	V
I_C	collector current (DC)	note 4	–	4	A
I_{CRM}	repetitive peak collector current	$t_p \leq 10$ ms; $\delta \leq 0.1$	–	6	A
I_{CM}	peak collector current	$t = 1$ ms or limited by $T_{j(max)}$	–	10	A
I_B	base current (DC)		–	1	A
I_{BM}	peak base current	$t \leq 300$ μ s	–	2	A
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C			
		notes 1 and 2	–	2.5	W
		note 2	–	550	mW
		note 3	–	1	W
		note 4	–	1.4	W
		note 5	–	1.6	W
T_j	junction temperature		–	150	°C
T_{amb}	ambient temperature		–65	+150	°C
T_{stg}	storage temperature		–65	+150	°C

Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see "Thermal considerations for SOT89 in the General Part of associated Handbook".

80 V, 4 A NPN low V_{CEsat} (BISS) transistor

PBSS4480X



- (1) FR4 PCB; 6 cm² mounting pad for collector.
- (2) FR4 PCB; 1 cm² mounting pad for collector.
- (3) FR4; standard footprint.

Fig.2 Power derating curves.

80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

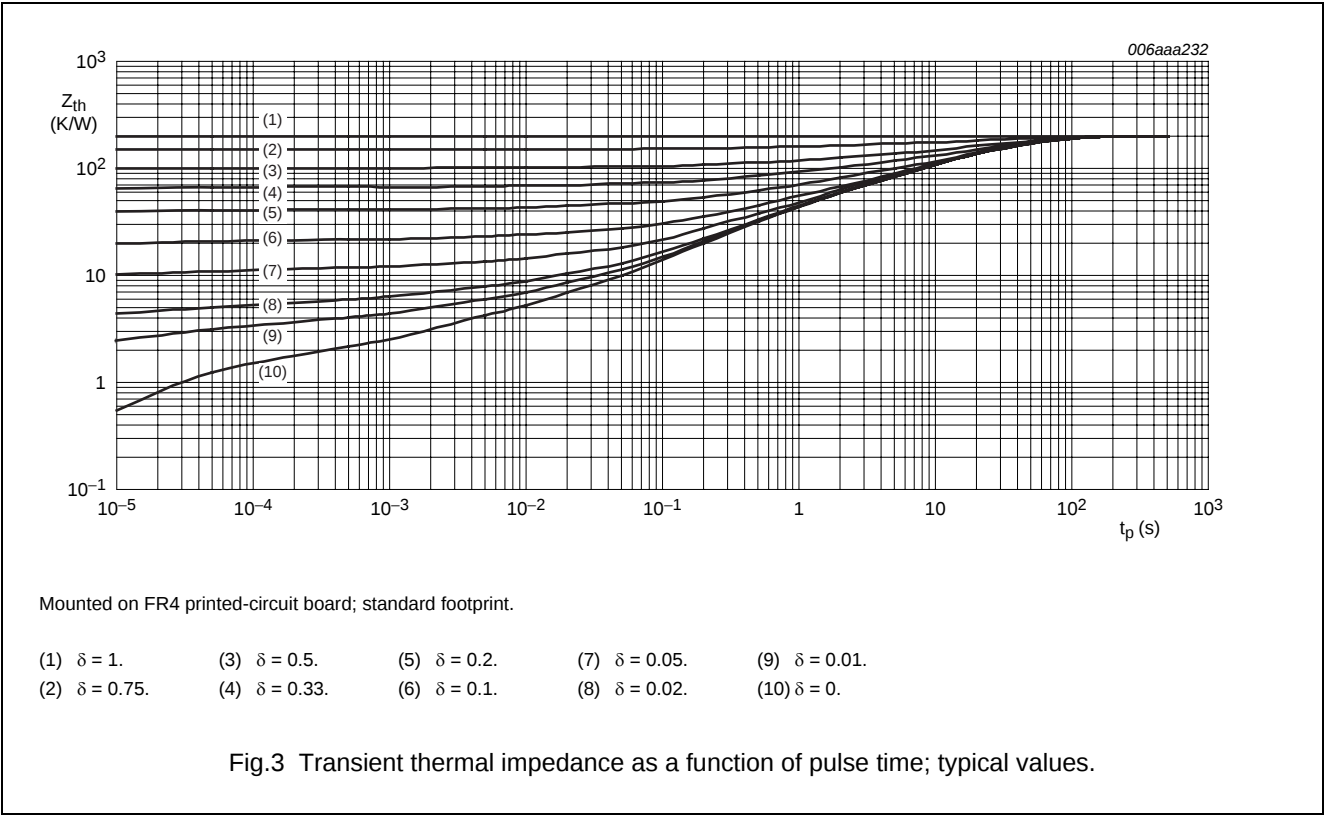
PBSS4480X

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		
		notes 1 and 2	50	K/W
		note 2	225	K/W
		note 3	125	K/W
		note 4	90	K/W
		note 5	80	K/W
$R_{th(j-s)}$	thermal resistance from junction to soldering point		16	K/W

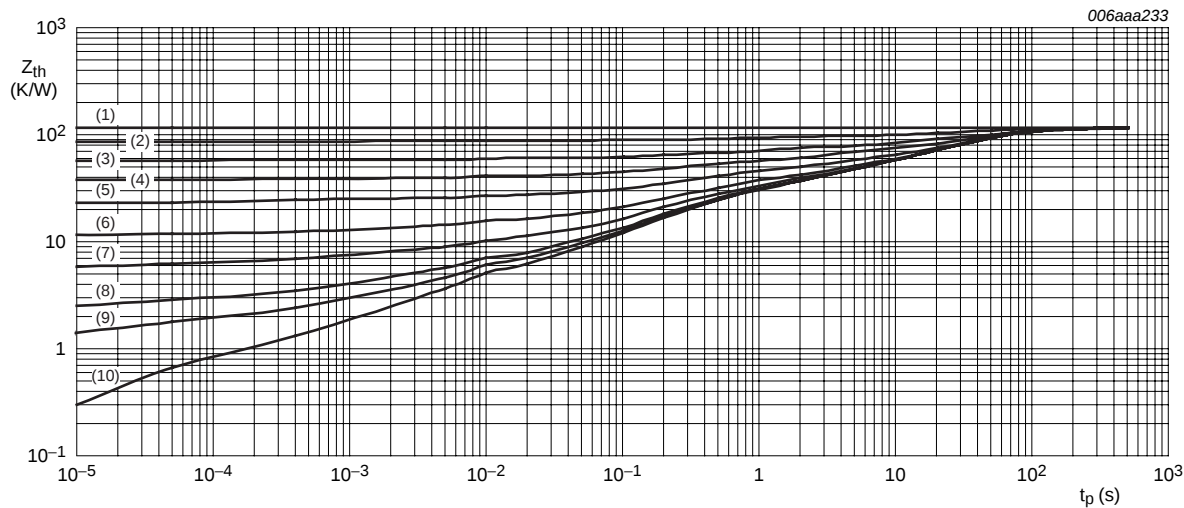
Notes

1. Operated under pulsed conditions; pulse width $t_p \leq 10$ ms; duty cycle $\delta \leq 0.2$.
2. Device mounted on a printed-circuit board, single-sided copper, tin-plated and standard footprint.
3. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 1 cm².
4. Device mounted on a printed-circuit board, single-sided copper, tin-plated and mounting pad for collector 6 cm².
5. Device mounted on a 7 cm² ceramic printed-circuit board, 1 cm² single-sided copper and tin-plated. For other mounting conditions, see “Thermal considerations for SOT89 in the General Part of associated Handbook”.



80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

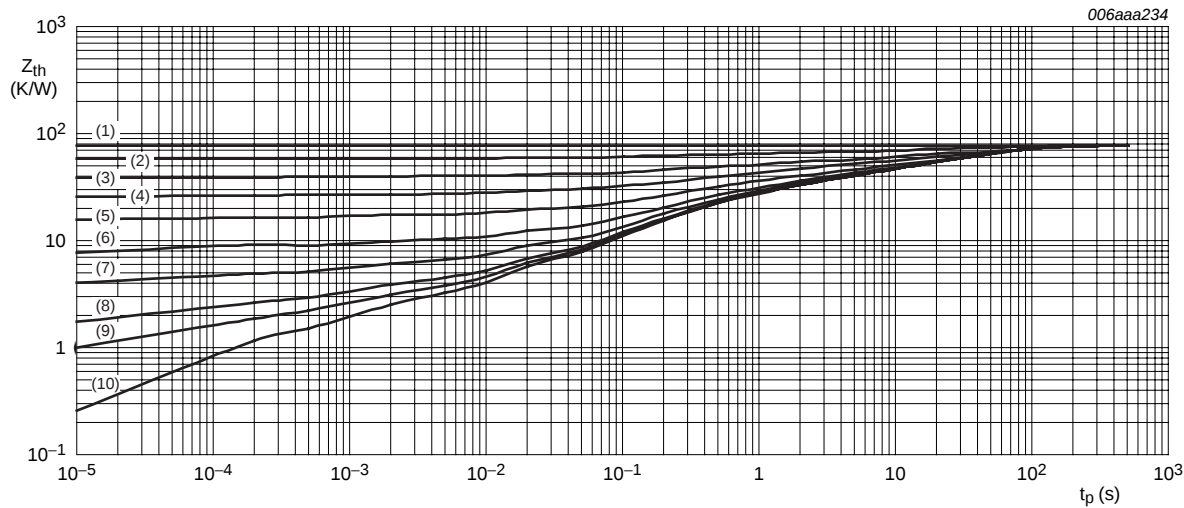
PBSS4480X



Mounted on FR4 printed-circuit board; mounting pad for collector 1 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.4 Transient thermal impedance as a function of pulse time; typical values.



Mounted on FR4 printed-circuit board; mounting pad for collector 6 cm².

- | | | | | |
|----------------------|----------------------|---------------------|----------------------|----------------------|
| (1) $\delta = 1.$ | (3) $\delta = 0.5.$ | (5) $\delta = 0.2.$ | (7) $\delta = 0.05.$ | (9) $\delta = 0.01.$ |
| (2) $\delta = 0.75.$ | (4) $\delta = 0.33.$ | (6) $\delta = 0.1.$ | (8) $\delta = 0.02.$ | (10) $\delta = 0.$ |

Fig.5 Transient thermal impedance as a function of pulse time; typical values.

80 V, 4 A

NPN low V_{CEsat} (BISS) transistor

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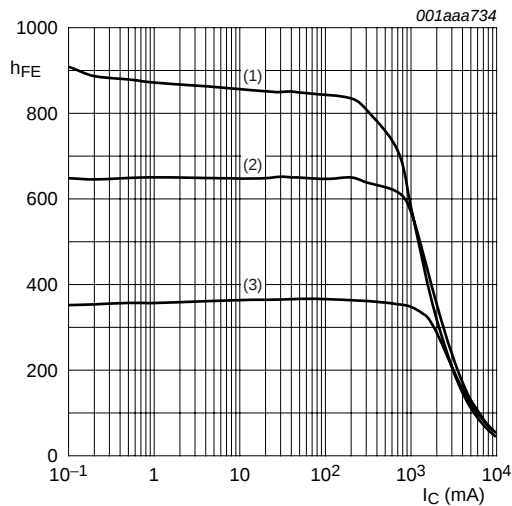
CHARACTERISTICS $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{CB} = 80\text{ V}; I_E = 0\text{ A}$	—	—	100	nA
		$V_{CB} = 80\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$	—	—	50	μA
I_{CES}	collector-emitter cut-off current	$V_{CE} = 80\text{ V}; V_{BE} = 0\text{ V}$	—	—	100	nA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	—	—	100	nA
h_{FE}	DC current gain	$V_{CE} = 2\text{ V}; I_C = 0.5\text{ A}$	250	400	—	—
		$V_{CE} = 2\text{ V}; I_C = 1\text{ A}; \text{note 1}$	250	400	—	—
		$V_{CE} = 2\text{ V}; I_C = 2\text{ A}; \text{note 1}$	175	270	—	—
		$V_{CE} = 2\text{ V}; I_C = 4\text{ A}; \text{note 1}$	80	140	—	—
V_{CEsat}	collector-emitter saturation voltage	$I_C = 0.5\text{ A}; I_B = 50\text{ mA}$	—	25	40	mV
		$I_C = 1\text{ A}; I_B = 50\text{ mA}$	—	55	80	mV
		$I_C = 2\text{ A}; I_B = 40\text{ mA}$	—	110	160	mV
		$I_C = 4\text{ A}; I_B = 200\text{ mA}; \text{note 1}$	—	170	230	mV
		$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	—	200	270	mV
R_{CEsat}	equivalent on-resistance	$I_C = 5\text{ A}; I_B = 500\text{ mA}; \text{note 1}$	—	40	54	$\text{m}\Omega$
V_{BEsat}	base-emitter saturation voltage	$I_C = 0.5\text{ A}; I_B = 50\text{ mA}$	—	0.78	0.85	V
		$I_C = 1\text{ A}; I_B = 50\text{ mA}$	—	0.79	0.9	V
		$I_C = 1\text{ A}; I_B = 100\text{ mA}; \text{note 1}$	—	0.82	0.95	V
		$I_C = 4\text{ A}; I_B = 400\text{ mA}; \text{note 1}$	—	0.95	1.05	V
V_{BEon}	base-emitter turn-on voltage	$I_C = 2\text{ A}; V_{CE} = 2\text{ V}$	—	0.78	0.85	V
f_T	transition frequency	$I_C = 100\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$	120	150	—	MHz
C_c	collector capacitance	$I_E = I_C = 0\text{ A}; V_{CB} = 10\text{ V}; f = 1\text{ MHz}$	—	35	50	pF

Note1. Pulse test: $t_p \leq 300\text{ }\mu\text{s}$; $\delta \leq 0.02$.

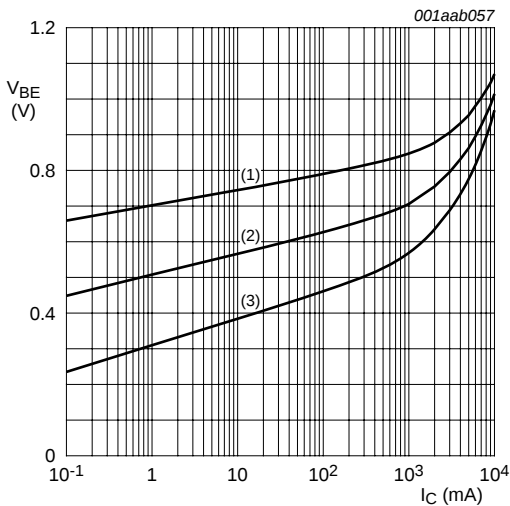
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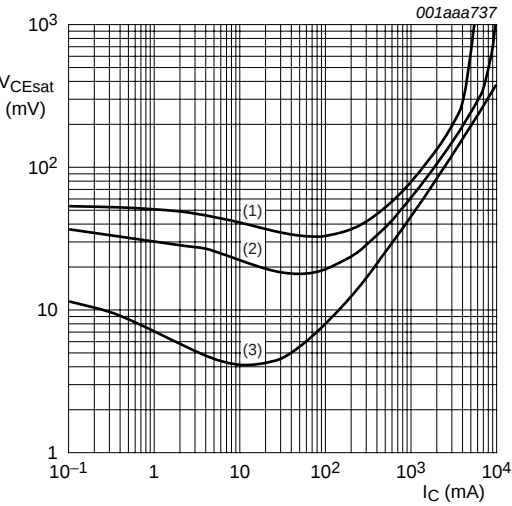
$V_{CE} = 2\text{ V}$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = -55^\circ\text{C}$.

Fig.6 DC current gain as a function of collector current; typical values.



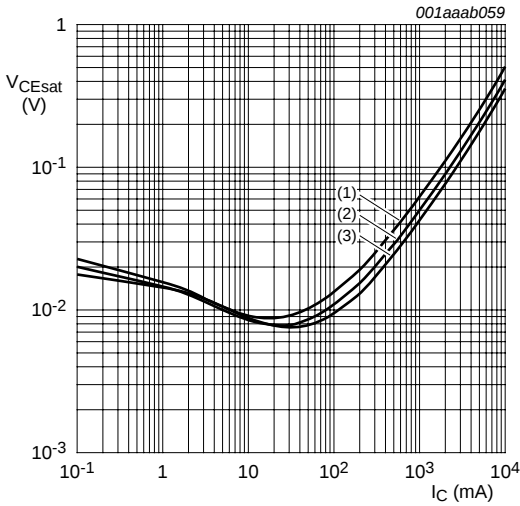
$V_{CE} = 2\text{ V}$.
(1) $T_{amb} = -55^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = 100^\circ\text{C}$.

Fig.7 Base-emitter voltage as a function of collector current; typical values.



(1) $I_C/I_B = 100$.
(2) $I_C/I_B = 50$.
(3) $I_C/I_B = 10$.

Fig.8 Collector-emitter saturation voltage as a function of collector current; typical values.

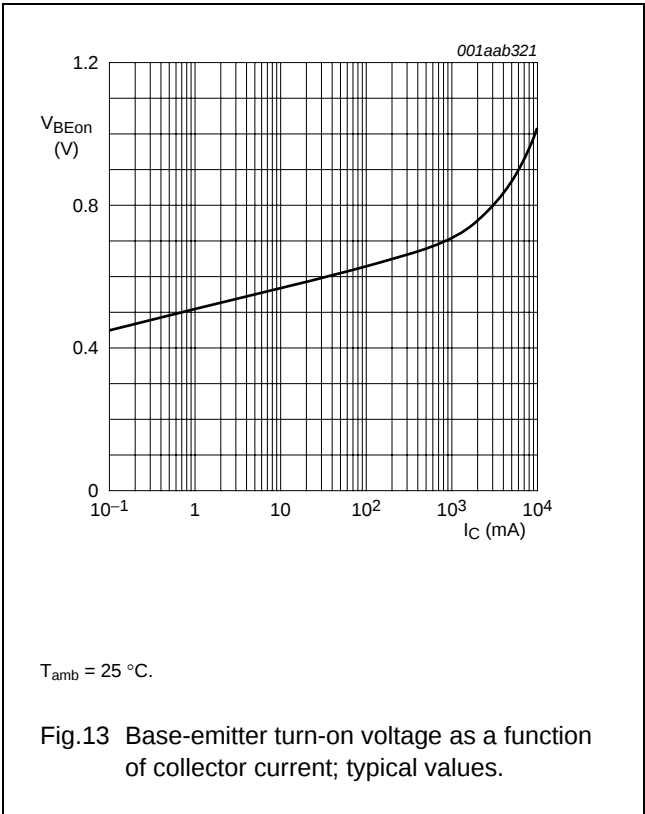
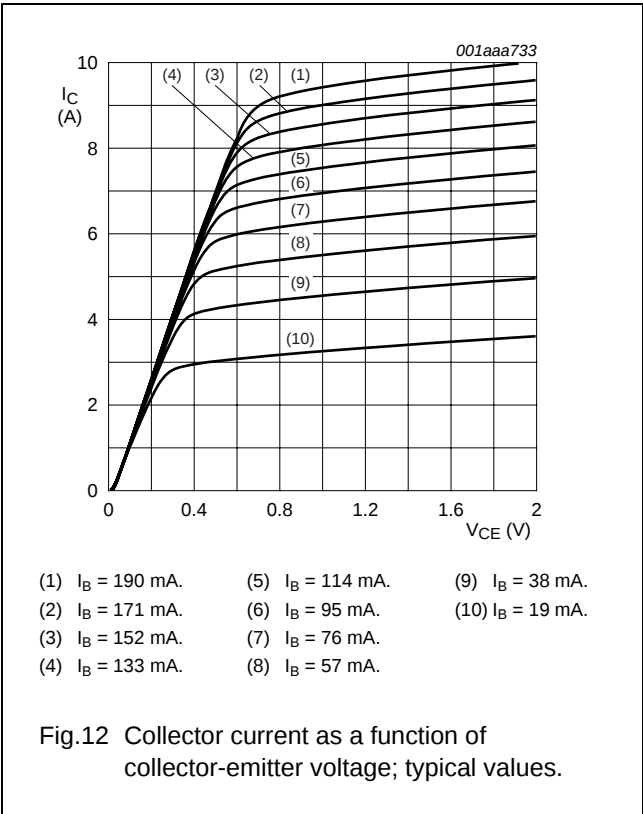
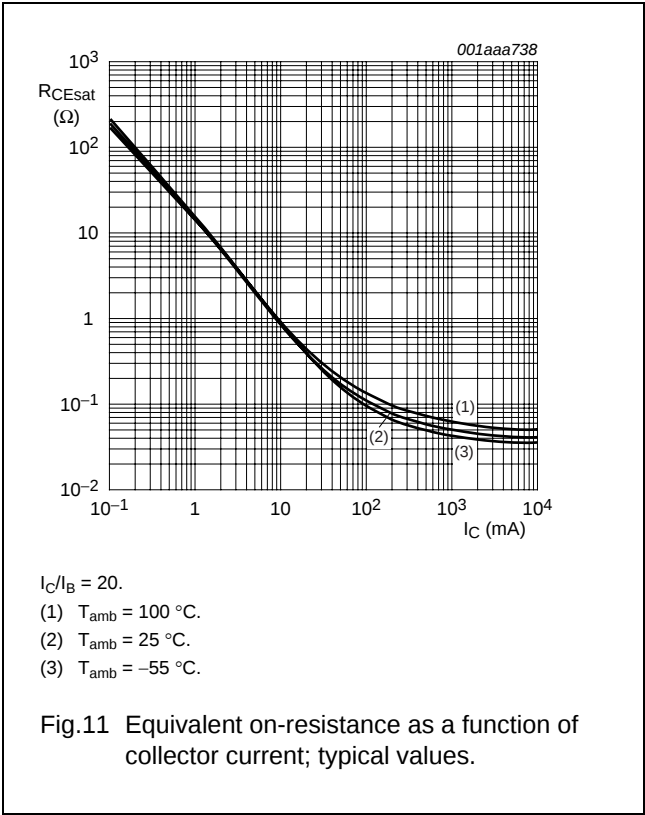
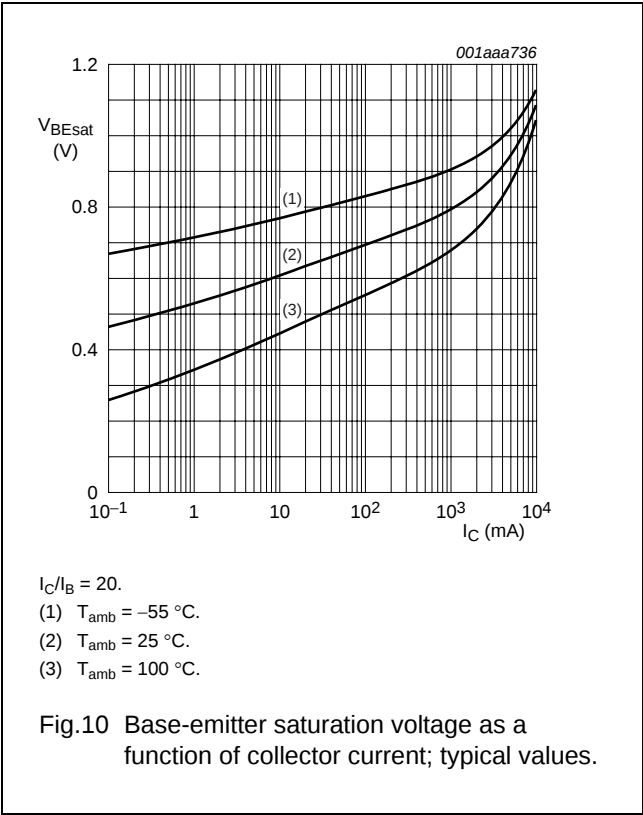


$I_C/I_B = 20$.
(1) $T_{amb} = 100^\circ\text{C}$.
(2) $T_{amb} = 25^\circ\text{C}$.
(3) $T_{amb} = -55^\circ\text{C}$.

Fig.9 Collector-emitter saturation voltage as a function of collector current; typical values.

80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

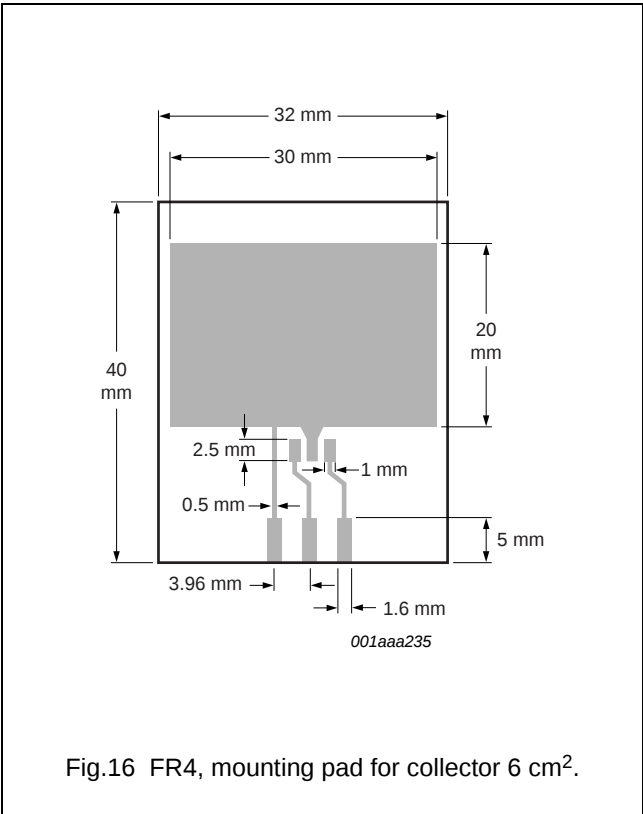
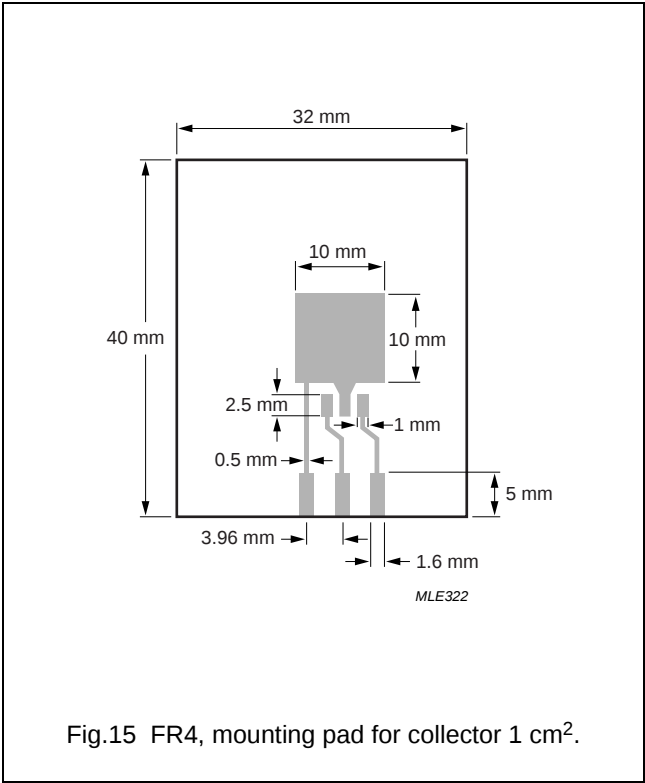
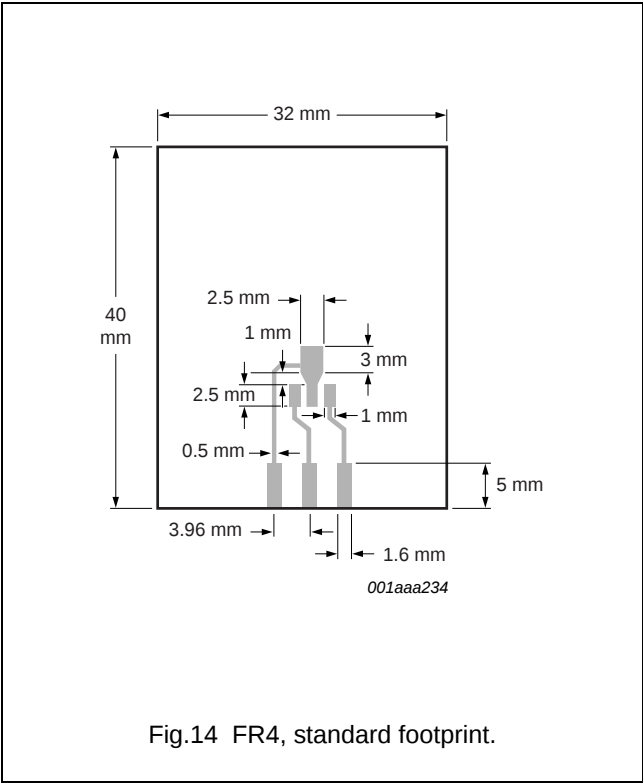
PBSS4480X



80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

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Reference mounting conditions



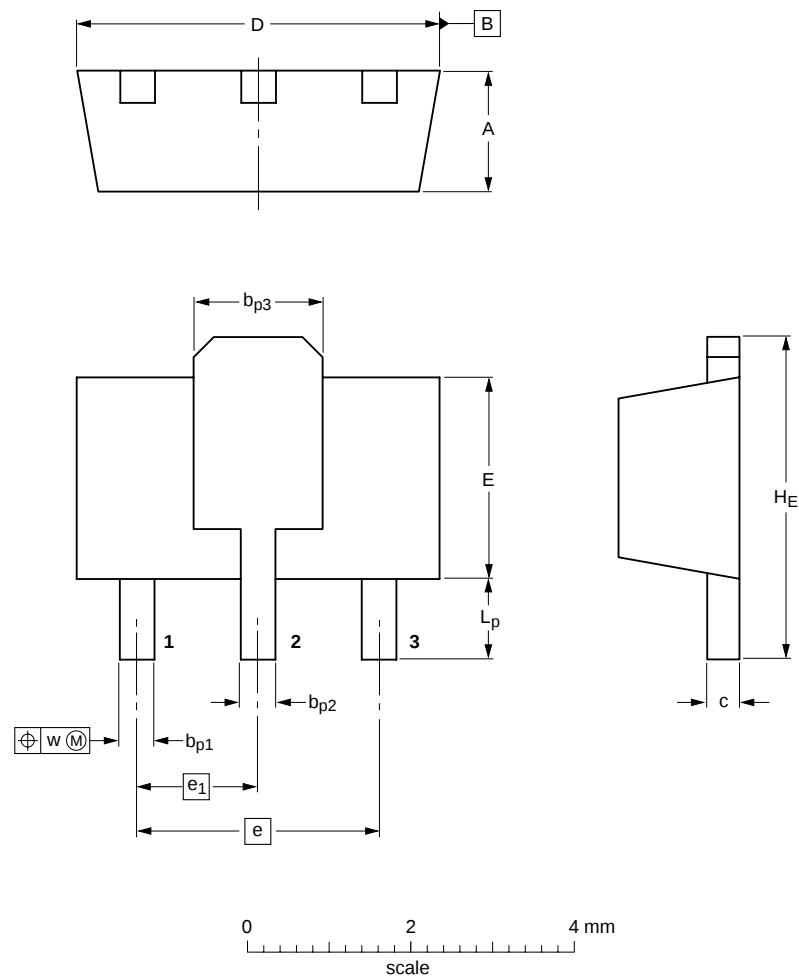
80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

PBSS4480X

PACKAGE OUTLINE

Plastic surface-mounted package; collector pad for good heat transfer; 3 leads

SOT89



DIMENSIONS (mm are the original dimensions)

UNIT	A	b _{p1}	b _{p2}	b _{p3}	c	D	E	e	e ₁	H _E	L _p	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.23	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	1.2 0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT89		TO-243	SC-62			04-08-03 06-03-16

80 V, 4 A
NPN low V_{CEsat} (BISS) transistor

PBSS4480X

DATA SHEET STATUS

DOCUMENT STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

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NXP Semiconductors

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Contact information

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