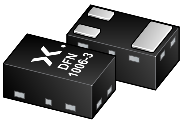


# PESD5V0C2UM-Q

## Extremely low capacitance unidirectional ESD protection diode array

25 May 2022

Product data sheet

## 1. General description

Extremely low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode array, part of the TrEOS protection family. This device is housed in a DFN1006-3 (SOT883-2) leadless ultra small Surface-Mounted Device (SMD) plastic package, designed to protect up to two signal lines from the damage caused by ESD and other transients.

## 2. Features and benefits

- Unidirectional ESD protection of one line pair
- $V_{RWM}$ = 5 V device
- Very high surge robustness of 6.5 A for a 8/20 μs pulse
- Very low diode capacitance: $C_d$ = 0.5 pF typical
- Extremely low clamping voltage to protect sensitive I/Os
- ESD protection up to ±15 kV according to IEC 61000-4-2
- Leadless ultra small SOT883-2 surface mount package
- IEC61000-4-4 robust up to level 4 (corresponds to 40 A into a 50 Ohm termination)
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

ESD protection for in-vehicle network lines in automotive environments

- High-speed data lines such USB2.0 and USB3.0 up to 5 Gbps
- Low-Voltage Differential Signaling (LVDS) automotive
- Automotive A/V monitors, display and cameras

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{RWM}$ | reverse standoff voltage | | [1] | - | - | 5 | V |
| $C_d$ | diode capacitance | f = 1 MHz; $V_R$ = 0 V; $T_{amb}$ = 25 °C | [1] | - | 0.5 | 0.6 | pF |

[1] Measured from pin 1 or 2 to pin 3.

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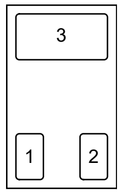
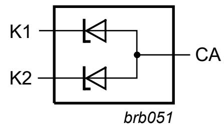
# 5. Pinning information

**Table 2. Pinning information**

<table>
<tr><th>Pin</th><th>Symbol</th><th>Description</th><th>Simplified outline</th><th>Graphic symbol</th></tr>
<tr><td>1</td><td>K1</td><td>cathode (diode 1)</td><td rowspan="3">

Transparent top view
DFN1006-3 (SOT883-2)</td><td rowspan="3">
</td></tr>
<tr><td>2</td><td>K2</td><td>cathode (diode 2)</td></tr>
<tr><td>3</td><td>CA</td><td>common anode</td></tr>
</table>

# 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| PESD5V0C2UM-Q | DFN1006-3 | Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.47 mm | SOT883-2 |

# 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| PESD5V0C2UM-Q | 6B |

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{RWM}$ | reverse standoff voltage | | [1] | - | 5 | V |
| $I_{PPM}$ | rated peak pulse current | $t_p$ = 8/20 µs | [1] [2] | -6.5 | 6.5 | A |
| $T_{amb}$ | ambient temperature | | | -55 | 150 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 150 | °C |
| **ESD maximum ratings** | | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | IEC 61000-4-2; contact discharge | [1] [3] | -15 | 15 | kV |
| | | IEC 61000-4-2; air discharge | [1] [3] | -15 | 15 | kV |

[1] Measured from pin 1 or 2 to pin 3.
[2] Non-repetitive current pulse 8/20 µs exponentially descaying waveform according to IEC 61000-4-5.
[3] Device stressed with ten non-repetitive ESD pulses.

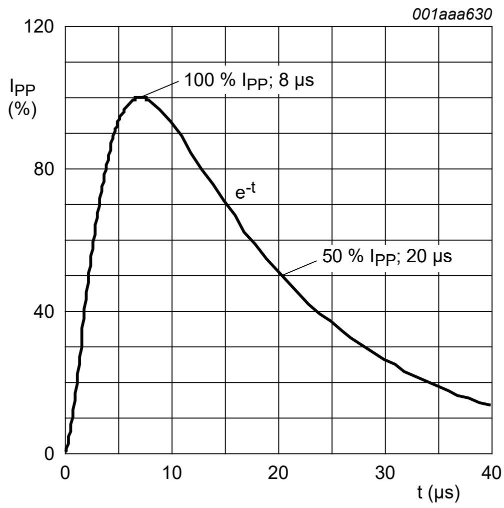



**Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5**

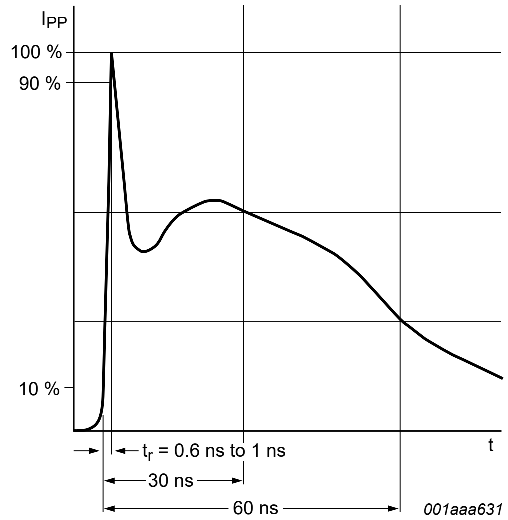



**Fig. 2. ESD pulse waveform according to IEC 61000-4-2**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{BR}$ | breakdown voltage | $I_R$ = 1 mA; $T_{amb}$ = 25 °C | [1] | - | 8 | - | V |
| $I_{RM}$ | reverse leakage current | $V_{RWM}$ = 4 V; $T_{amb}$ = 25 °C | [1] | - | 1 | 50 | nA |
| $C_d$ | diode capacitance | f = 1 MHz; $V_R$ = 0 V; $T_{amb}$ = 25 °C | [1] | - | 0.5 | 0.6 | pF |
| $V_{CL}$ | clamping voltage | $I_{TLP}$ = 8 A; $t_p$ = 100 ns; $T_{amb}$ = 25 °C | [1] [2] | - | 3.2 | - | V |
| | | $I_{TLP}$ = 16 A; $t_p$ = 100 ns; $T_{amb}$ = 25 °C | [1] [2] | - | 5 | - | V |
| | | $I_{PPM}$ = 6.5 A; $t_p$ = 8/20 µs; $T_{amb}$ = 25 °C | [1] [3] | - | 3.4 | - | V |
| $R_{dyn}$ | dynamic resistance | $I_R$ = 10 A; $T_{amb}$ = 25 °C | [1] [2] | - | 0.27 | - | Ω |
| | | $I_R$ = -10 A; $T_{amb}$ = 25 °C | [1] [2] | - | 0.27 | - | Ω |
| $f_{-3dB,dd}$ | differential cut-off frequency | normalized to attenuation at 1 MHz; $T_{amb}$ = 25 °C | [1] | - | 5.8 | - | GHz |

[1] Measured from pin 1 or 2 to pin 3.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP); square pulse; ANSI / ESD STM5.5.1-2008
[3] Device stressed with 8/20 µs exponential decay waveform according to IEC 61000-4-5

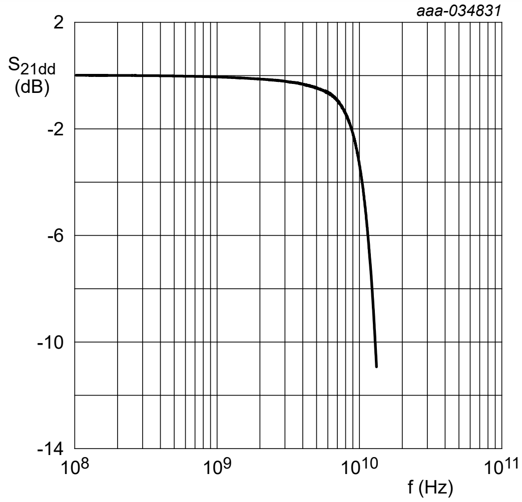



**Fig. 3. Insertion loss; typical values**

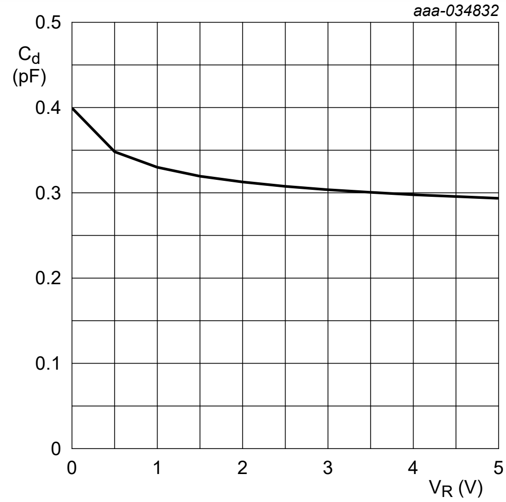
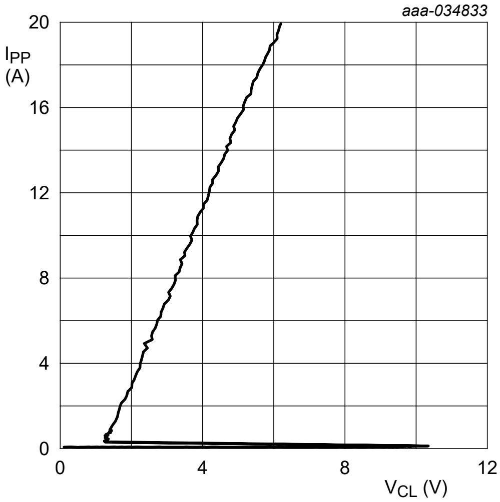
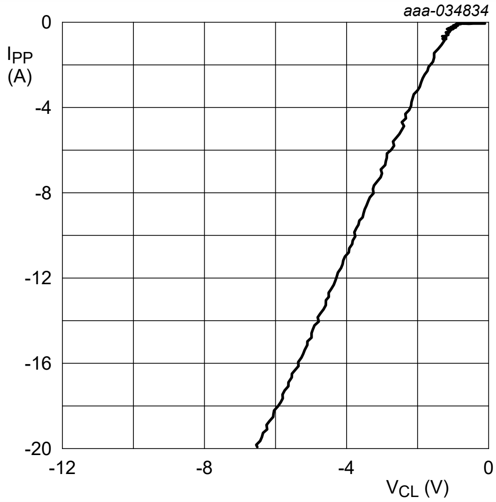



**Fig. 4. Capacitance as a function of reverse voltage; typical values**



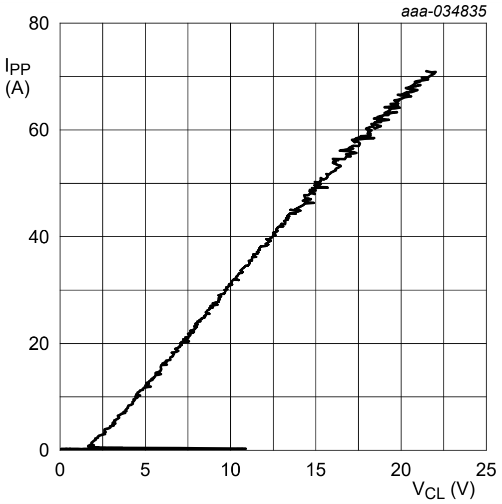

Transmission Line Pulse (TLP);
$t_p$ = 100 ns; $t_r$ = 1 ns

**Fig. 5. Dynamic resistance with positive clamping; typical values**



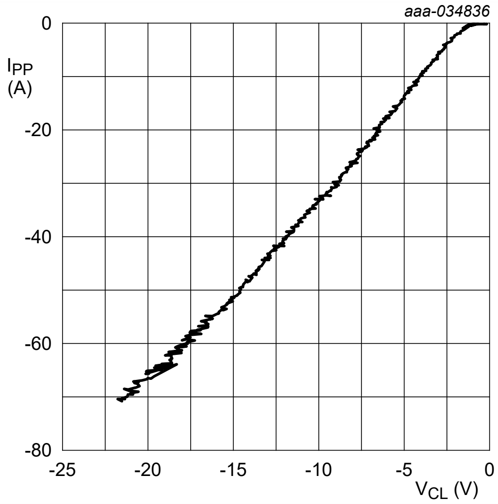

Transmission Line Pulse (TLP);
$t_p$ = 100 ns; $t_r$ = 1 ns

**Fig. 6. Dynamic resistance with negative clamping; typical values**



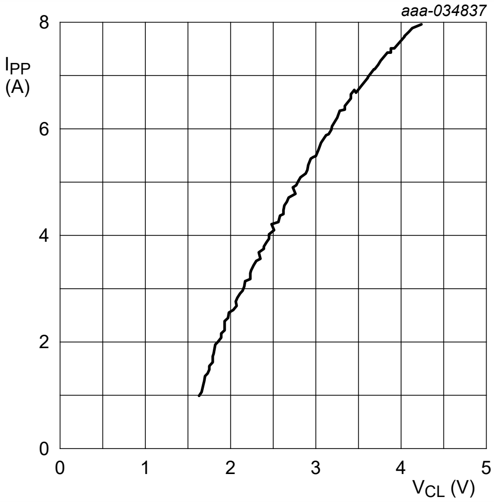

Very-Fast Transmission Line Pulse (VF-TLP);
$t_p$ = 5 ns; $t_r$ = 600 ps

**Fig. 7. Dynamic resistance with positive clamping; typical values**



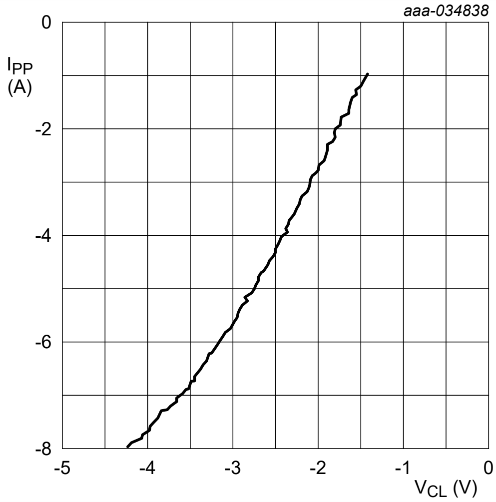

Very-Fast Transmission Line Pulse (VF-TLP);
$t_p$ = 5 ns; $t_r$ = 600 ps

**Fig. 8. Dynamic resistance with negative clamping; typical values**




IEC 61000-4-5; $t_p$ = 8/20 μs; positive pulse

**Fig. 9. Dynamic resistance with positive clamping; typical values**




IEC 61000-4-5; $t_p$ = 8/20 μs; negative pulse

**Fig. 10. Dynamic resistance with negative clamping; typical values**

# 10. Application information

The device is designed for the protection of two uni-directional or one bi-directional data or signal lines from surge pulses and ESD damage.

The device uses an advanced clamping structure showing a negative dynamic resistance. This snap-back behavior strongly reduces the clamping voltage to the system behind the ESD protection during an ESD event. Do not connect unlimited DC current sources to the data lines to avoid keeping the ESD protection device in snap-back state after exceeding breakdown voltage (due to an ESD pulse for instance).

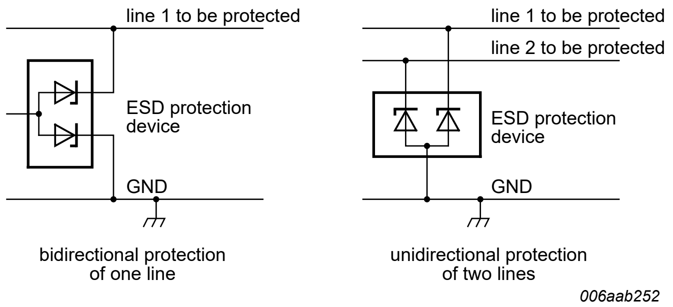



**Fig. 11. Application diagram**

**Circuit board layout and protection device placement**

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

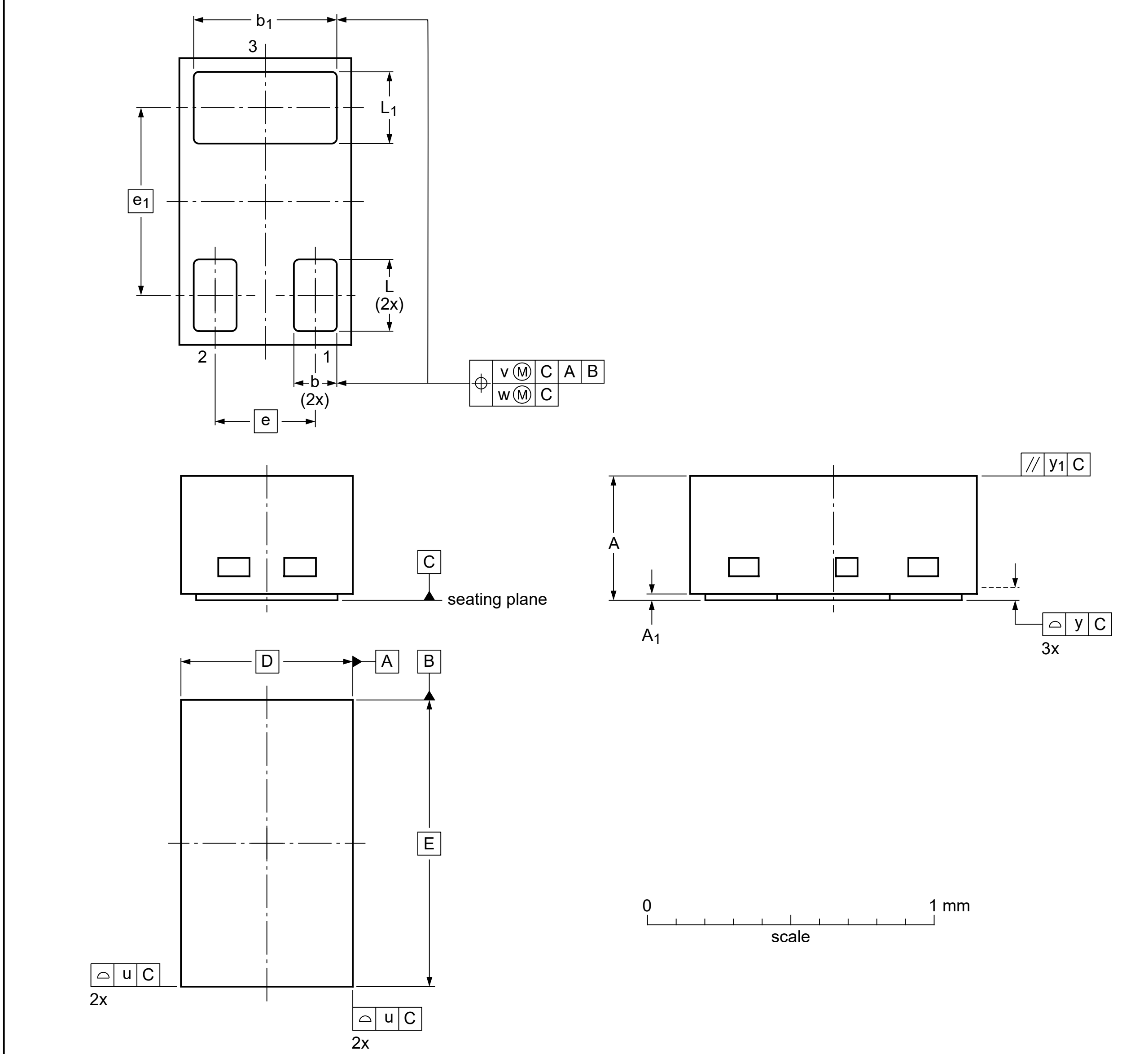
# 11. Test information

## Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

# 12. Package outline

**Leadless ultra small plastic package; 3 solder lands; body 1.0 x 0.6 x 0.47 mm** **SOT883-2**




Dimensions

| Unit | | A | A1 | b | b1 | D | E | e | e1 | L | L1 | u | v | w | y | y1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | max | 0.50 | 0.03 | 0.20 | 0.55 | | | | | 0.30 | 0.30 | | | | | |
| mm | nom | 0.47 | | 0.15 | 0.50 | 0.60 | 1.00 | 0.35 | 0.65 | 0.25 | 0.25 | 0.05 | 0.1 | 0.05 | 0.05 | 0.05 |
| | min | 0.44 | | 0.10 | 0.45 | | | | | 0.20 | 0.20 | | | | | |

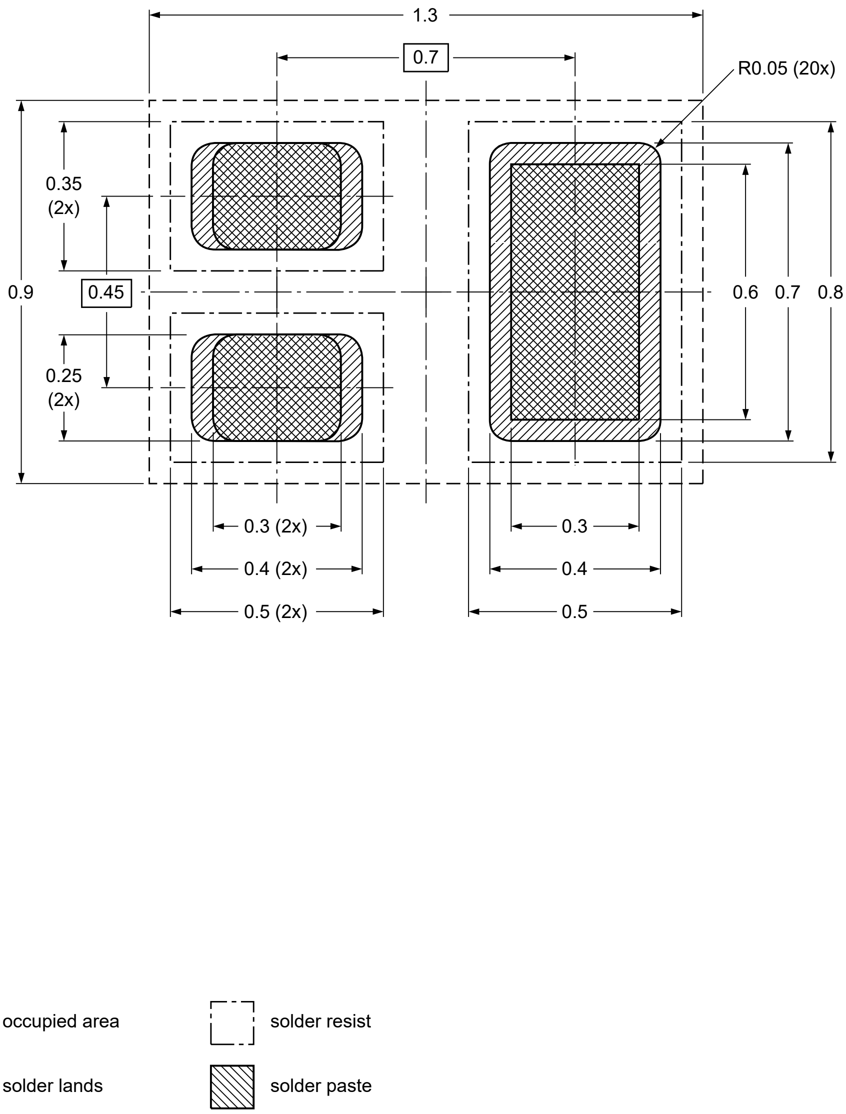
*sot883-2_po*

| Outline version | References IEC | References JEDEC | References JEITA | | European projection | Issue date |
|---|---|---|---|---|---|---|
| SOT883-2 | | - - - | | | | ~~21-10-19~~ 21-11-03 |

**Fig. 12. Package outline DFN1006-3 (SOT883-2)**

## 13. Soldering

**Footprint information for reflow soldering of DFN1006-3 package** **SOT883-2**




Issue date 21-10-18

*sot883-2_fr*

**Fig. 13. Reflow soldering footprint for DFN1006-3 (SOT883-2)**

## 14. Revision history

**Table 7. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| PESD5V0C2UM-Q v.2 | 20220525 | Product data sheet | - | PESD5V0C2UM-Q v.1 |
| Modifications: | • Typo correction: package version set to SOT883-2 | | | |
| PESD5V0C2UM-Q v.1 | 20220520 | Product data sheet | - | - |

# 15. Legal information

## Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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**Date of release: 25 May 2022**

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