

74VHC32-Q100; 74VHCT32-Q100

Quad 2-input OR gate

Rev. 3 — 18 April 2024

Product data sheet

1. General description

The 74VHC32-Q100; 74VHCT32-Q100 are high-speed Si-gate CMOS devices and are pin compatible with Low-power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard No. 7-A.

The 74VHC32-Q100; 74VHCT32-Q100 provide the 2-input OR function.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

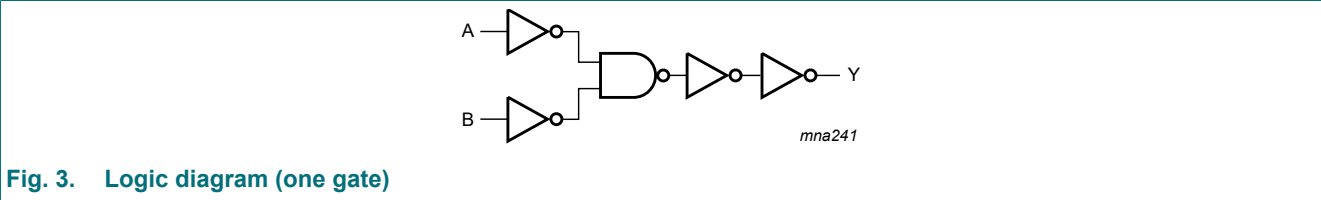
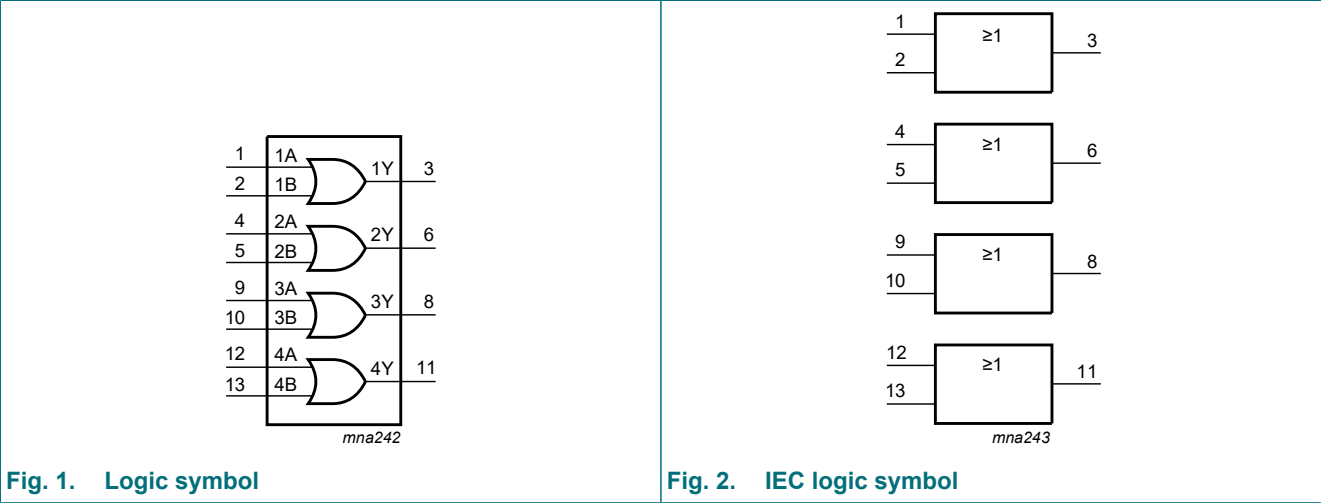
- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - The 74VHC32-Q100 operates with CMOS input level
 - The 74VHCT32-Q100 operates with TTL input level
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

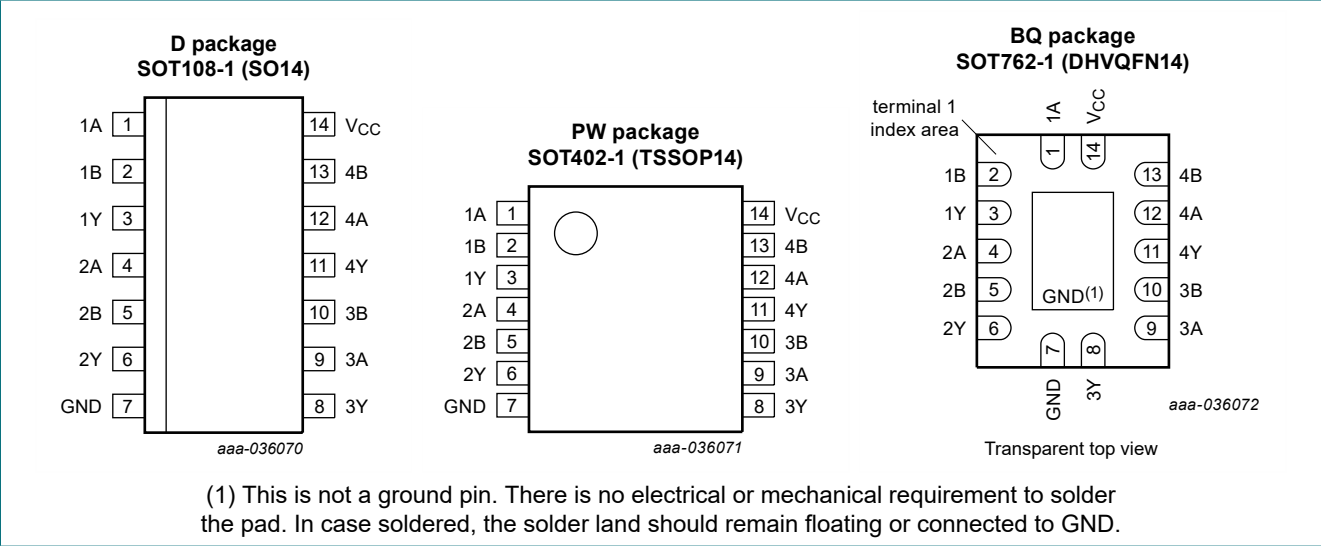
| Type number | Package | | | |
|---|-------------------|----------|--|--------------------------|
| | Temperature range | Name | Description | Version |
| 74VHC32D-Q100 74VHCT32D-Q100 | -40 °C to +125 °C | SO14 | plastic small outline package; 14 leads; body width 3.9 mm | SOT108-1 |
| 74VHC32PW-Q100 74VHCT32PW-Q100 | -40 °C to +125 °C | TSSOP14 | plastic thin shrink small outline package; 14 leads; body width 4.4 mm | SOT402-1 |
| 74VHC32BQ-Q100 74VHCT32BQ-Q100 | -40 °C to +125 °C | DHVQFN14 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm | SOT762-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------|----------------|
| 1A, 2A, 3A, 4A | 1, 4, 9, 12 | data input |
| 1B, 2B, 3B, 4B | 2, 5, 10, 13 | data input |
| 1Y, 2Y, 3Y, 4Y | 3, 6, 8, 11 | data output |
| GND | 7 | ground (0 V) |
| V _{CC} | 14 | supply voltage |

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

| Input | | Output |
|-------|----|--------|
| nA | nB | nY |
| L | L | L |
| X | H | H |
| H | X | H |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|---|------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | -0.5 | +7.0 | V |
| I _{IK} | input clamping current | V _I < -0.5 V [1] | -20 | - | mA |
| I _{OK} | output clamping current | V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1] | -20 | +20 | mA |
| I _O | output current | V _O = -0.5 V to (V _{CC} + 0.5 V) | -25 | +25 | mA |
| I _{CC} | supply current | | - | +75 | mA |
| I _{GND} | ground current | | -75 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [2] | - | 500 | mW |

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.
For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.
For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|-------------------------------------|----------------------------------|-----|-----|-----------------|------|
| 74VHC32-Q100 | | | | | | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 3.0 V to 3.6 V | - | - | 100 | ns/V |
| | | V _{CC} = 4.5 V to 5.5 V | - | - | 20 | ns/V |
| 74VHCT32-Q100 | | | | | | |
| V _{CC} | supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | 5.5 | V |
| V _O | output voltage | | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 4.5 V to 5.5 V | - | - | 20 | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|---|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74VHC32-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | - | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 3.0 V | 2.1 | - | - | 2.1 | - | 2.1 | - | V |
| | | V _{CC} = 5.5 V | 3.85 | - | - | 3.85 | - | 3.85 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | - | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 3.0 V | - | - | 0.9 | - | 0.9 | - | 0.9 | V |
| | | V _{CC} = 5.5 V | - | - | 1.65 | - | 1.65 | - | 1.65 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -50 µA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -50 µA; V _{CC} = 3.0 V | 2.9 | 3.0 | - | 2.9 | - | 2.9 | - | V |
| | | I _O = -50 µA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -4.0 mA; V _{CC} = 3.0 V | 2.58 | - | - | 2.48 | - | 2.40 | - | V |
| | | I _O = -8.0 mA; V _{CC} = 4.5 V | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 50 µA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 µA; V _{CC} = 3.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 50 µA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 4.0 mA; V _{CC} = 3.0 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| | | I _O = 8.0 mA; V _{CC} = 4.5 V | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | µA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|---|-------|-----|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74VHCT32-Q100 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | - | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | - | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -50 µA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -8.0 mA | 3.94 | - | - | 3.80 | - | 3.70 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 50 µA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 8.0 mA | - | - | 0.36 | - | 0.44 | - | 0.55 | V |
| I _I | input leakage current | V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V | - | - | 0.1 | - | 1.0 | - | 2.0 | µA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 2.0 | - | 20 | - | 40 | µA |
| ΔI _{CC} | additional supply current | per input pin; V _I = V _{CC} - 2.1 V; other pins at V _{CC} or GND; I _O = 0 A; V _{CC} = 4.5 V to 5.5 V | - | - | 1.35 | - | 1.5 | - | 1.5 | mA |
| C _I | input capacitance | V _I = V _{CC} or GND | - | 3 | 10 | - | 10 | - | 10 | pF |
| C _O | output capacitance | | - | 4 | - | - | - | - | - | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|-------------------------------|---|-------|--------|------|------------------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74VHC32-Q100 | | | | | | | | | | |
| t _{pd} | propagation delay | nA, nB to nY; see Fig. 4 [2] | | | | | | | | |
| | | V _{CC} = 3.0 V to 3.6 V | | | | | | | | |
| | | C _L = 15 pF | - | 3.9 | 7.9 | 1.0 | 9.5 | 1.0 | 10.0 | ns |
| | | C _L = 50 pF | - | 5.6 | 11.4 | 1.0 | 13 | 1.0 | 14.5 | ns |
| | | V _{CC} = 4.5 V to 5.5 V | | | | | | | | |
| | | C _L = 15 pF | - | 2.8 | 5.5 | 1.0 | 6.5 | 1.0 | 7.0 | ns |
| | | C _L = 50 pF | - | 4.1 | 7.5 | 1.0 | 8.5 | 1.0 | 9.5 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [3] | - | 10 | - | - | - | - | - | pF |

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|---|-------------------------------|---|-------|--------|-----|------------------|-----|-------------------|------|------|
| | | | Min | Typ[1] | Max | Min | Max | Min | Max | |
| 74VHCT32-Q100; V _{CC} = 4.5 V to 5.5 V | | | | | | | | | | |
| t _{pd} | propagation delay | nA, nB to nY; see Fig. 4 [2] | | | | | | | | |
| | | C _L = 15 pF | - | 3.1 | 6.9 | 1.0 | 8.0 | 1.0 | 9.0 | ns |
| | | C _L = 50 pF | - | 4.3 | 7.9 | 1.0 | 9.0 | 1.0 | 10.0 | ns |
| C _{PD} | power dissipation capacitance | f _i = 1 MHz; V _I = GND to V _{CC} [3] | - | 12 | - | - | - | - | - | pF |

- [1] Typical values are measured at nominal supply voltage (V_{CC} = 3.3 V and V_{CC} = 5.0 V).
- [2] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
P_D = C_{PD} × V_{CC}² × f_i × N + Σ(C_L × V_{CC}² × f_o) where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
Σ(C_L × V_{CC}² × f_o) = sum of the outputs.

10.1. Waveforms and test circuit

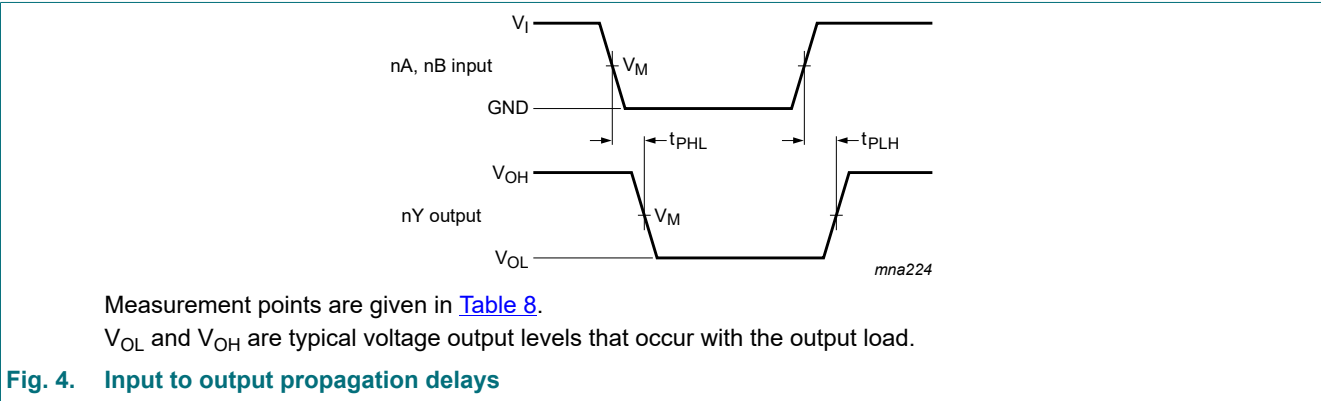
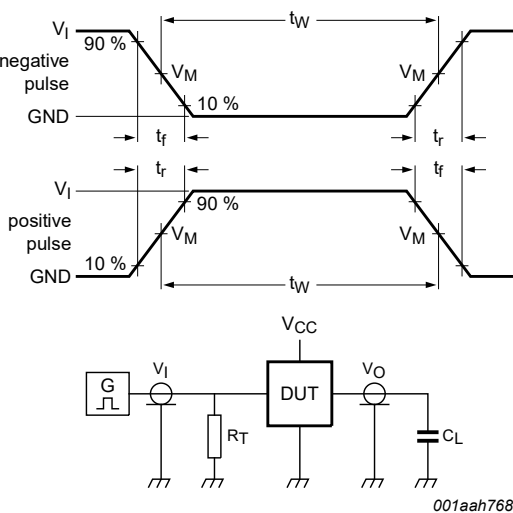


Table 8. Measurement points

| Type | Input | Output |
|---------------|--------------------|--------------------|
| | V _M | V _M |
| 74VHC32-Q100 | 0.5V _{CC} | 0.5V _{CC} |
| 74VHCT32-Q100 | 1.5 V | 0.5V _{CC} |



Test data is given in [Table 9](#).
Definitions test circuit:
 R_T = termination resistance should be equal to output impedance Z_o of the pulse generator.
 C_L = load capacitance including jig and probe capacitance.

Fig. 5. Test circuit for measuring switching times

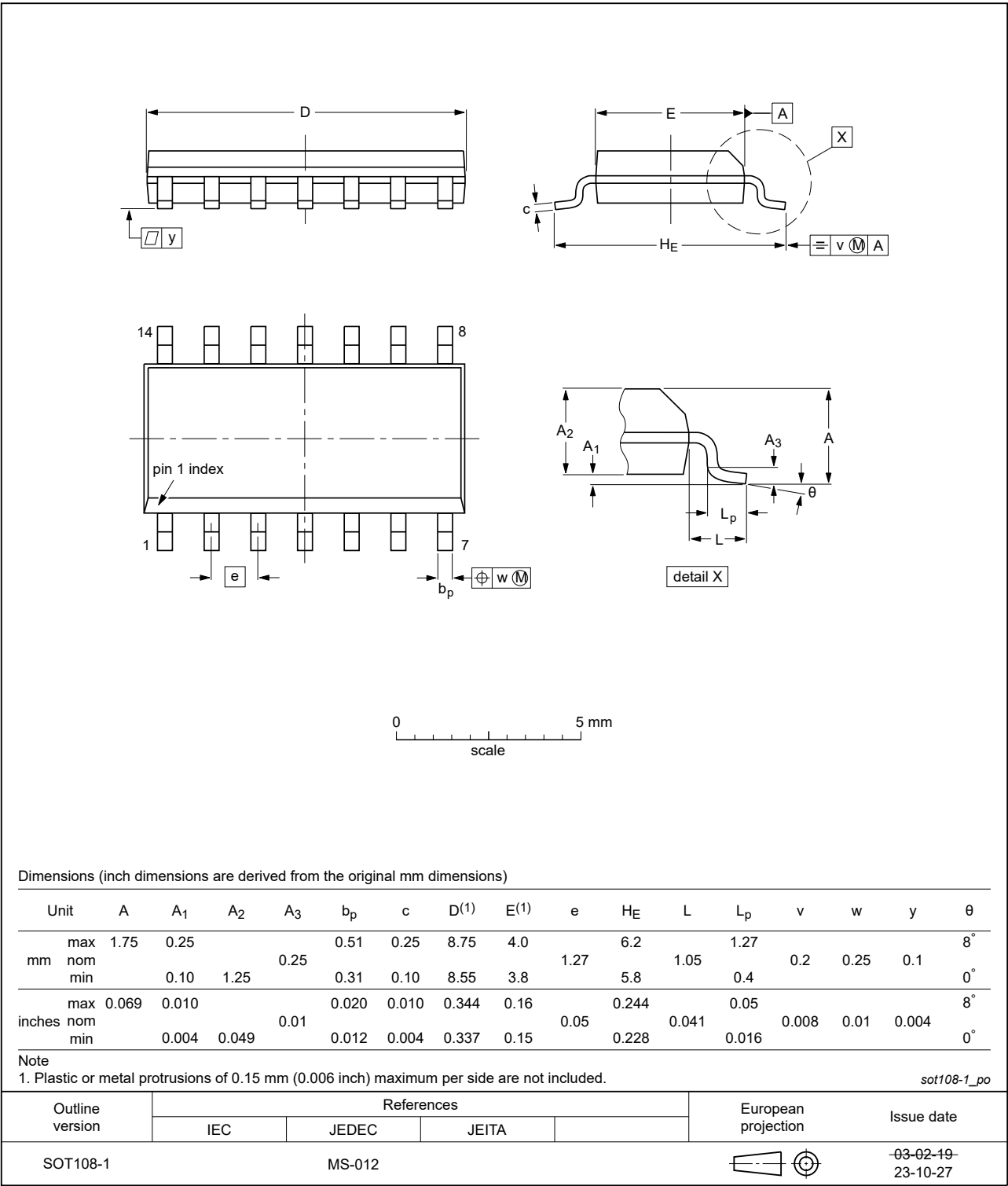
Table 9. Test data

| Type | Input | | Load | Test |
|---------------|----------|-----------------------|--------------|--------------------|
| | V_I | t_r, t_f | C_L | |
| 74VHC32-Q100 | V_{CC} | $\leq 3.0 \text{ ns}$ | 15 pF, 50 pF | t_{PLH}, t_{PHL} |
| 74VHCT32-Q100 | 3.0 V | $\leq 3.0 \text{ ns}$ | 15 pF, 50 pF | t_{PLH}, t_{PHL} |

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1



0

5 mm

scale

detail X

Fig. 6. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

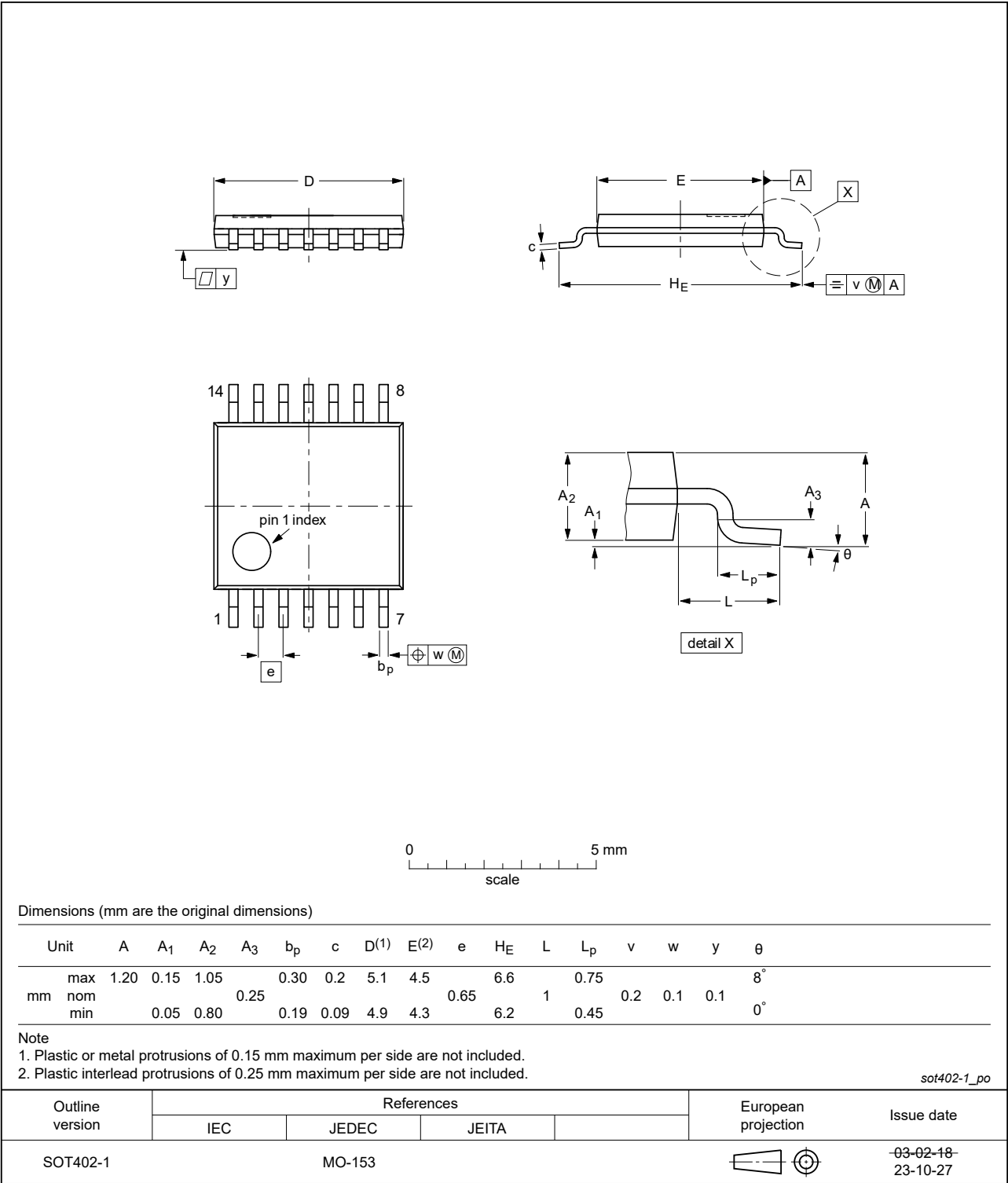


Fig. 7. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

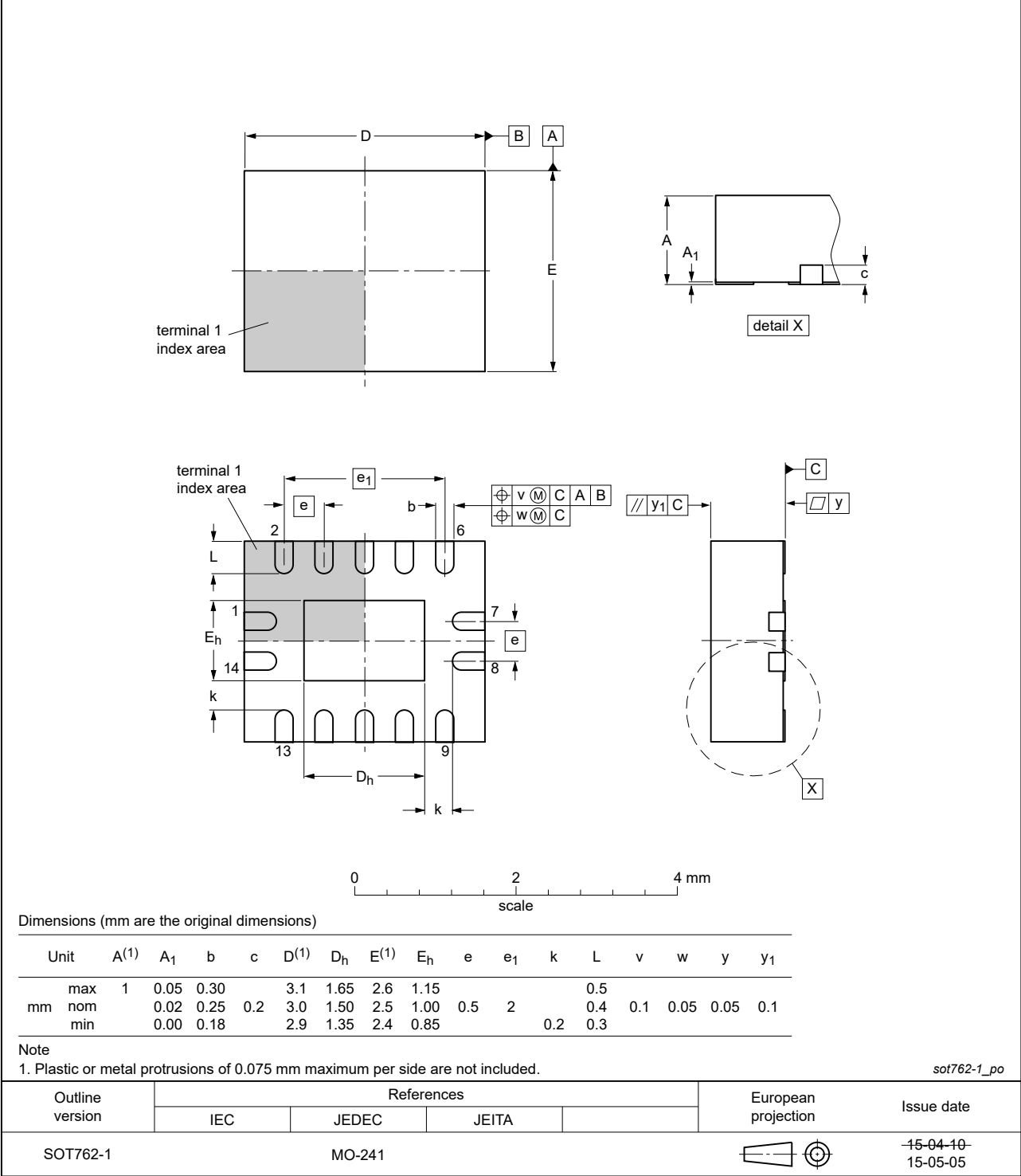


Fig. 8. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|--|
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| LSTTL | Low-power Schottky Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------------|---|--------------------|---------------|-----------------------|
| 74VHC_VHCT32_Q100 v.3 | 20240418 | Product data sheet | - | 74VHC_VHCT32_Q100 v.2 |
| Modifications: | <ul style="list-style-type: none">• Fig. 6, Fig. 7: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.• Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74VHC_VHCT32_Q100 v.2 | 20200903 | Product data sheet | - | 74VHC_VHCT32_Q100 v.1 |
| Modifications: | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.• Legal texts have been adapted to the new company name where appropriate.• Section 2 updated.• Table 4: Derating values for P_{tot} total power dissipation have been updated.• Fig. 8: Package outline drawing of SOT762-1 (DHVQFN14) updated. | | | |
| 74VHC_VHCT32_Q100 v.1 | 20131220 | Product data sheet | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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