



PDTD143XT

50 V, 500 mA NPN resistor-equipped transistor;
R1 = 4.7 k Ω , R2 = 10 k Ω

13 October 2022

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a small SOT23 (TO-236AB) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTB143XT

2. Features and benefits

- 500 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- $\pm 10\%$ resistor ratio tolerance
- High temperature applications up to 175 °C
- AEC-Q101 qualified

3. Applications

- IC inputs control
- Cost-saving alternative to BC807 series transistors in digital applications
- Switching loads

4. Quick reference data

Table 1. Quick reference data

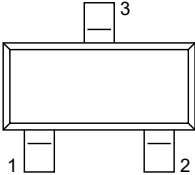
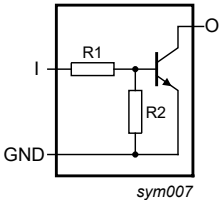
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
I _O	output current			-	-	500	mA
R1	bias resistor 1 (input)		[1]	3.3	4.7	6.1	k Ω
R2/R1	bias resistor ratio		[1]	1.91	2.13	2.34	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

50 V, 500 mA NPN resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 10 kΩ

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	 SOT23	 sym007
2	GND	ground (emitter)		
3	O	output (collector)		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PDTD143XT	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code ^[1]
PDTD143XT	%5Z

[1] % = placeholder for manufacturing site code

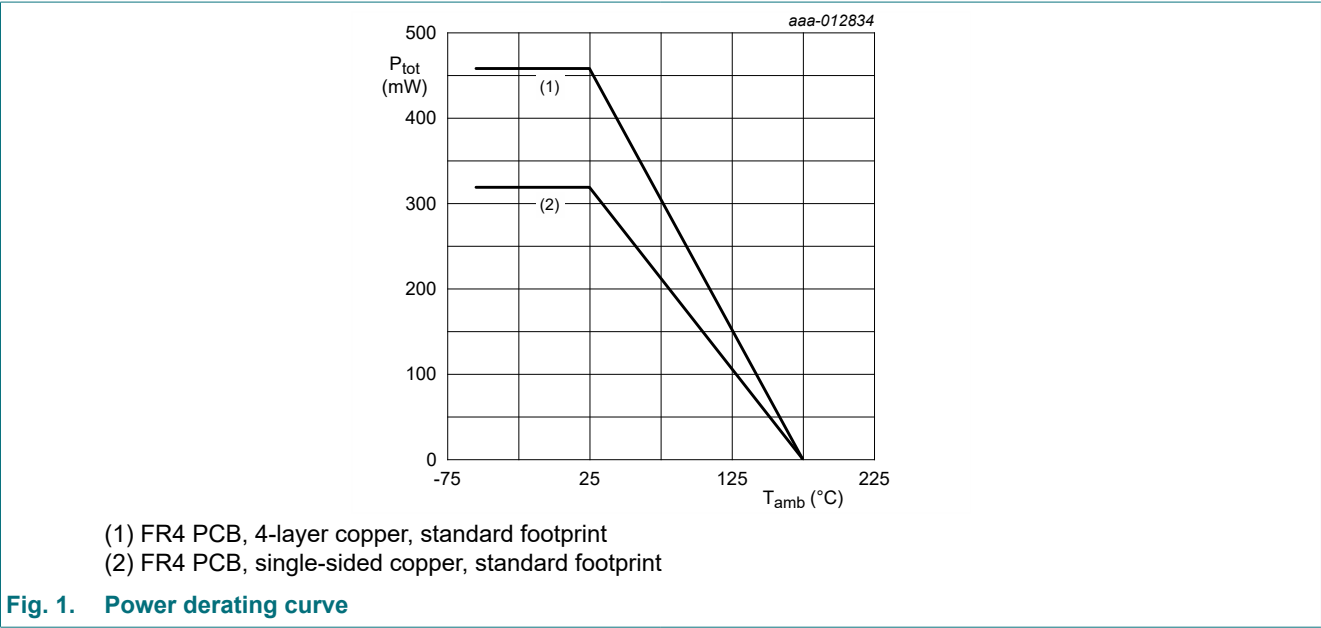
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	7	V
V _I	input voltage	positive		-7	30	V
I _O	output current			-	500	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1]	-	320	mW
			[2]	-	460	mW
T _j	junction temperature			-	175	°C
T _{amb}	ambient temperature			-55	175	°C
T _{stg}	storage temperature			-55	175	°C

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.



9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	470	K/W
			[2]	-	-	327	K/W

- [1] Device mounted on an FR4 PCB, 35 μm copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, 4-layer copper, tin-plated and standard footprint.

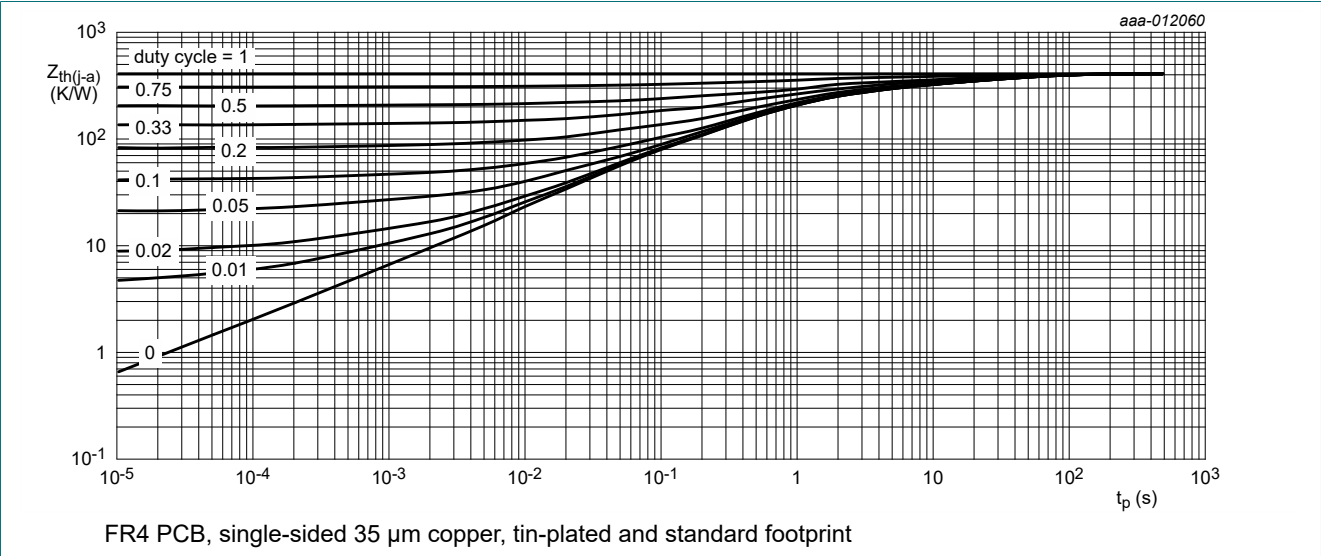


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

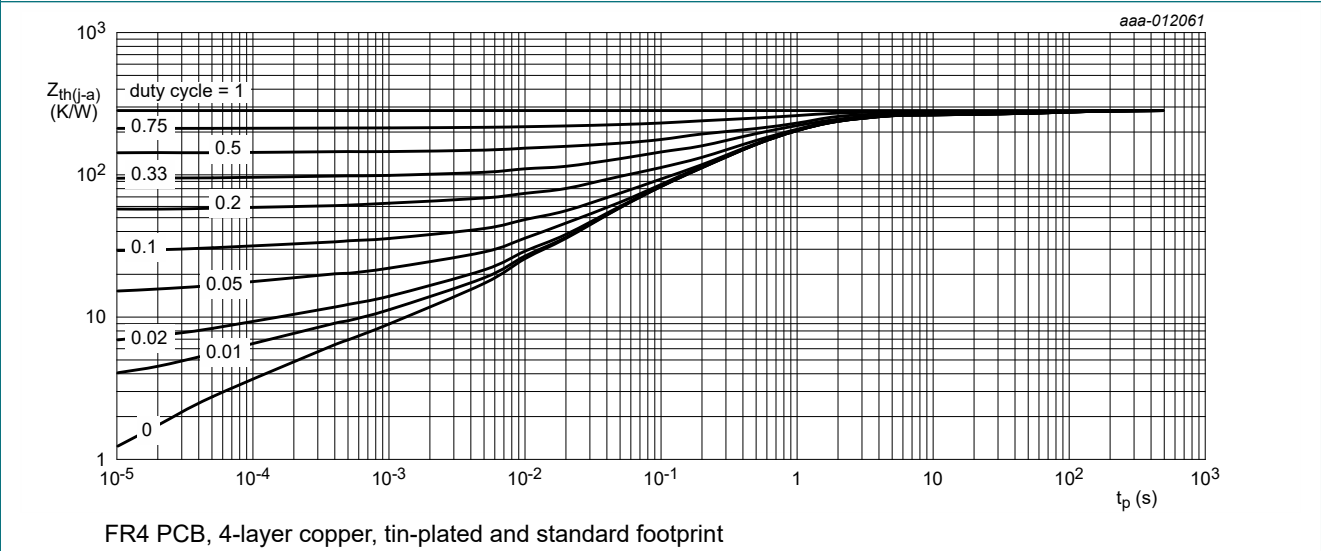


Fig. 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

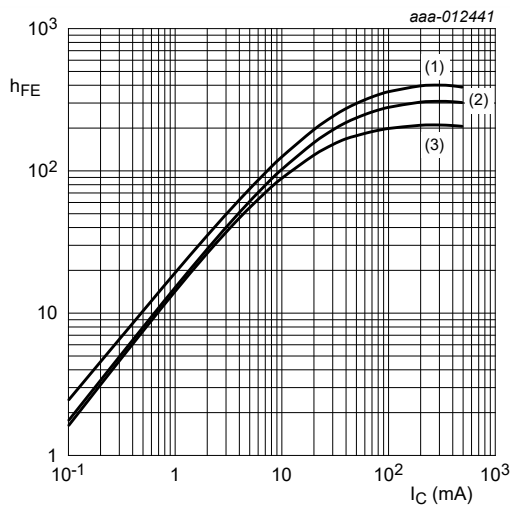
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)CBO}$	collector-base breakdown voltage	$I_C = 100\ \mu\text{A}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 10\ \text{mA}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	50	-	-	V
I_{CBO}	collector-base cut-off current	$V_{CB} = 40\ \text{V}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	100	nA
		$V_{CB} = 50\ \text{V}$; $I_E = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	100	nA
I_{CEO}	collector-emitter cut-off current	$V_{CE} = 50\ \text{V}$; $I_B = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	0.5	μA
I_{EBO}	emitter-base cut-off current	$V_{EB} = 5\ \text{V}$; $I_C = 0\ \text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	0.6	mA
h_{FE}	DC current gain	$V_{CE} = 5\ \text{V}$; $I_C = 50\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	70	-	-	
V_{CEsat}	collector-emitter saturation voltage	$I_C = 50\ \text{mA}$; $I_B = 2.5\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	-	100	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\ \text{V}$; $I_C = 100\ \mu\text{A}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	0.5	0.75	1.1	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\ \text{V}$; $I_C = 20\ \text{mA}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	1	1.25	2	V
R1	bias resistor 1 (input)		[1]	3.3	4.7	kΩ
R2/R1	bias resistor ratio		[1]	1.91	2.13	
C_c	collector capacitance	$V_{CB} = 10\ \text{V}$; $I_E = 0\ \text{A}$; $i_e = 0\ \text{A}$; $f = 1\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	-	7	-	pF
f_T	transition frequency	$V_{CE} = 5\ \text{V}$; $I_C = 50\ \text{mA}$; $f = 100\ \text{MHz}$; $T_{\text{amb}} = 25\ ^\circ\text{C}$	[2]	225	-	MHz

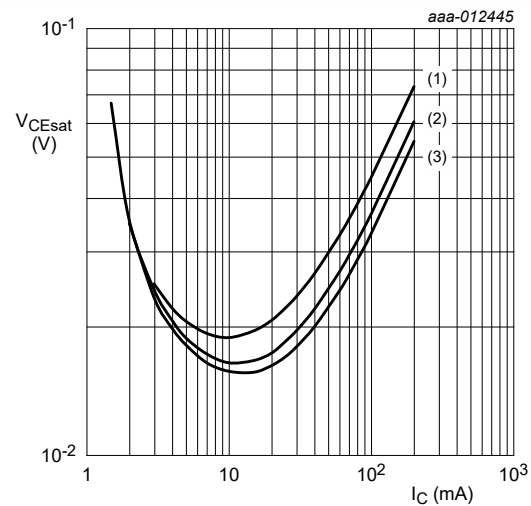
[1] See "Section 11: Test information" for resistor calculation and test conditions.

[2] Characteristics of built-in transistor.



$V_{CE} = 5\ \text{V}$
 (1) $T_{\text{amb}} = 100\ ^\circ\text{C}$
 (2) $T_{\text{amb}} = 25\ ^\circ\text{C}$
 (3) $T_{\text{amb}} = -40\ ^\circ\text{C}$

Fig. 4. DC current gain as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{\text{amb}} = 100\ ^\circ\text{C}$
 (2) $T_{\text{amb}} = 25\ ^\circ\text{C}$
 (3) $T_{\text{amb}} = -40\ ^\circ\text{C}$

Fig. 5. Collector-emitter saturation voltage as a function of collector current; typical values

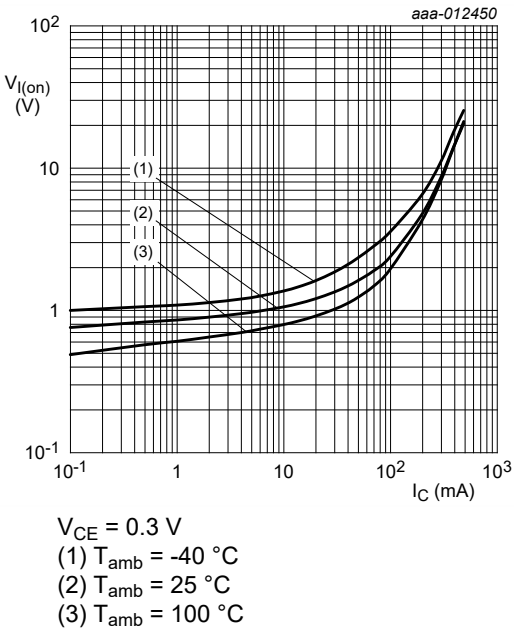


Fig. 6. On-state input voltage as a function of collector current; typical values

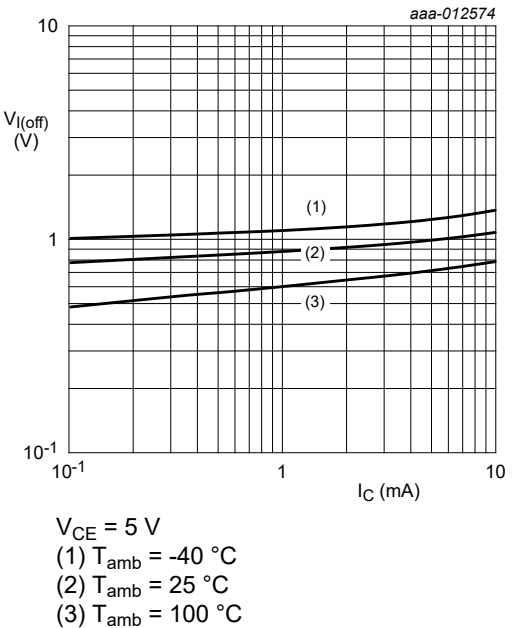


Fig. 7. Off-state input voltage as a function of collector current; typical values

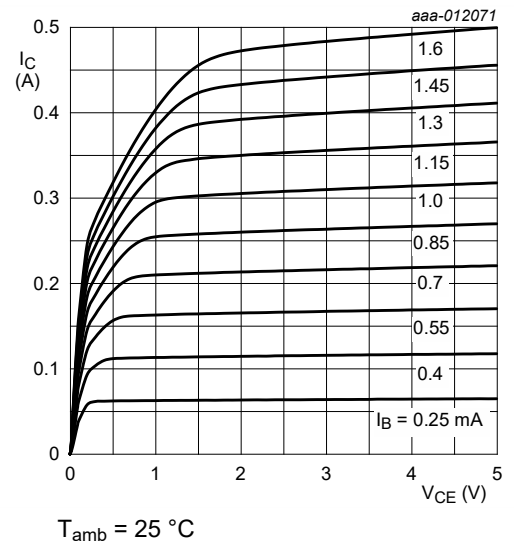


Fig. 8. Collector current as a function of collector-emitter voltage; typical values

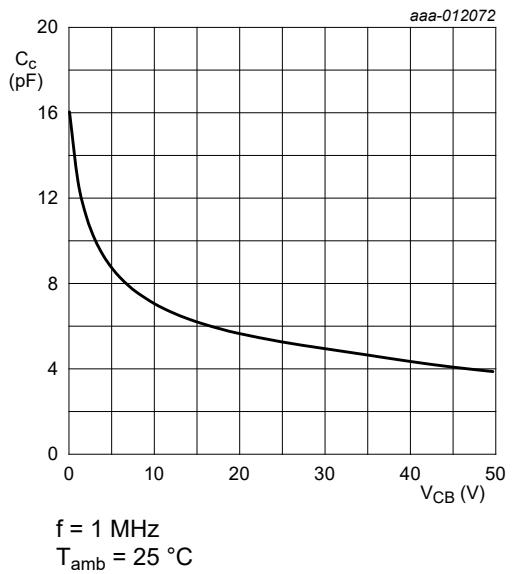
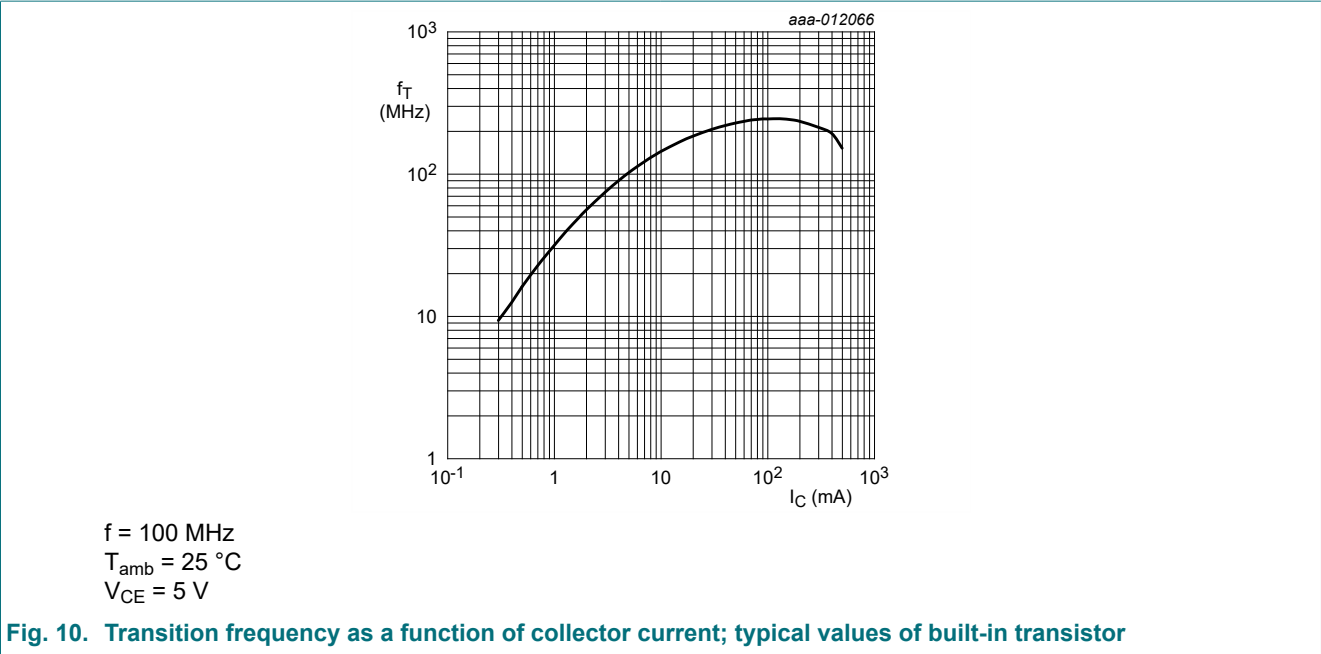


Fig. 9. Collector capacitance as a function of collector-base voltage; typical values

50 V, 500 mA NPN resistor-equipped transistor; R1 = 4.7 kΩ, R2 = 10 kΩ



11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R_1 = \frac{V(I_2) - V(I_1)}{I_2 - I_1}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R_2}{R_1} = \frac{V(I_4) - V(I_3)}{R_1 \cdot (I_4 - I_3)} - 1$$

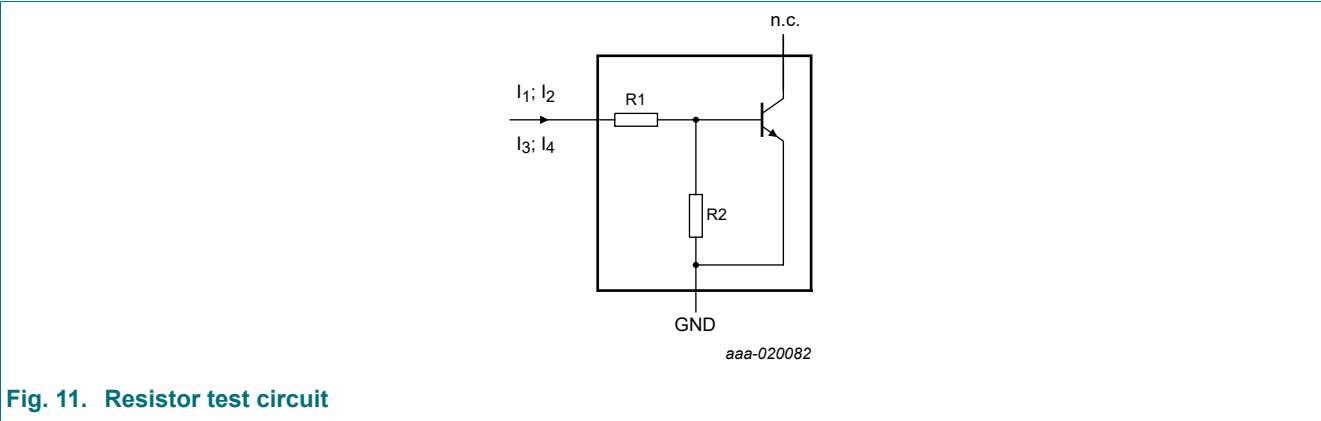


Fig. 11. Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I ₁	I ₂	I ₃	I ₄
PDTD143XT	4.7	10	1.3 mA	1.5 mA	-0.45 mA	-0.55 mA

12. Package outline

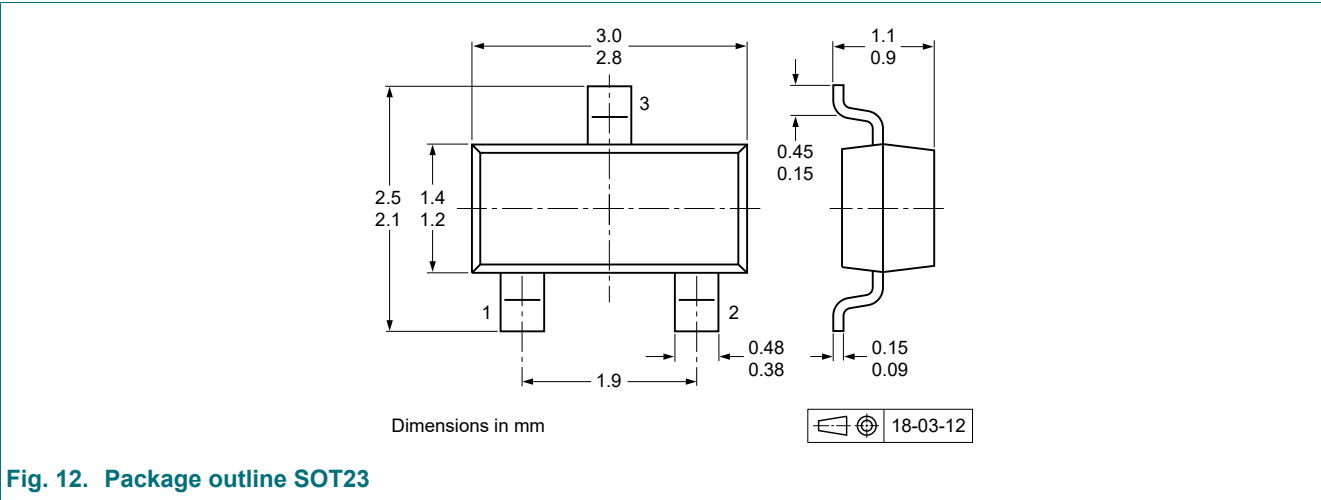


Fig. 12. Package outline SOT23

13. Soldering

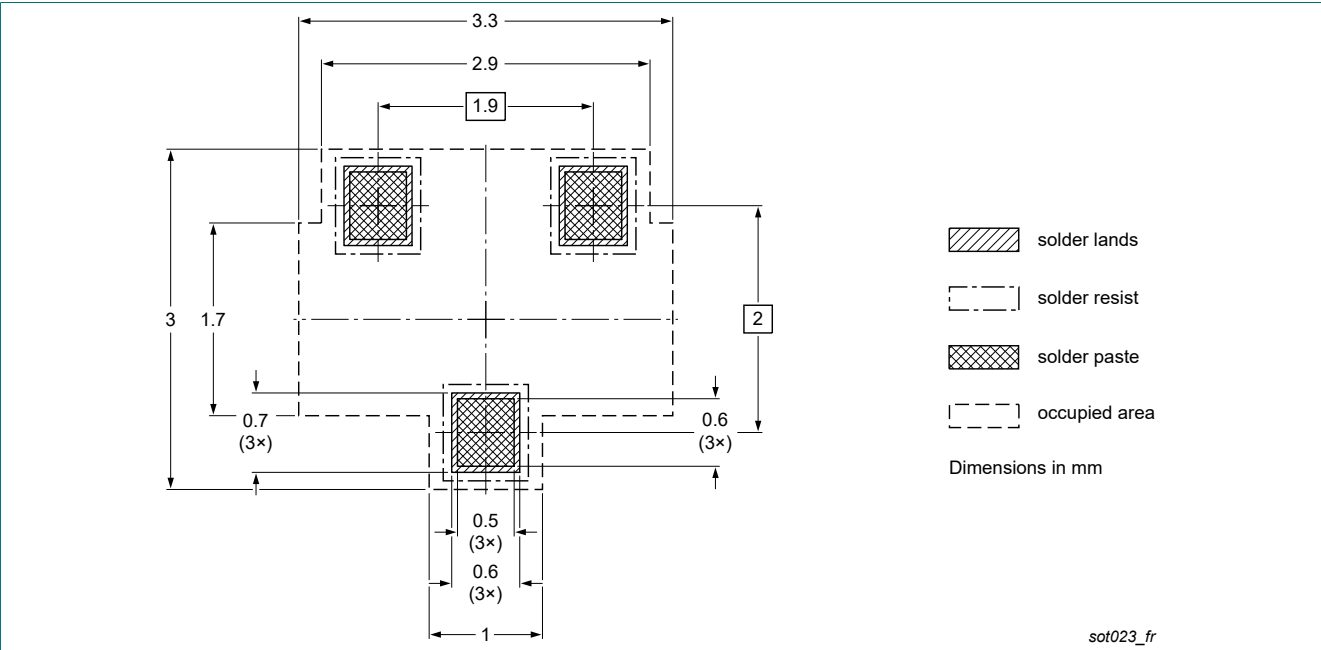


Fig. 13. Reflow soldering footprint for SOT23

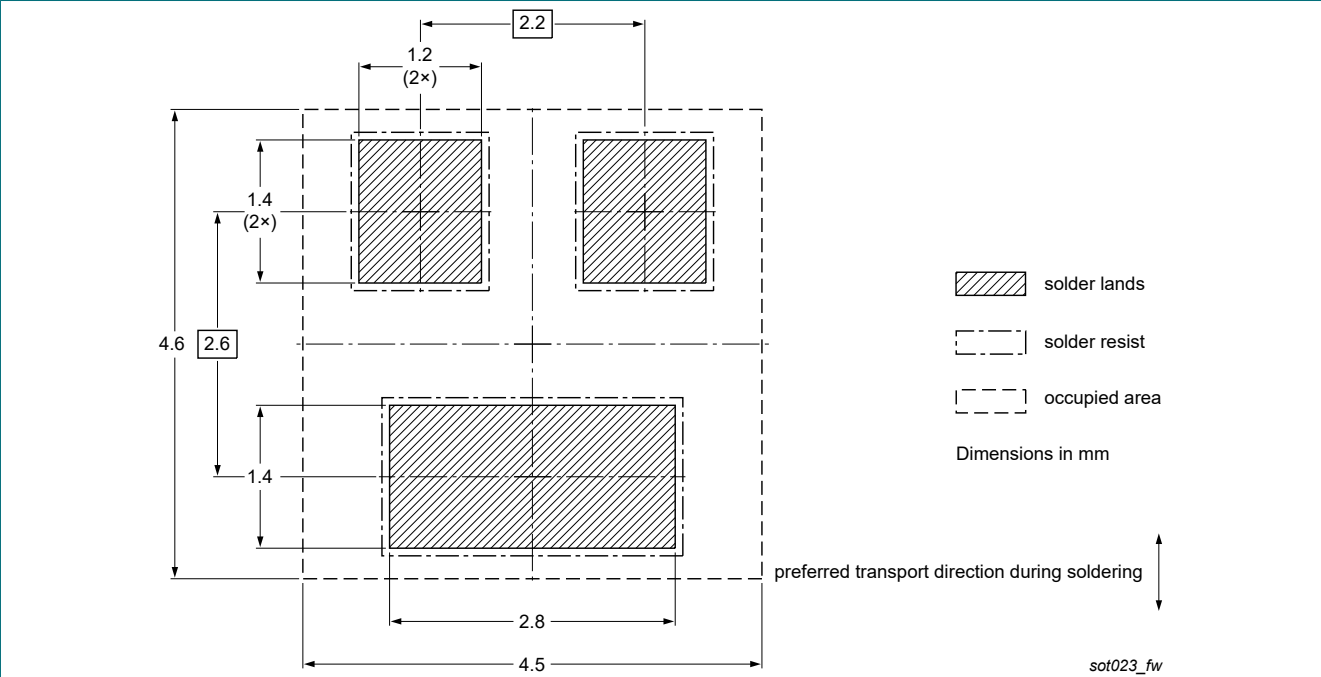


Fig. 14. Wave soldering footprint for SOT23

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PDTD143XT v.2	20221013	Product data sheet	-	PDTD1XXXT_SER v.1
Modifications:	• Family data sheet reduced to single type data sheet.			
PDTD1XXXT_SER v.1	20140515	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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