PSMNR70-40YSN

N-channel 40 V, 0.81 mOhm, 320 A standard level MOSFET in LFPAK56E using NextPower-S3 Schottky-Plus technology

6 December 2023 Objective data sheet

1. General description

320 Amp, standard level gate drive N-channel enhancement mode MOSFET in 175 °C LFPAK56E package using advanced TrenchMOS Superjunction technology. This product has been designed and qualified for high performance power switching applications.

2. Features and benefits

- 320 A continuous $I_{D(max)}$
- Avalanche rated, 100% tested at I_{AS} = 190 A
- Low spiking, allowing for high system efficiency and low EMI designs
- NextPower-S3 technology delivers 'superfast switching with soft body-diode recovery
- Low Q_{rr}, spiking, ringing, and oscillation for high system efficiency and low EMI designs
- Schottky-Plus body-diode with low V_{SD}, and low I_{DSS} leakage
- High reliability LFPAK (Power SO8) package, with copper-clip and solder die attach, qualified to 175 °C
- Exposed leads for enhanced visual solder joint inspection and high-quality solder joints for ultimate reliability
- Low parasitic inductance and resistance

3. Applications

- High-performance synchronous rectification
- DC-to-DC converters
- High performance and high efficiency server power supply
- Brushless DC motor control
- Battery protection
- Load-switch
- eFuse

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	-	40	V
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	-	320	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	-	333	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		0.48	0.68	0.81	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 6		17	57	96	nC

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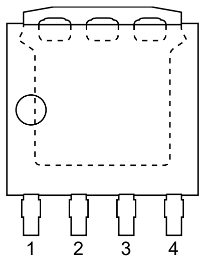
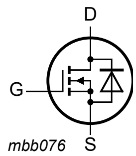
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Source-drain diode							
Q_r	recovered charge	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 7	[2]	-	[tbd]	-	nC

[1] 320 A continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] includes capacitive recovery

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56E; Power-SO8 (SOT1023)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMNR70-40YSN	LFPAK56E; Power-SO8	plastic, single-ended surface-mounted package (LFPAK56); 4 leads; 1.27 mm pitch	SOT1023

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMNR70-40YSN	N9040S

8. Limiting values

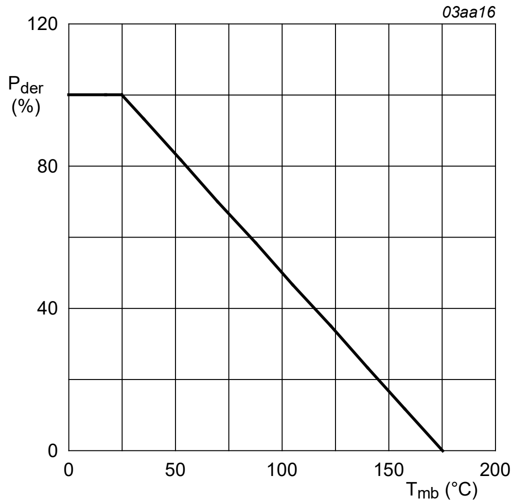
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).T_j = 25 °C unless otherwise stated.

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	25 °C ≤ T_j ≤ 175 °C		-	40	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	333	W
I_D	drain current	V_{GS} = 10 V; T_{mb} = 25 °C	[1]	-	320	A
I_{DM}	peak drain current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	1810	A
T_{stg}	storage temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T_j	junction temperature			-55	175	°C
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq$ 10 µs; T_{mb} = 25 °C		-	1810	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$V_{sup} \leq$ 40 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	[2]	-	[tbd]	mJ

[1] 320 A continuous current will be demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.
[2] Protected by 100% test.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ C)}} \times 100\,\%$$

Fig. 1. Normalized total power dissipation as a function of mounting base temperature

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	-	0.45	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 2		-	50	-	K/W
		Fig. 3		-	125	-	K/W

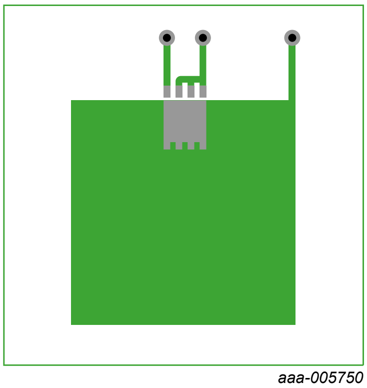


Fig. 2. **PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper**

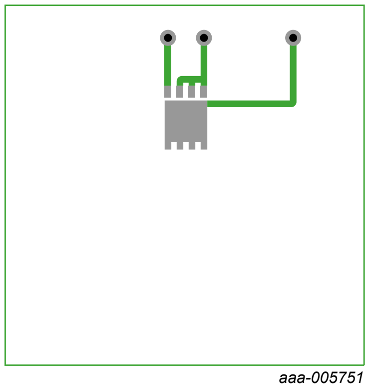


Fig. 3. **PCB layout for thermal resistance junction to ambient minimum footprint;FR4 board; 2oz copper**

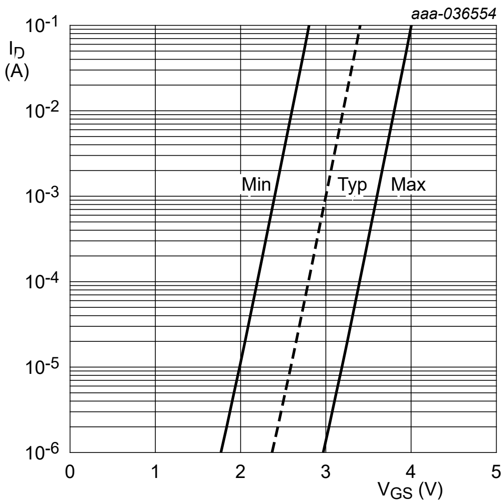
10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V; T_j = 25 °C		40	43	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -40 °C		-	40	-	V
		I_D = 250 µA; V_{GS} = 0 V; T_j = -55 °C		36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS}=V_{GS}; T_j = 25 °C; Fig. 4		2.4	3	3.6	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = -55 °C		-	-	4.3	V
		I_D = 1 mA; V_{DS}=V_{GS}; T_j = 175 °C		1	-	-	V
I_{DSS}	drain leakage current	V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 °C		-	0.1	1	µA
		V_{DS} = 16 V; V_{GS} = 0 V; T_j = 125 °C		-	1.1	10	µA
I_{GSS}	gate leakage current	V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C		0.48	0.68	0.81	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 105 °C; Fig. 5		[tbd]	[tbd]	[tbd]	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 125 °C; Fig. 5		[tbd]	[tbd]	[tbd]	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 175 °C; Fig. 5		[tbd]	[tbd]	1.67	mΩ
R_G	gate resistance	f = 1 MHz; T_j = 25 °C		0.34	0.85	2.12	Ω
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 6		109	182	255	nC
		I_D = 0 A; V_{DS} = 0 V		-	107	-	nC
Q_{GS}	gate-source charge	I_D = 25 A; V_{DS} = 32 V; V_{GS} = 10 V; T_j = 25 °C; Fig. 6		19	35	51	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			10	19	28	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			4	7.6	11	nC
Q_{GD}	gate-drain charge			17	57	96	nC

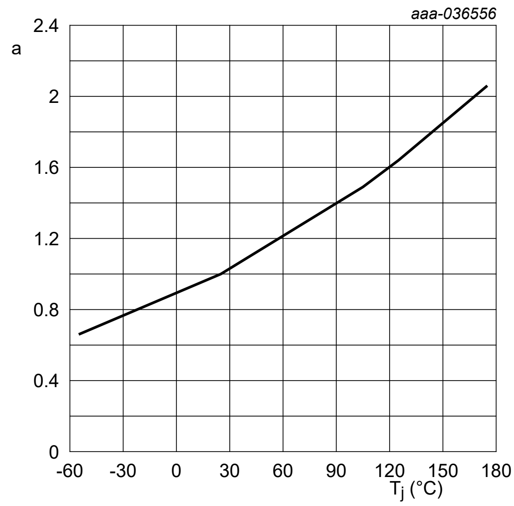
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_{GS(pl)}$	gate-source plateau voltage	I_D = 25 A; V_{DS} = 32 V; T_j = 25 °C; Fig. 6		-	4.1	-	V
C_{iss}	input capacitance	V_{DS} = 25 V; V_{GS} = 0 V; f = 1 MHz; T_j = 25 °C		6131	10219	14307	pF
C_{oss}	output capacitance			1571	2244	2917	pF
C_{rss}	reverse transfer capacitance			340	850	1360	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω; T_j = 25 °C		-	[tbd]	-	ns
t_r	rise time			-	[tbd]	-	ns
$t_{d(off)}$	turn-off delay time			-	[tbd]	-	ns
t_f	fall time			-	[tbd]	-	ns
Source-drain diode							
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C		-	0.79	1	V
t_{rr}	reverse recovery time	I_S = 25 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 20 V; T_j = 25 °C; Fig. 7		-	[tbd]	-	ns
Q_r	recovered charge		[1]	-	[tbd]	-	nC

[1] includes capacitive recovery



T_j = 25 °C; V_{DS} = 5 V

Fig. 4. Sub-threshold drain current as a function of gate-source voltage



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig. 5. Normalized drain-source on-state resistance factor as a function of junction temperature

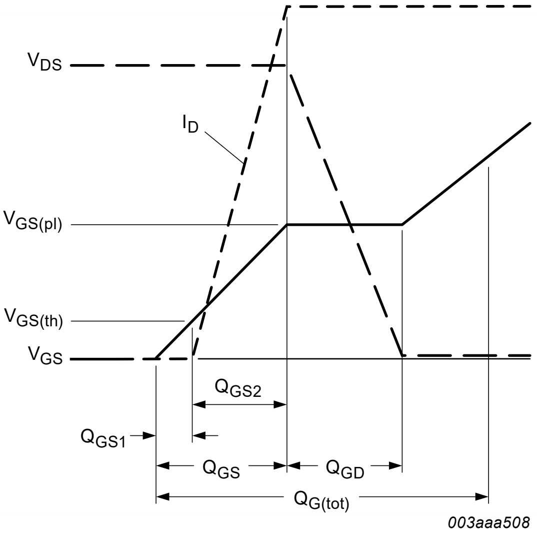


Fig. 6. Gate charge waveform definitions

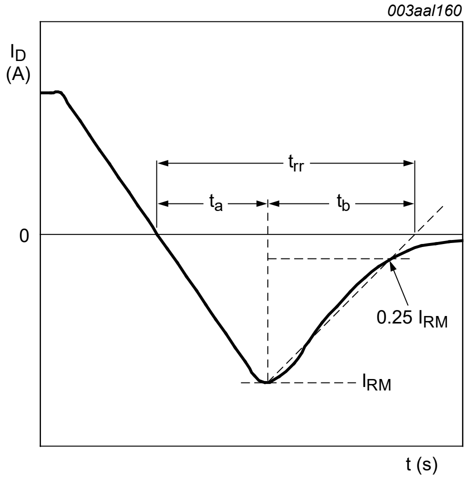
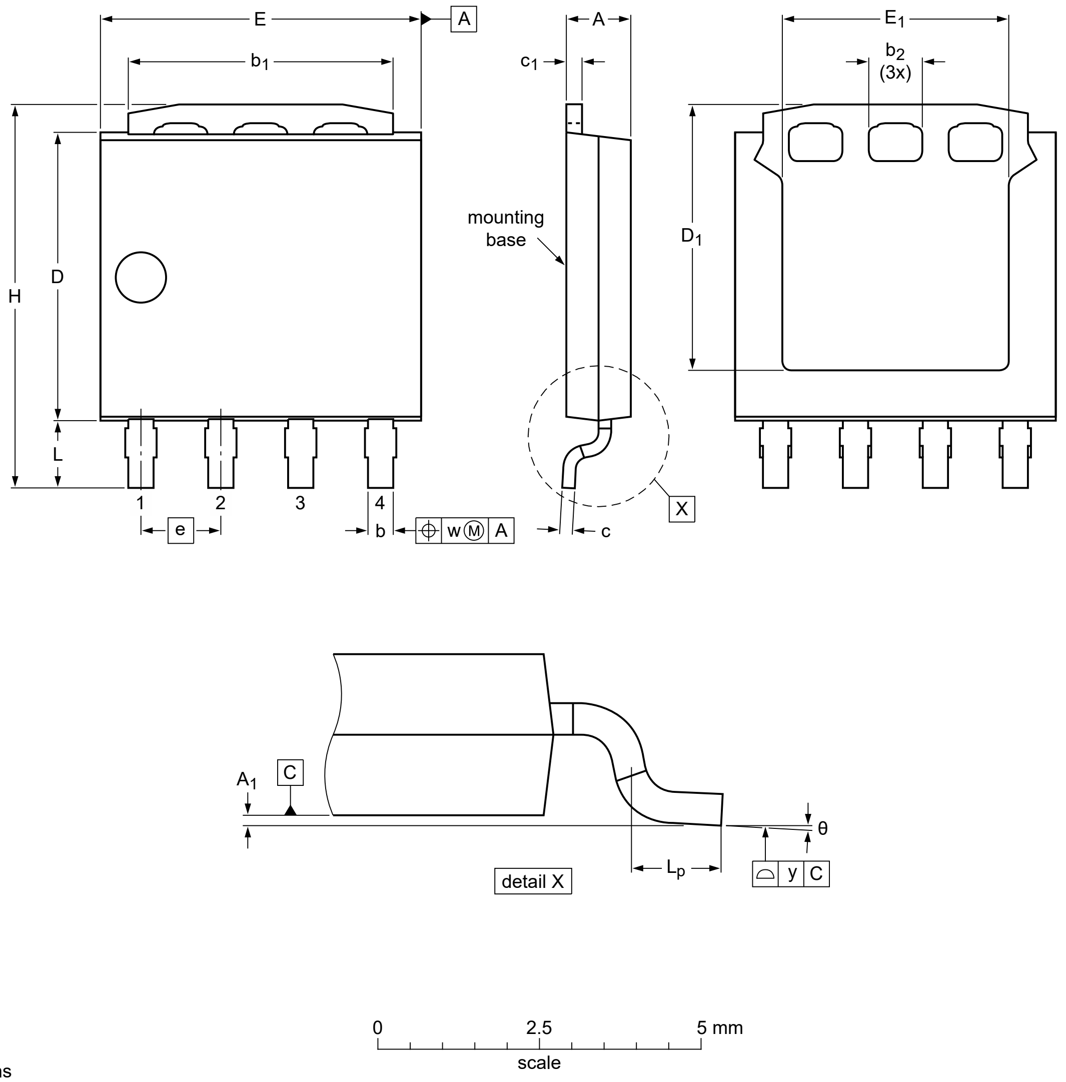


Fig. 7. Reverse recovery timing definition

11. Package outline

Plastic single-ended surface-mounted package (LFPAK56E); 4 leads **SOT1023**



Dimensions

Unit		A	A_1	b	b_1	b_2	c	c_1	D(1)	D_1(1)	E(1)	E_1(1)	e	H	L	L_p	w	y	θ
mm	max	1.10	0.15	0.50	4.41		0.25	0.30	4.70	4.45	5.30	3.7		6.2	1.3	0.85			8°
	nom					0.85							1.27				0.25	0.1	
	min	0.95	0.00	0.35	3.62		0.19	0.24	4.45		4.95	3.5		5.9	0.8	0.40			0°

Note
1. Plastic or metal protrusions of 0.15 mm per side are not included.

sot1023_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1023						~~13-03-05~~ 17-07-31

Fig. 8. Package outline LFPAK56E; Power-SO8 (SOT1023)

12. Soldering

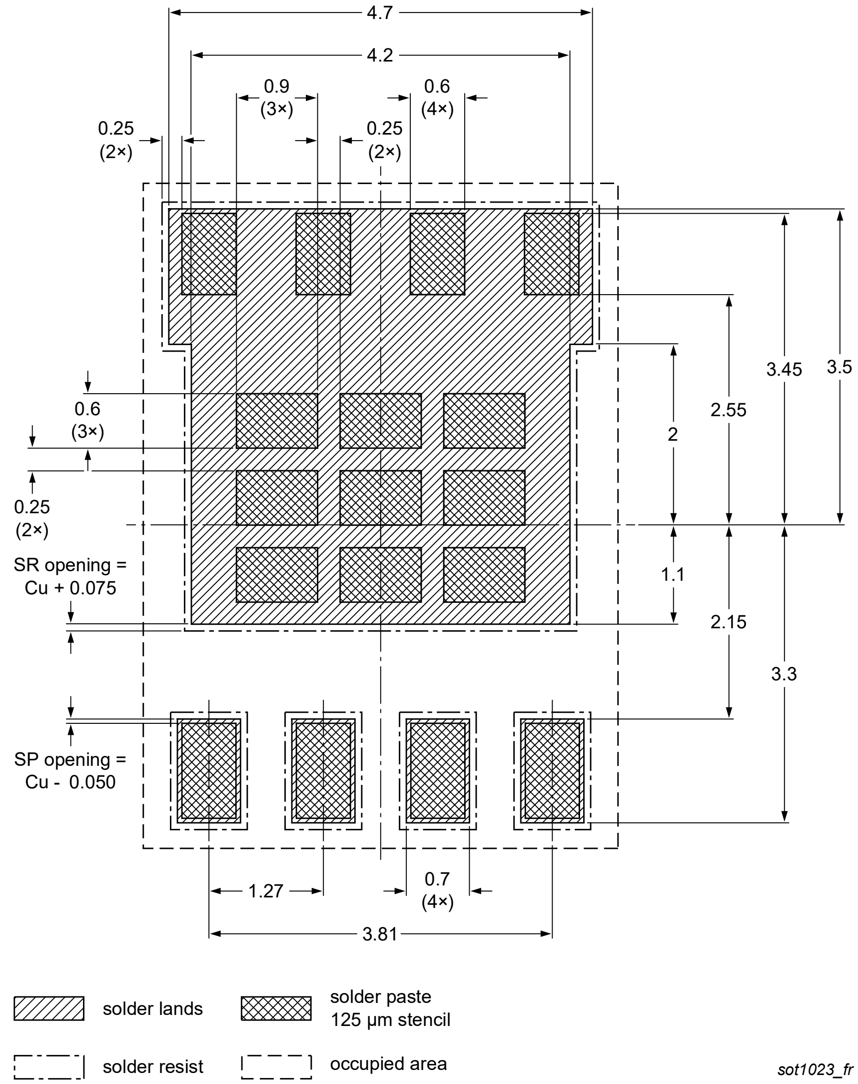


Fig. 9. Reflow soldering footprint for LFPAK56E; Power-SO8 (SOT1023)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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