HEF40175B

Quad D-type flip-flop

Rev. 11 — 8 August 2024 Product data sheet

1. General description

The HEF40175B is a quad positive edge triggered D-type flip-flop with four data (Dn) inputs, common clock (CP) and asynchronous master reset ($\overline{MR}$) inputs, and complementary Qn and $\overline{Q}$n outputs. When $\overline{MR}$ is HIGH data at the D-input that meets the set-up and hold time requirements on the LOW-to-HIGH clock transition will be stored in the flip-flop and appear at the Q output. When LOW, $\overline{MR}$ resets all flip-flops (Qn = LOW, $\overline{Q}$n = HIGH), independent of CP and Dn. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

2. Features and benefits

- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85°C and from -40 °C to +125 °C

3. Applications

- Shift registers
- Buffer/storage register
- Pattern generator

4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF40175BT	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
HEF40175BTT	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

5. Functional diagram

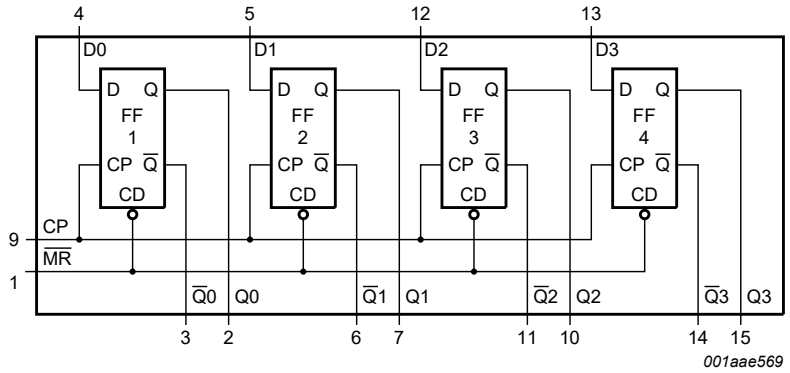


Fig. 1. Functional diagram

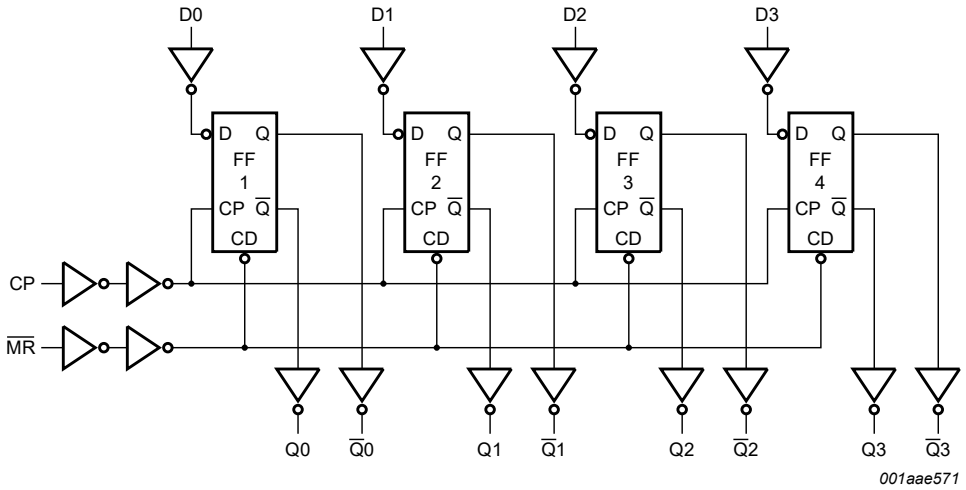
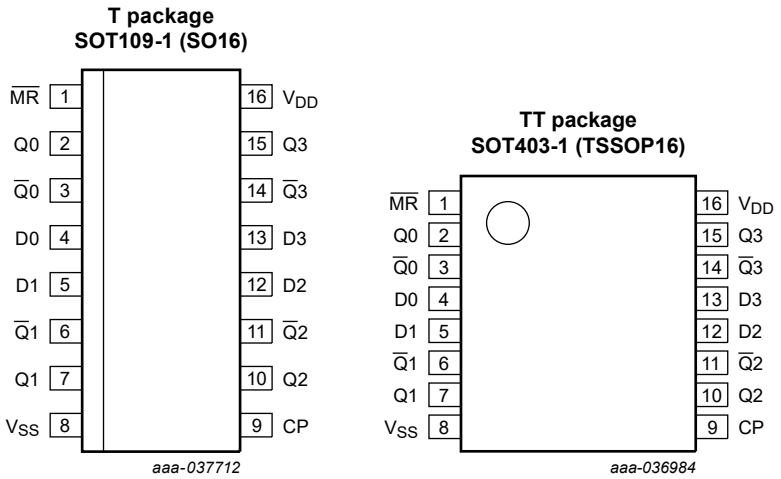


Fig. 2. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{MR}$	1	master reset input (active LOW)
Q0, Q1, Q2, Q3	2, 7, 10, 15	buffered output
$\overline{Q0}$, $\overline{Q1}$, $\overline{Q2}$, $\overline{Q3}$	3, 6, 11, 14	complementary buffered output
D0, D1, D2, D3	4, 5, 12, 13	data input
V_{SS}	8	ground supply voltage
CP	9	clock input (LOW-to-HIGH edge-triggered)
V_{DD}	16	supply voltage

7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;
↑ = positive-going transition; ↓ = negative-going transition.

Input			Output	
CP	**Dn**	**$\overline{MR}$**	**Qn**	**$\overline{Q}$n**
↑	H	H	H	L
↑	L	H	L	H
↓	X	H	no change	no change
X	X	L	L	H

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I_{IK}	input clamping current	V_I < -0.5 V or V_I > V_{DD} + 0.5 V	-	±10	mA
V_I	input voltage		-0.5	V_{DD} + 0.5	V
I_{OK}	output clamping current	V_O < -0.5 V or V_O > V_{DD} + 0.5 V	-	±10	mA
$I_{I/O}$	input/output current		-	±10	mA
I_{DD}	supply current		-	50	mA
T_{stg}	storage temperature		-65	+150	°C
T_{amb}	ambient temperature		-40	+125	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C [1]	-	500	mW
P	power dissipation	per output	-	100	mW

[1] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

10. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = -40 °C		T_{amb} = +25 °C		T_{amb} = +85 °C		T_{amb} = +125 °C		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		V_O = 4.6 V	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		V_O = 9.5 V	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		V_O = 13.5 V	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		V_O = 1.5 V	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
I_I	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	µA
I_{DD}	supply current	all valid input combinations; $\|I_O\|$= 0 A	5 V	-	1.0	-	1.0	-	30	-	30	µA
			10 V	-	2.0	-	2.0	-	60	-	60	µA
			15 V	-	4.0	-	4.0	-	120	-	120	µA
C_I	input capacitance		-	-	-	-	-	7.5	-	-	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C unless otherwise specified; for test circuit see Fig. 4.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula[1]	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to Qn or $\overline{Q}$n; see Fig. 3	5 V	53 ns + (0.55 ns/pF) C_L	-	80	160	ns
			10 V	24 ns + (0.23 ns/pF) C_L	-	35	70	ns
			15 V	17 ns + (0.16 ns/pF) C_L	-	25	50	ns
		$\overline{MR}$ to Qn; see Fig. 3	5 V	48 ns + (0.55 ns/pF) C_L	-	75	155	ns
			10 V	19 ns + (0.23 ns/pF) C_L	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C_L	-	25	50	ns
t_{PLH}	LOW to HIGH propagation delay	CP to Qn or $\overline{Q}$n; see Fig. 3	5 V	43 ns + (0.55 ns/pF) C_L	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF) C_L	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C_L	-	25	45	ns
		$\overline{MR}$ to $\overline{Q}$n; see Fig. 3	5 V	43 ns + (0.55 ns/pF) C_L	-	70	140	ns
			10 V	19 ns + (0.23 ns/pF) C_L	-	30	65	ns
			15 V	17 ns + (0.16 ns/pF) C_L	-	25	50	ns
t_t	transition time	see Fig. 3	5 V	10 ns + (1.00 ns/pF) C_L	-	60	120	ns
			10 V	9 ns + (0.42 ns/pF) C_L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF) C_L	-	20	40	ns
t_{su}	set-up time	Dn to CP; see Fig. 3	5 V		60	30	-	ns
			10 V		20	10	-	ns
			15 V		15	5	-	ns
t_h	hold time	Dn to CP; see Fig. 3	5 V		+25	-5	-	ns
			10 V		10	0	-	ns
			15 V		10	0	-	ns
t_W	pulse width	CP input LOW; minimum pulse width; see Fig. 3	5 V		90	45	-	ns
			10 V		35	15	-	ns
			15 V		25	10	-	ns
		$\overline{MR}$ input LOW; minimum pulse width; see Fig. 3	5 V		80	40	-	ns
			10 V		30	15	-	ns
			15 V		20	10	-	ns
t_{rec}	recovery time	$\overline{MR}$ input; see Fig. 3	5 V		0	-30	-	ns
			10 V		0	-20	-	ns
			15 V		0	-15	-	ns
f_{max}	maximum frequency		5 V		5	11	-	MHz
			10 V		15	30	-	MHz
			15 V		20	45	-	MHz

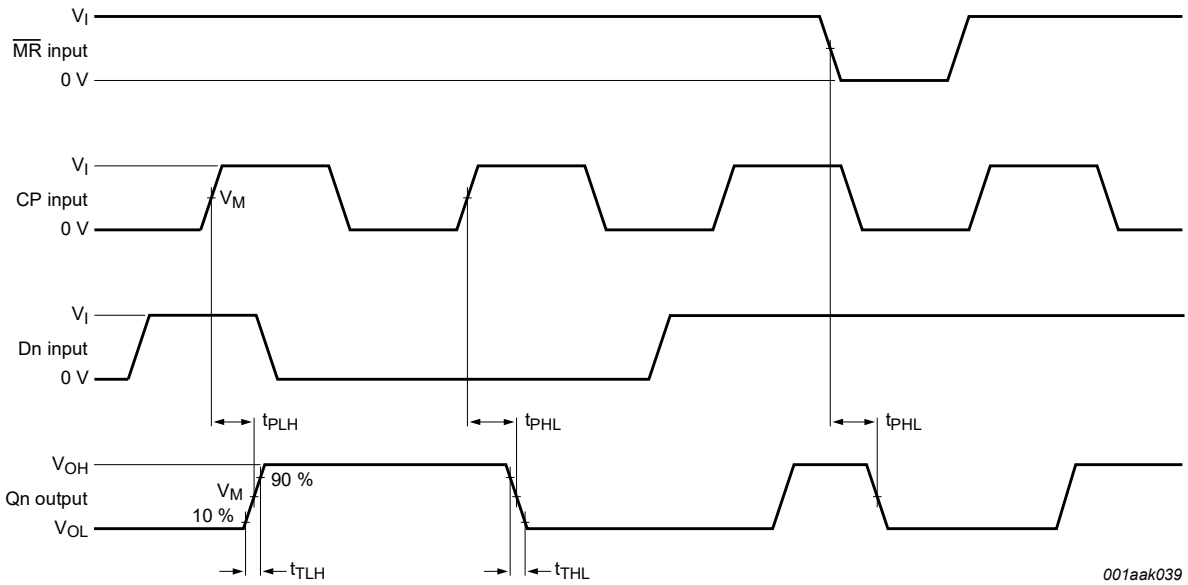
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formula shown (C_L in pF).

Table 8. Dynamic power dissipation P_D

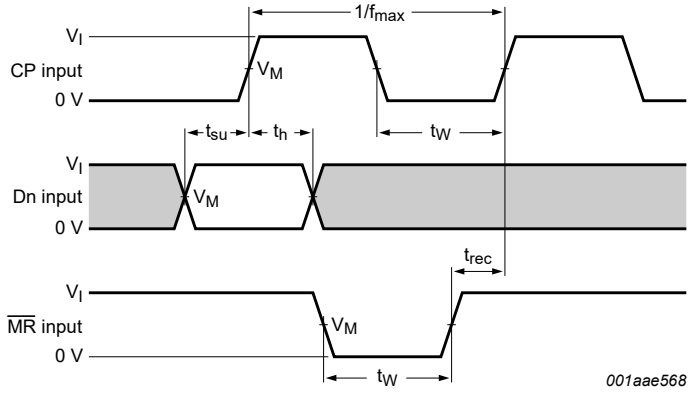
P_D can be calculated from the formulas shown. V_{SS} = 0 V; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	where:
P_D	dynamic power dissipation	5 V	$P_D = 2000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz; f_o = output frequency in MHz; C_L = output load capacitance in pF; V_{DD} = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 8400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 22500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

11.1. Waveforms and test circuit



a. CP and $\overline{MR}$ to Qn propagation delays and Qn transition times

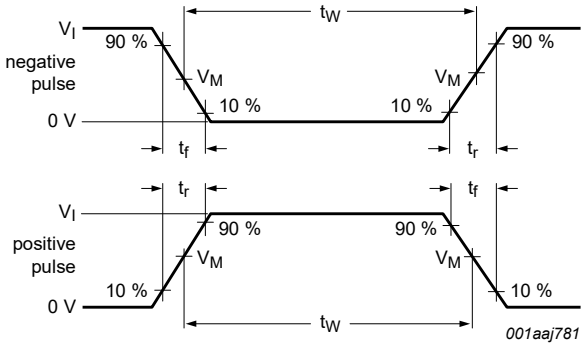


b. Minimum pulse widths for CP and $\overline{MR}$, $\overline{MR}$ to CP recovery time, and set-up and hold time for Dn to CP
V_{OH} and V_{OL} are typical output voltage levels that occur with the output load.
Set-up and hold times are shown as positive values but may be specified as negative values.
The shaded area are where input changes result in predicable output performance.
Measurement points are given in Table 9.

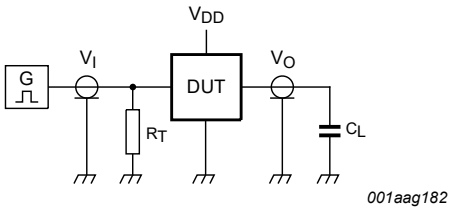
Fig. 3. Waveforms showing switching times

Table 9. Measurement points

Supply voltage	Input	Output
V_{DD}	V_M	V_M
5 V to 15 V	0.5 × V_{DD}	0.5 × V_{DD}



a. Input waveforms



b .Test circuit

Test and measurement data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance.

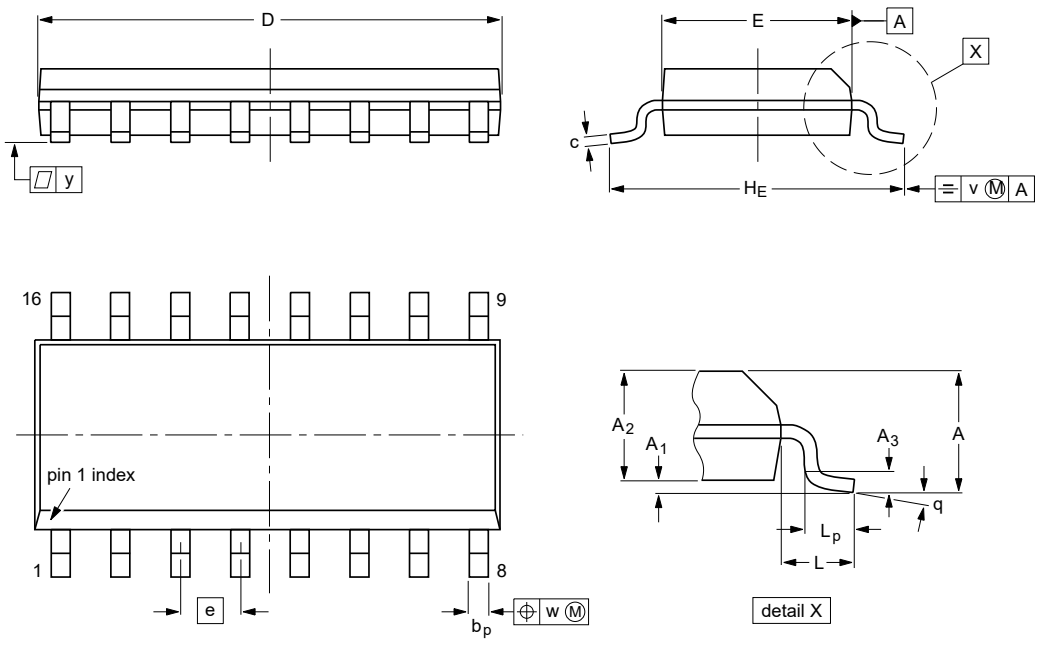
Fig. 4. Test circuit for measuring switching times

Table 10. Measurement points and test data

Supply voltage	Input		Load
V_{DD}	V_I	t_r, t_f	C_L
5 V to 15 V	V_{SS} or V_{DD}	≤ 20 ns	50 pF

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

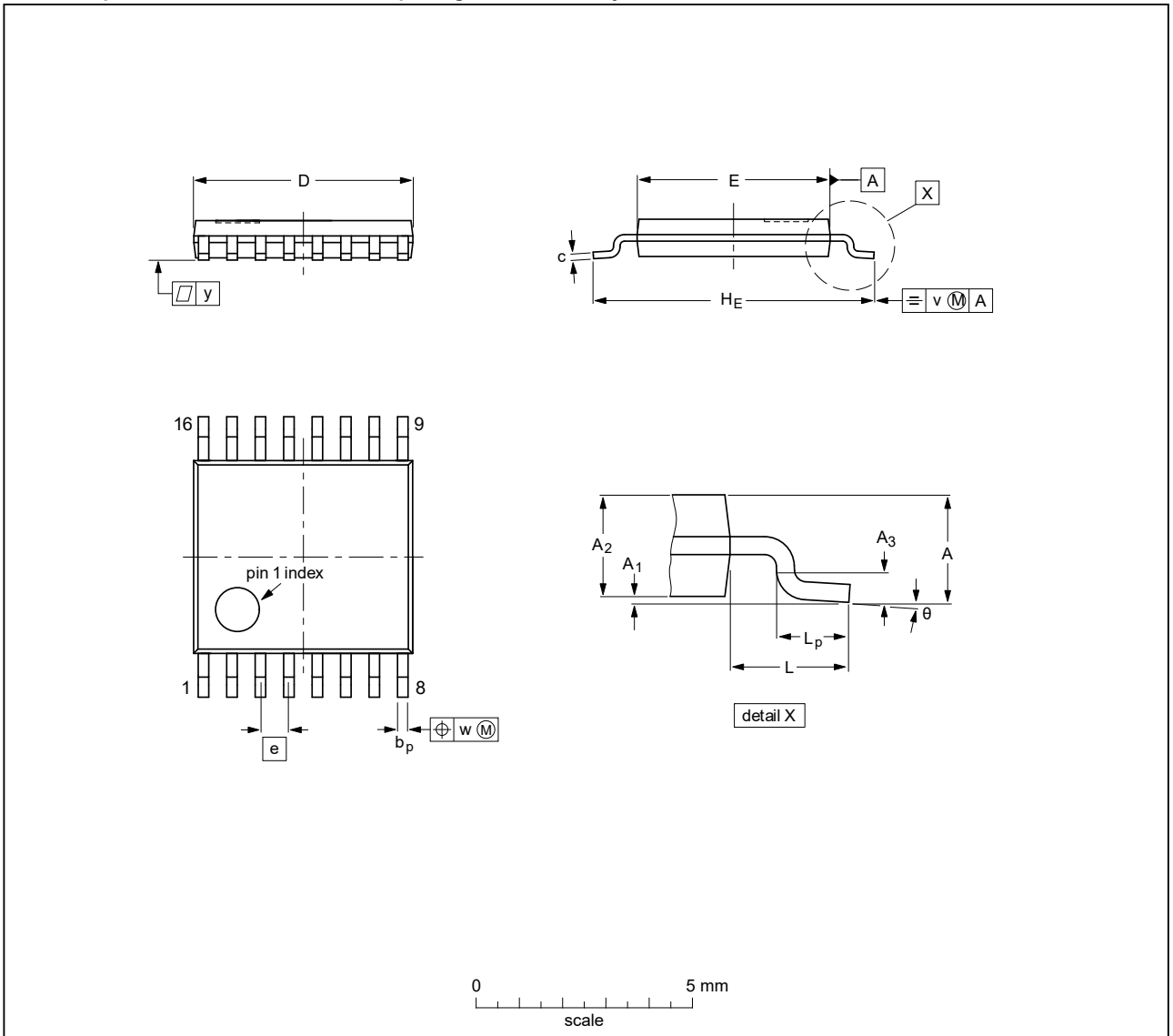
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 5. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
mm	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 6. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF40175B v.11	20240808	Product data sheet	-	HEF40175B v.10.1
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Fig. 5, Fig. 6: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153			
HEF40175B v.10.1	20231020	Product data sheet	-	HEF40175B v.9
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 1 and Section 2 updated. • Table 4: Derating values for P_{tot} total power dissipation updated.			
HEF40175B v.9	20160321	Product data sheet	-	HEF40175B v.8
Modifications:	• Type number HEF40175BP (SOT38-4) removed.			
HEF40175B v.8	20111121	Product data sheet	-	HEF40175B v.7
Modifications:	• Legal pages updated. • Changes in "General description", "Features and benefits" and "Applications".			
HEF40175B v.7	20110503	Product data sheet	-	HEF40175B v.6
HEF40175B v.6	20101214	Product data sheet	-	HEF40175B v.5
HEF40175B v.5	20100105	Product data sheet	-	HEF40175B v.4
HEF40175B v.4	20090813	Product data sheet	-	HEF40175B_CNV v.3
HEF40175B_CNV v.3	19950101	Product specification	-	HEF40175B_CNV v.2
HEF40175B_CNV v.2	19950101	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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