

74LVC4066-Q100

Quad bilateral switch

Rev. 4 — 22 February 2024

Product data sheet

1. General description

The 74LVC4066-Q100 is a high-speed Si-gate CMOS device.

The 74LVC4066-Q100 provides four single pole, single-throw analog switch functions. Each switch has two input/output terminals (nY and nZ) and an active HIGH enable input (nE). When nE is LOW, the analog switch is turned off.

Schmitt-trigger action at the enable inputs makes the circuit tolerant of slower input rise and fall times across the entire V_{CC} range from 1.65 V to 5.5 V.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
 - 7.5 Ω (typical) at $V_{CC} = 2.7$ V
 - 6.5 Ω (typical) at $V_{CC} = 3.3$ V
 - 6 Ω (typical) at $V_{CC} = 5$ V
- Switch current capability of 32 mA
- High noise immunity
- CMOS low-power consumption
- Direct interface TTL-levels
- Latch-up performance exceeds 250 mA
- Enable inputs accept voltages up to 5 V
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- DHVQFN package with Side-Wettable Flanks enabling Automatic Optical Inspection (AOI) of solder joints

3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC4066D-Q100	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74LVC4066PW-Q100	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74LVC4066BQ-Q100	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1

4. Functional diagram

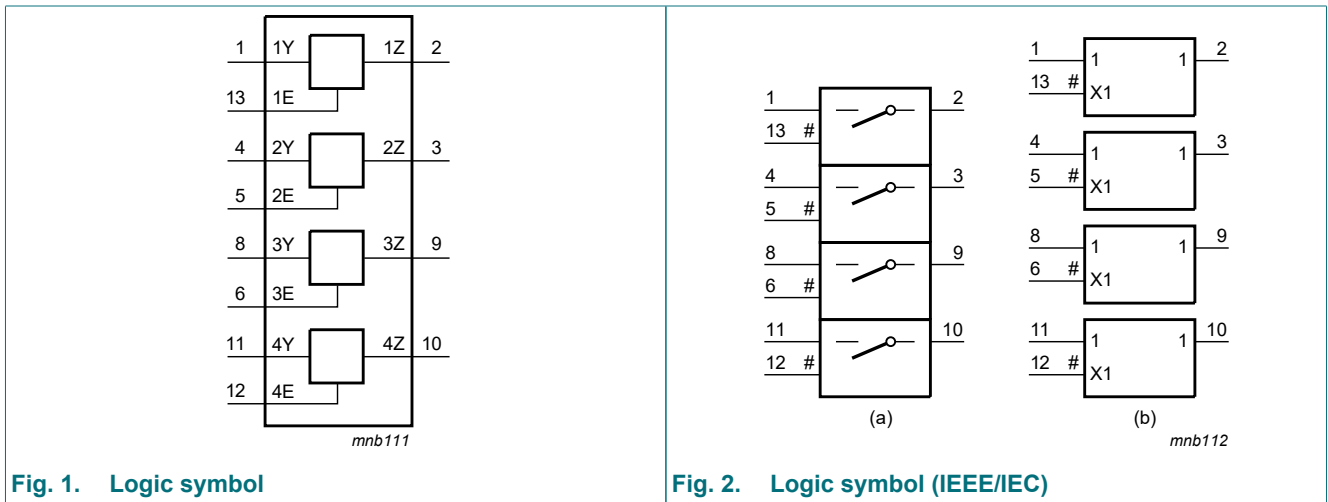


Fig. 1. Logic symbol

Fig. 2. Logic symbol (IEEE/IEC)

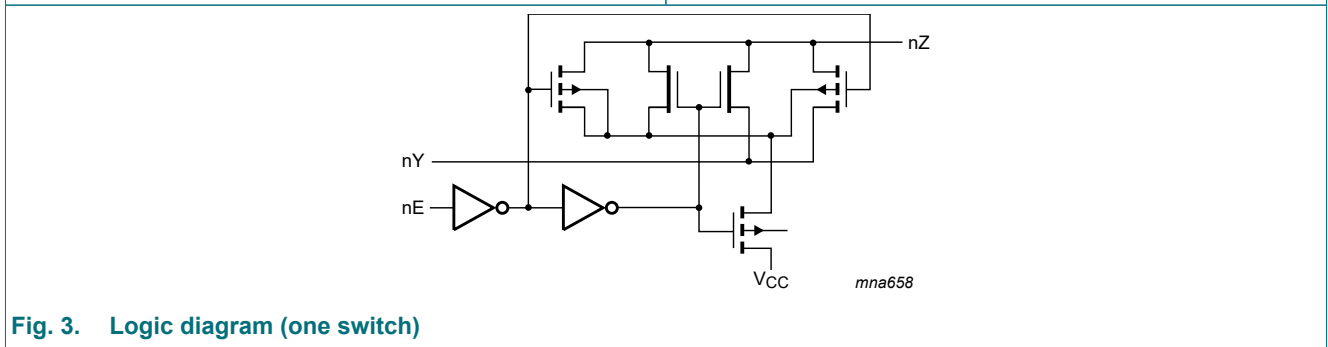
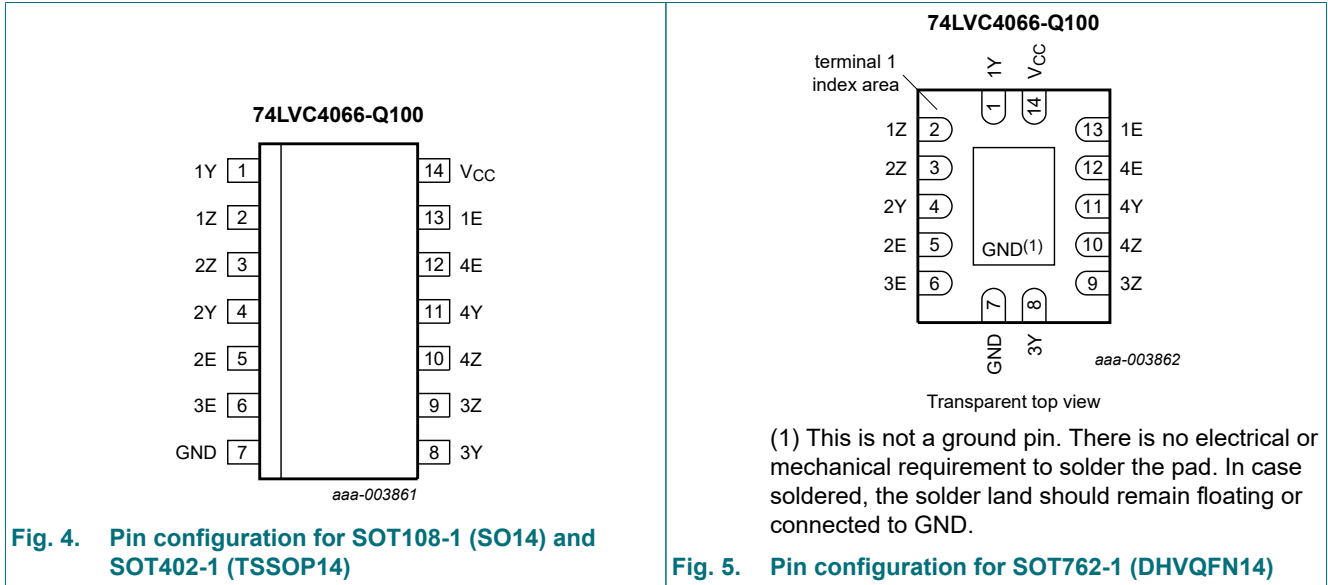


Fig. 3. Logic diagram (one switch)

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Y, 2Y, 3Y, 4Y	1, 4, 8, 11	independent input/output
1Z, 2Z, 3Z, 4Z	2, 3, 9, 10	independent output/input
1E, 2E, 3E, 4E	13, 5, 6, 12	enable input (active HIGH)
GND	7	ground (0 V)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Input nE	Switch
L	OFF
H	ON

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+6.5	V
V_I	input voltage	[1]	-0.5	+6.5	V
I_{IK}	input clamping current	$V_I < -0.5 \text{ V}$ or $V_I < V_{CC} + 0.5 \text{ V}$	-50	-	mA
I_{SK}	switch clamping current	$V_I < -0.5 \text{ V}$ or $V_I < V_{CC} + 0.5 \text{ V}$	-	± 50	mA
V_{SW}	switch voltage	enable and disable mode [2]	-0.5	+6.5	V
I_{SW}	switch current	$-0.5 < V_{SW} < V_{CC} + 0.5 \text{ V}$	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40 \text{ °C}$ to $+125 \text{ °C}$ [3]	-	500	mW

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		1.65	-	5.5	V
V_I	input voltage		0	-	5.5	V
V_{SW}	switch voltage	[1]	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	-	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65 \text{ V}$ to 2.7 V [2]	-	-	20	ns/V
		$V_{CC} = 2.7 \text{ V}$ to 5.5 V [2]	-	-	10	ns/V

[1] To avoid sinking GND current from terminal nZ when switch current flows in terminal nY, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal nZ, no GND current will flow from terminal nY. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

9. Static characteristics

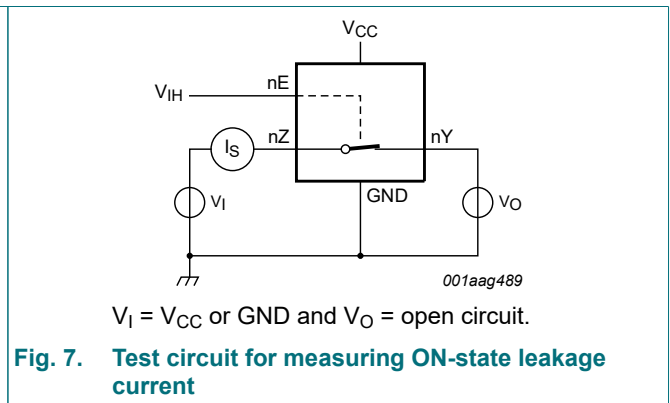
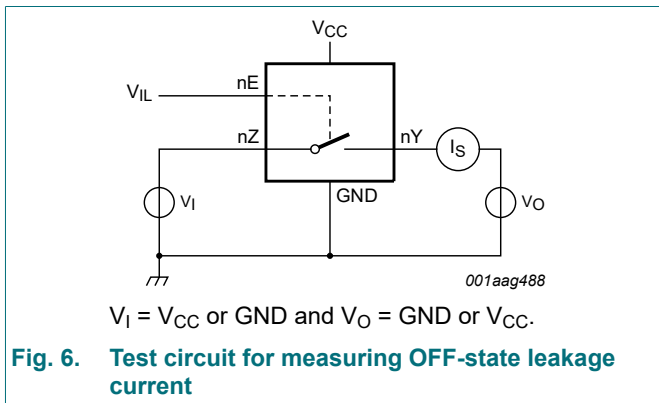
Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65V _{CC}	-	-	0.65V _{CC}	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	2.0	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	0.7V _{CC}	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35V _{CC}	-	0.35V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	-	0.3V _{CC}	V
I _I	input leakage current	pin nE; V _{CC} = 5.5 V; V _I = 5.5 V or GND [2]	-	±0.1	±5	-	±20	µA
I _{S(OFF)}	OFF-state leakage current	V _{SW} = V _{CC} - GND; V _{CC} = 5.5 V; see Fig. 6 [2]	-	±0.1	±5	-	±20	µA
I _{S(ON)}	ON-state leakage current	V _{SW} = V _{CC} - GND; V _{CC} = 5.5 V; see Fig. 7 [2]	-	±0.1	±5	-	±20	µA
I _{CC}	supply current	V _I = V _{CC} or GND; V _{SW} = GND or V _{CC} ; V _{CC} = 5.5 V [2]	-	0.1	10	-	40	µA
ΔI _{CC}	additional supply current	pin nE; V _I = V _{CC} - 0.6 V; V _{CC} = 5.5 V; V _{SW} = GND or V _{CC} [2]	-	5	500	-	5000	µA
C _I	input capacitance		-	12.5	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance		-	8.0	-	-	-	pF
C _{S(ON)}	ON-state capacitance		-	14.0	-	-	-	pF

- [1] All typical values are measured at T_{amb} = 25 °C.
- [2] These typical values are measured at V_{CC} = 3.3 V.

9.1. Test circuits



9.2. ON resistance

Table 7. ON resistance

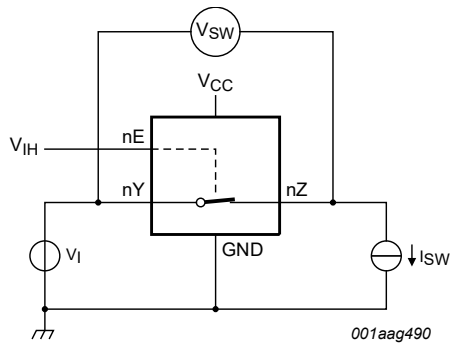
At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see [Fig. 9](#) to [Fig. 14](#).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON(peak)}	ON resistance (peak)	V _I = GND to V _{CC} ; see Fig. 8						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	34.0	130	-	195	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	12.0	30	-	45	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	10.4	25	-	38	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	7.8	20	-	30	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	6.2	15	-	23	Ω
R _{ON(rail)}	ON resistance (rail)	V _I = GND; see Fig. 8						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	8.2	18	-	27	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.1	16	-	24	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	6.9	14	-	21	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.5	12	-	18	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	5.8	10	-	15	Ω
		V _I = V _{CC} ; see Fig. 8						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	10.4	30	-	45	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	7.6	20	-	30	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	7.0	18	-	27	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	6.1	15	-	23	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	4.9	10	-	15	Ω
R _{ON(flat)}	ON resistance (flatness)	V _I = GND to V _{CC} [2]						
		I _{SW} = 4 mA; V _{CC} = 1.65 V to 1.95 V	-	26.0	-	-	-	Ω
		I _{SW} = 8 mA; V _{CC} = 2.3 V to 2.7 V	-	5.0	-	-	-	Ω
		I _{SW} = 12 mA; V _{CC} = 2.7 V	-	3.5	-	-	-	Ω
		I _{SW} = 24 mA; V _{CC} = 3 V to 3.6 V	-	2.0	-	-	-	Ω
		I _{SW} = 32 mA; V _{CC} = 4.5 V to 5.5 V	-	1.5	-	-	-	Ω

[1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.

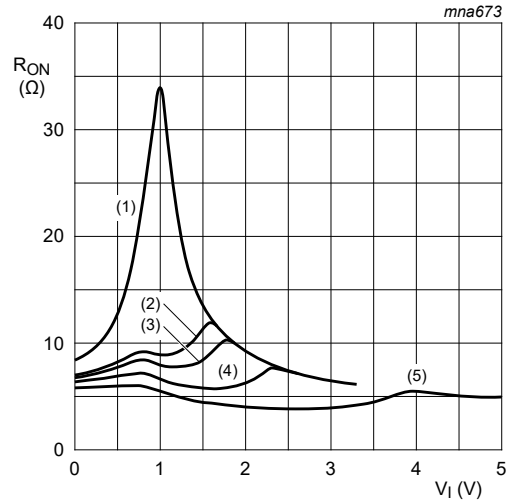
[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical V_{CC} and temperature.

9.3. ON resistance test circuit and graphs



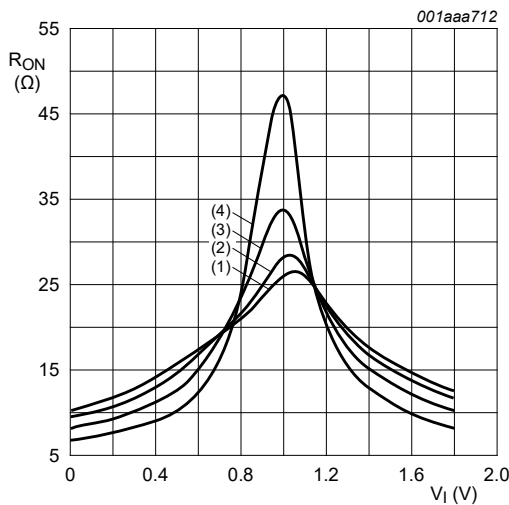
$R_{ON} = V_{SW} / I_{SW}$.

Fig. 8. Test circuit for measuring ON resistance



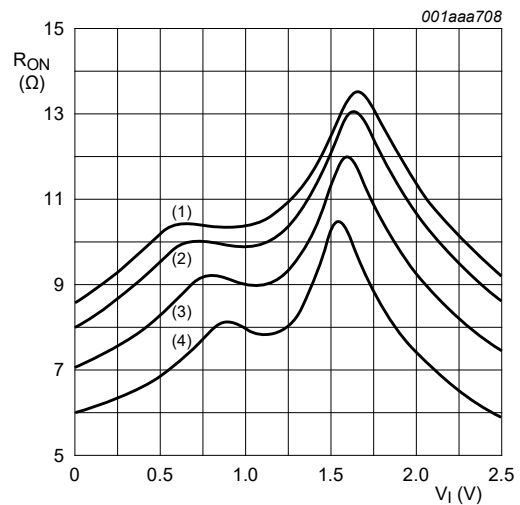
- (1) $V_{CC} = 1.8$ V.
- (2) $V_{CC} = 2.5$ V.
- (3) $V_{CC} = 2.7$ V.
- (4) $V_{CC} = 3.3$ V.
- (5) $V_{CC} = 5.0$ V.

Fig. 9. Typical ON resistance as a function of input voltage; $T_{amb} = 25$ °C



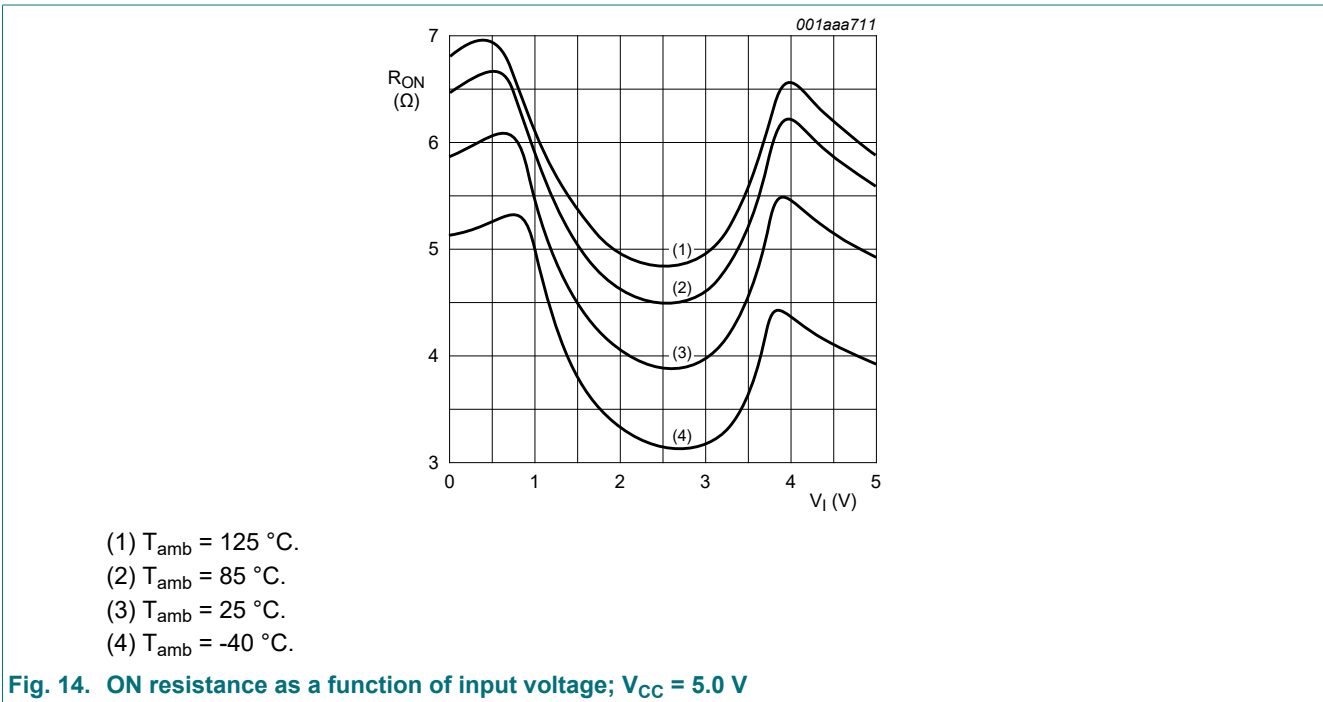
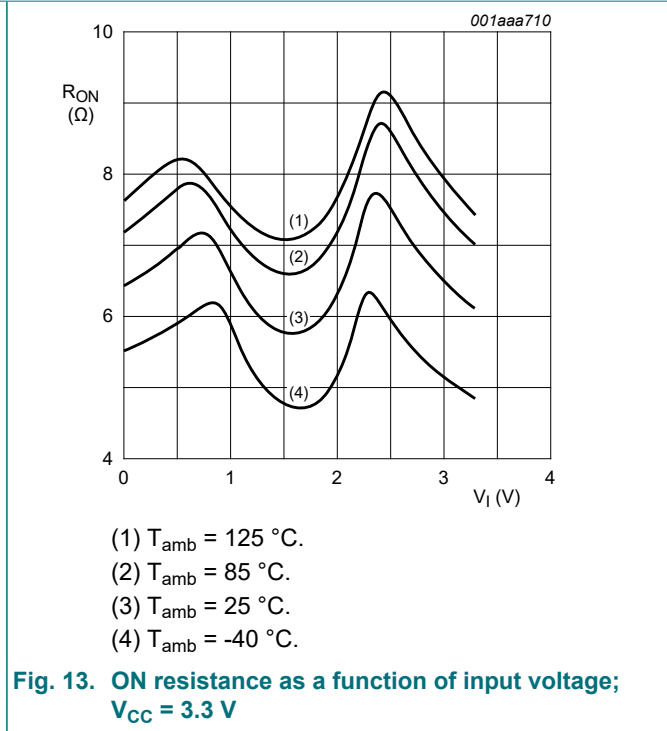
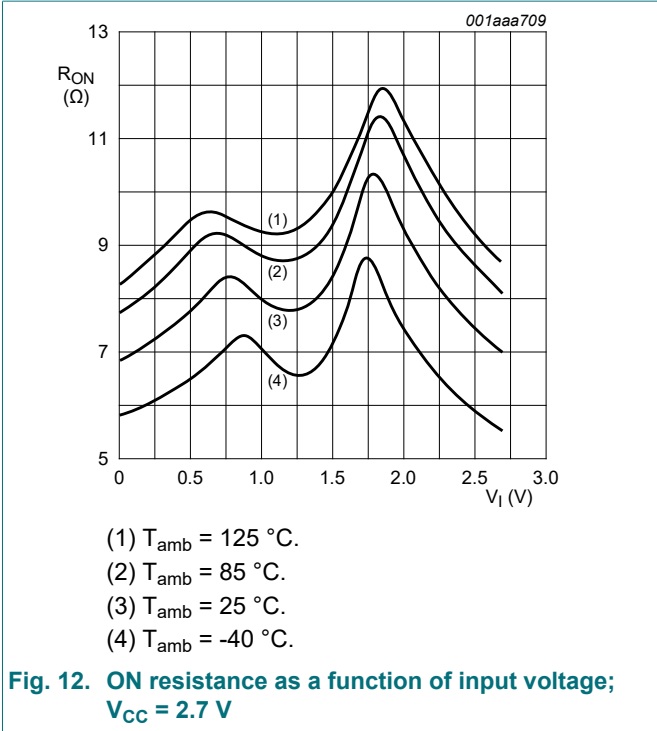
- (1) $T_{amb} = 125$ °C.
- (2) $T_{amb} = 85$ °C.
- (3) $T_{amb} = 25$ °C.
- (4) $T_{amb} = -40$ °C.

Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 1.8$ V



- (1) $T_{amb} = 125$ °C.
- (2) $T_{amb} = 85$ °C.
- (3) $T_{amb} = 25$ °C.
- (4) $T_{amb} = -40$ °C.

Fig. 11. ON resistance as a function of input voltage; $V_{CC} = 2.5$ V



10. Dynamic characteristics

Table 8. Dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 17.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nY to nZ or nZ to nY; see Fig. 15 [2] [3]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	0.8	2.0	-	3.0	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	0.4	1.2	-	2.0	ns
		$V_{CC} = 2.7 \text{ V}$	-	0.4	1.0	-	1.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	0.3	0.8	-	1.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	0.2	0.6	-	1.0	ns
t_{en}	enable time	nE to nY or nZ; see Fig. 16 [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.3	10	1.0	12.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	3.0	5.6	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.6	5.0	1.0	6.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.5	4.4	1.0	5.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	1.9	3.9	1.0	5.0	ns
t_{dis}	disable time	nE to nY or nZ; see Fig. 16 [5]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	4.2	9.0	1.0	11.5	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.0	2.4	5.5	1.0	7.0	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.6	6.5	1.0	8.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	3.4	6.0	1.0	7.5	ns
		$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	1.0	2.5	5.0	1.0	6.5	ns
C_{PD}	power dissipation capacitance	$C_L = 50 \text{ pF}$; $f_i = 10 \text{ MHz}$; $V_I = \text{GND to } V_{CC}$ [6]						
		$V_{CC} = 2.5 \text{ V}$	-	11.0	-	-	-	pF
		$V_{CC} = 3.3 \text{ V}$	-	12.5	-	-	-	pF
		$V_{CC} = 5.0 \text{ V}$	-	15.6	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and nominal V_{CC} .

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] t_{en} is the same as t_{PZH} and t_{PZL} .

[5] t_{dis} is the same as t_{PLZ} and t_{PHZ} .

[6] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\} \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

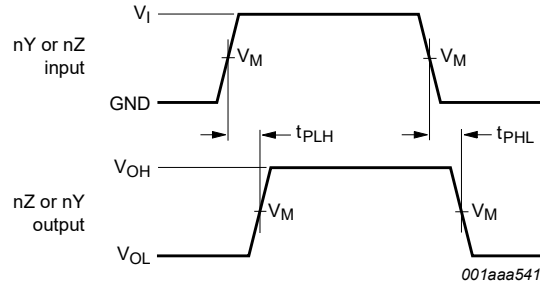
$C_{S(ON)}$ = maximum ON-state switch capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma\{(C_L + C_{S(ON)}) \times V_{CC}^2 \times f_o\}$ = sum of the outputs.

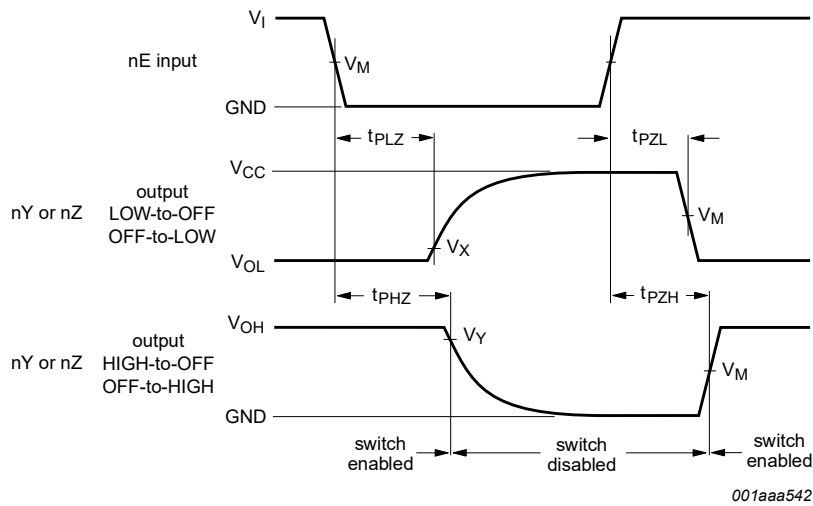
10.1. Waveforms and test circuit



Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 15. Input (nY or nZ) to output (nZ or nY) propagation delays



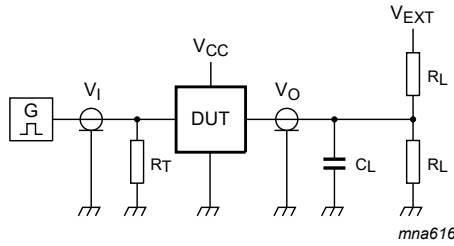
Measurement points are given in [Table 9](#).

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig. 16. Enable and disable times

Table 9. Measurement points

Supply voltage	Input	Output		
V_{CC}	V_M	V_M	V_X	V_Y
1.65 V to 1.95 V	$0.5V_{CC}$	$0.5 V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.3 V to 2.7 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 V$	$V_{OH} - 0.15 V$
2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
3.0 V to 3.6 V	1.5 V	1.5 V	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$
4.5 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.3 V$	$V_{OH} - 0.3 V$



Test data is given in [Table 10](#).

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

C_L = Load capacitance including jig and probe capacitance.

R_L = Load resistance.

V_{EXT} = External voltage for measuring switching times.

Fig. 17. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
1.65 V to 1.95 V	V_{CC}	≤ 2.0 ns	30 pF	1 k Ω	open	GND	$2V_{CC}$
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	GND	$2V_{CC}$
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	GND	6 V
4.5 V to 5.5 V	V_{CC}	≤ 2.5 ns	50 pF	500 Ω	open	GND	$2V_{CC}$

10.2. Additional dynamic characteristics

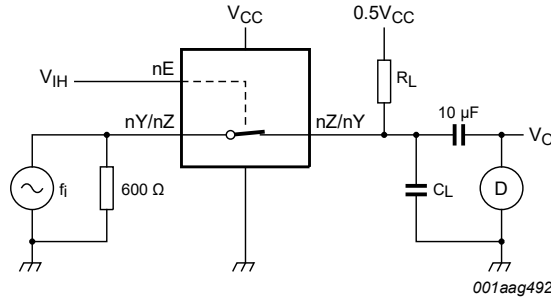
Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
THD	total harmonic distortion	$R_L = 10$ k Ω ; $C_L = 50$ pF; $f_i = 1$ kHz; see Fig. 18					
		$V_{CC} = 1.65$ V	-	0.032	-	%	
		$V_{CC} = 2.3$ V	-	0.008	-	%	
		$V_{CC} = 3$ V	-	0.006	-	%	
		$V_{CC} = 4.5$ V	-	0.005	-	%	
		$R_L = 10$ k Ω ; $C_L = 50$ pF; $f_i = 10$ kHz; see Fig. 18					
		$V_{CC} = 1.65$ V	-	0.068	-	%	
		$V_{CC} = 2.3$ V	-	0.009	-	%	
		$V_{CC} = 3$ V	-	0.008	-	%	
$V_{CC} = 4.5$ V	-	0.006	-	%			

Symbol	Parameter	Conditions	Min	Typ	Max	Unit		
$f_{(-3dB)}$	-3 dB frequency response	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; see Fig. 19						
		$V_{CC} = 1.65 \text{ V}$	-	170	-	MHz		
		$V_{CC} = 2.3 \text{ V}$	-	210	-	MHz		
		$V_{CC} = 3 \text{ V}$	-	212	-	MHz		
		$V_{CC} = 4.5 \text{ V}$	-	215	-	MHz		
		$R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; see Fig. 19						
		$V_{CC} = 1.65 \text{ V}$	-	> 500	-	MHz		
		$V_{CC} = 2.3 \text{ V}$	-	> 500	-	MHz		
		$V_{CC} = 3 \text{ V}$	-	> 500	-	MHz		
		$V_{CC} = 4.5 \text{ V}$	-	> 500	-	MHz		
α_{iso}	isolation (OFF-state)	$R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 20						
		$V_{CC} = 1.65 \text{ V}$	-	-46	-	dB		
		$V_{CC} = 2.3 \text{ V}$	-	-46	-	dB		
		$V_{CC} = 3 \text{ V}$	-	-46	-	dB		
		$V_{CC} = 4.5 \text{ V}$	-	-46	-	dB		
		$R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 20						
		$V_{CC} = 1.65 \text{ V}$	-	-42	-	dB		
		$V_{CC} = 2.3 \text{ V}$	-	-42	-	dB		
		$V_{CC} = 3 \text{ V}$	-	-42	-	dB		
		$V_{CC} = 4.5 \text{ V}$	-	-42	-	dB		
V_{ct}	crosstalk voltage	between digital inputs and switch; $R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; $t_r = t_f = 2 \text{ ns}$; see Fig. 21						
		$V_{CC} = 1.65 \text{ V}$	-	69	-	mV		
		$V_{CC} = 2.3 \text{ V}$	-	87	-	mV		
		$V_{CC} = 3 \text{ V}$	-	156	-	mV		
		$V_{CC} = 4.5 \text{ V}$	-	302	-	mV		
Xtalk	crosstalk	between switches; $R_L = 600 \Omega$; $C_L = 50 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 22						
		$V_{CC} = 1.65 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 2.3 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 3 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 4.5 \text{ V}$	-	-58	-	dB		
		between switches; $R_L = 50 \Omega$; $C_L = 5 \text{ pF}$; $f_i = 1 \text{ MHz}$; see Fig. 22						
		$V_{CC} = 1.65 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 2.3 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 3 \text{ V}$	-	-58	-	dB		
		$V_{CC} = 4.5 \text{ V}$	-	-58	-	dB		
		Q_{inj}	charge injection	$C_L = 0.1 \text{ nF}$; $V_{gen} = 0 \text{ V}$; $R_{gen} = 0 \Omega$; $f_i = 1 \text{ MHz}$; $R_L = 1 \text{ M}\Omega$; see Fig. 23				
				$V_{CC} = 1.8 \text{ V}$	-	3.3	-	pC
$V_{CC} = 2.5 \text{ V}$	-			4.1	-	pC		
$V_{CC} = 3.3 \text{ V}$	-			5.0	-	pC		
$V_{CC} = 4.5 \text{ V}$	-			6.4	-	pC		
$V_{CC} = 5.5 \text{ V}$	-			7.5	-	pC		

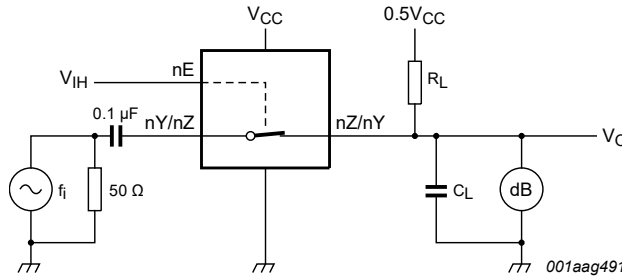
10.3. Test circuits



Test conditions:

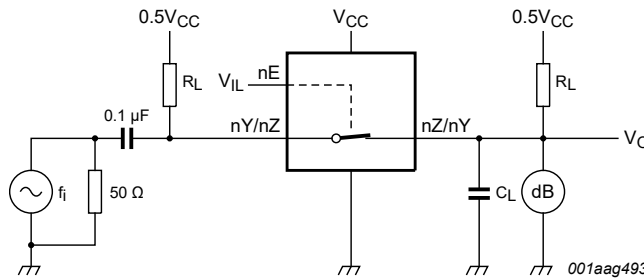
- $V_{CC} = 1.65\text{ V}; V_i = 1.4\text{ V (p-p)}$.
- $V_{CC} = 2.3\text{ V}; V_i = 2\text{ V (p-p)}$.
- $V_{CC} = 3\text{ V}; V_i = 2.5\text{ V (p-p)}$.
- $V_{CC} = 4.5\text{ V}; V_i = 4\text{ V (p-p)}$.

Fig. 18. Test circuit for measuring total harmonic distortion



Adjust f_i voltage to obtain 0 dBm level at output. Increase f_i frequency until dB meter reads -3 dB.

Fig. 19. Test circuit for measuring the frequency response when switch is in ON-state



Adjust f_i voltage to obtain 0 dBm level at input.

Fig. 20. Test circuit for measuring isolation (OFF-state)

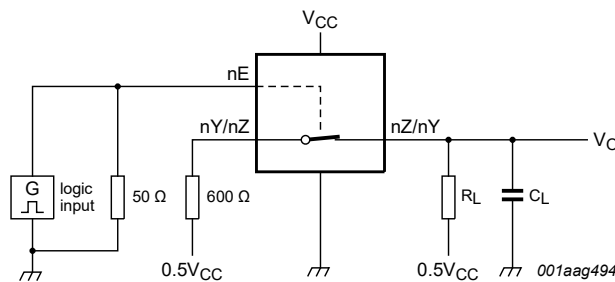
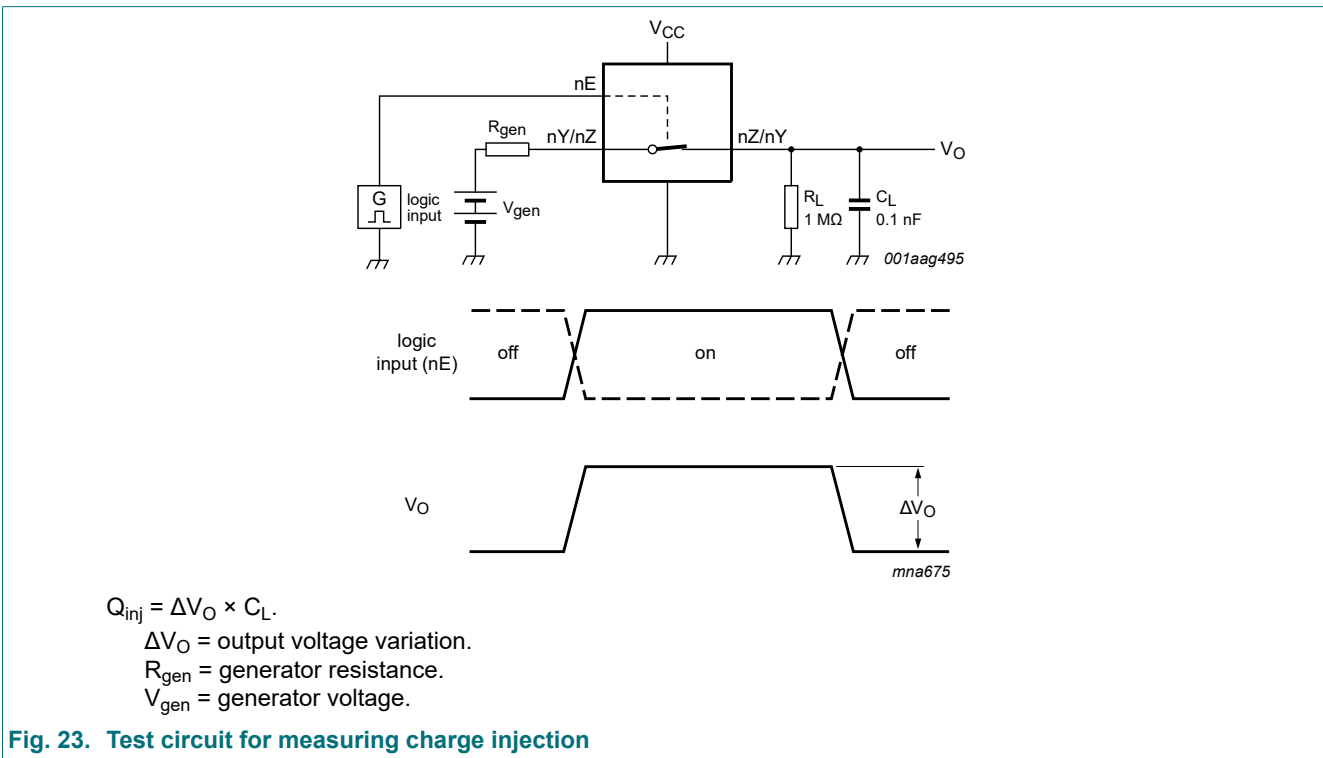
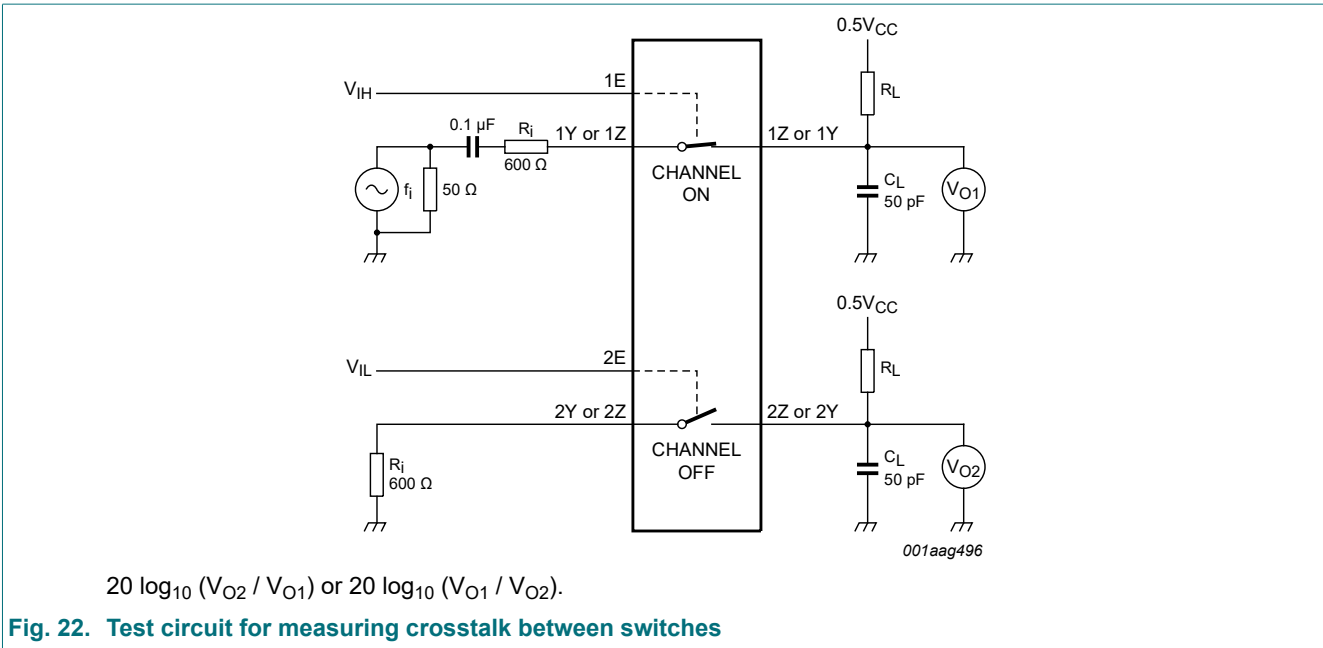


Fig. 21. Test circuit for measuring crosstalk voltage (between digital inputs and switch)



11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

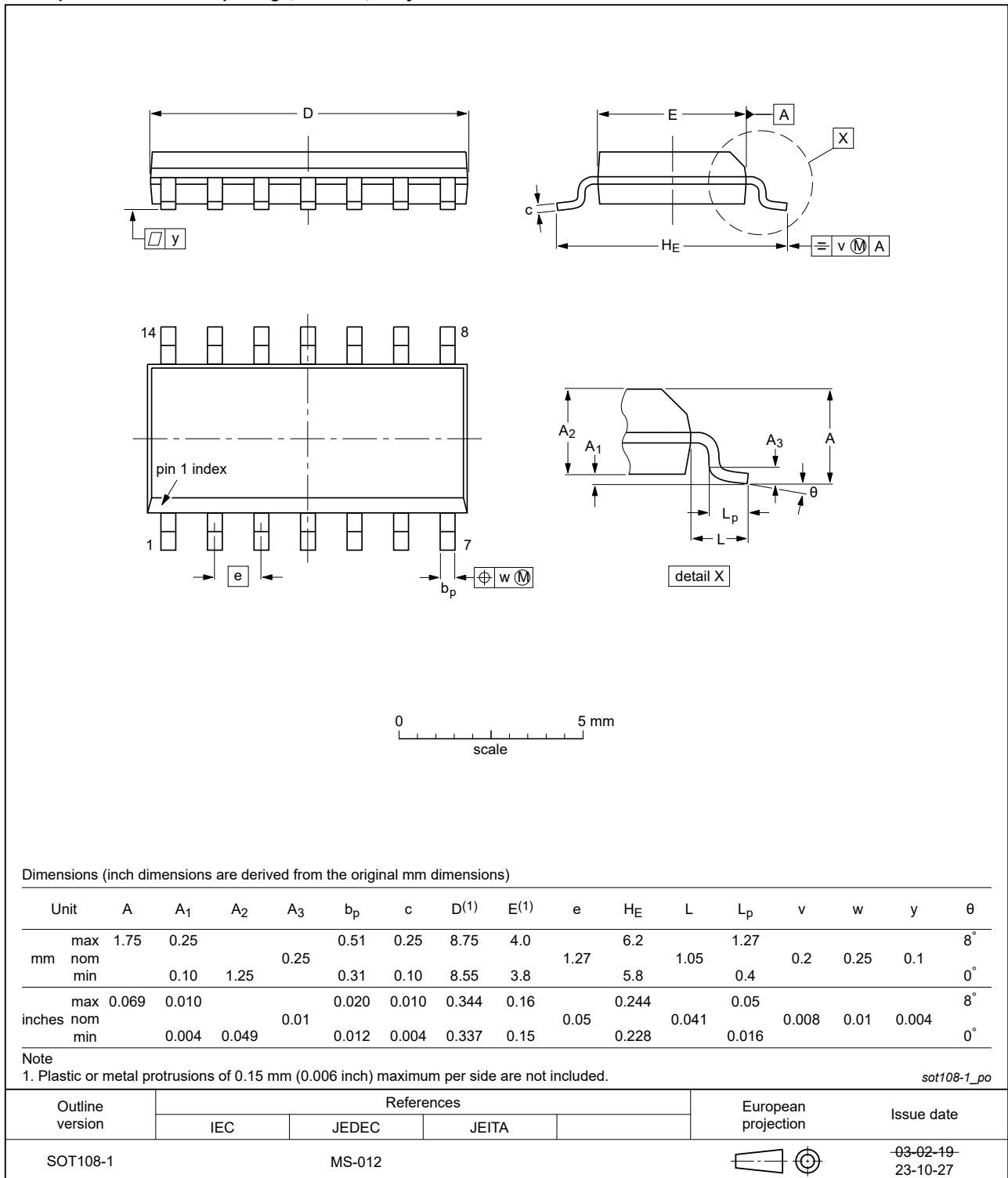


Fig. 24. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1



Fig. 25. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Fig. 26. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4066_Q100 v.4	20240222	Product data sheet	-	74LVC4066_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Fig. 24, Fig. 25: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. 			
74LVC4066_Q100 v.3	20230824	Product data sheet	-	74LVC4066_Q100 v.2
Modifications:	<ul style="list-style-type: none"> Section 2: ESD specification updated according to the latest JEDEC standard. 			
74LVC4066_Q100 v.2	20200326	Product data sheet	-	74LVC4066_Q100 v.1
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 2 updated. Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 26: Package outline drawing SOT762-1 (DHVQFN14) updated. 			
74LVC4066_Q100 v.1	20120807	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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