



PSMN015-100YL

N-channel 100 V, 15 mΩ logic level MOSFET in LPAK56

4 November 2016

Product data sheet

1. General description

Logic level N-channel MOSFET in an LPAK56 (Power SO8) package using TrenchMOS technology. This product is designed and qualified for use in a wide range of power supply & motor control equipment.

2. Features and benefits

- Advanced TrenchMOS provides low $R_{DS(on)}$ and low gate charge
- Logic level gate operation
- Avalanche rated, 100 % tested
- LPAK provides maximum power density in a Power SO8 package

3. Applications

- Synchronous rectification in power supply equipment
- Chargers & adaptors with $V_{out} < 10$ V
- Fast charge & USB-PD applications
- Battery powered motor control
- LED lighting & TV backlight

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	100	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	-	69	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	-	195	W
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 20\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11	-	12.1	15	mΩ
Dynamic characteristics						
Q_{GD}	gate-drain charge	$I_D = 20\text{ A}$; $V_{DS} = 80\text{ V}$; $V_{GS} = 5\text{ V}$; Fig. 13 ; Fig. 14	-	16	-	nC

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN015-100YL	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN015-100YL	15L100

8. Limiting values

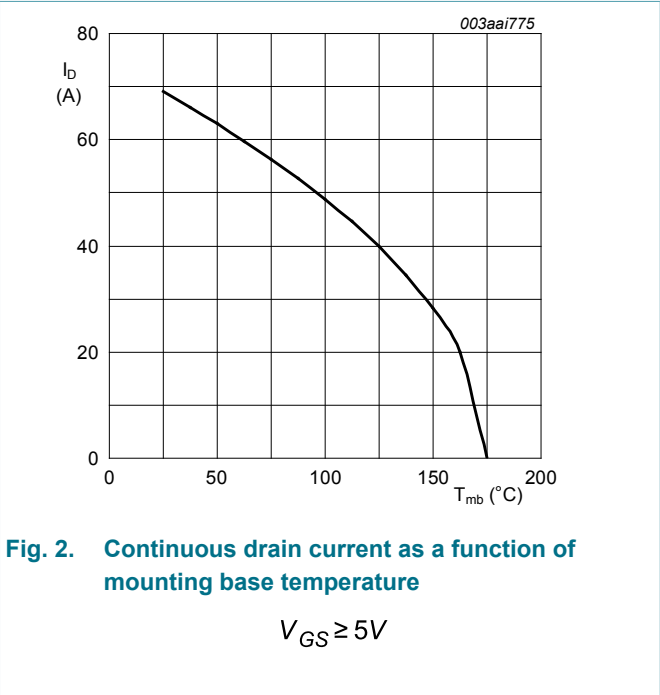
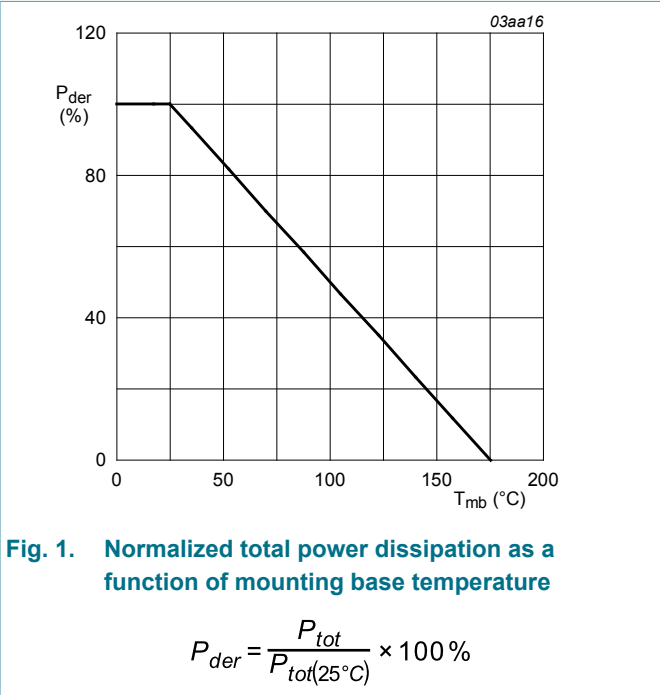
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	100	V
V_{GS}	gate-source voltage		-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1	-	195	W
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	-	69	A
		$V_{GS} = 5\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	-	49	A
I_{DM}	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; Fig. 3	-	274	A
T_{stg}	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	69	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	274	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 69 A; V _{sup} ≤ 100 V; R _{GS} = 50 Ω; V _{GS} = 5 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[1][2]	-	110	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.



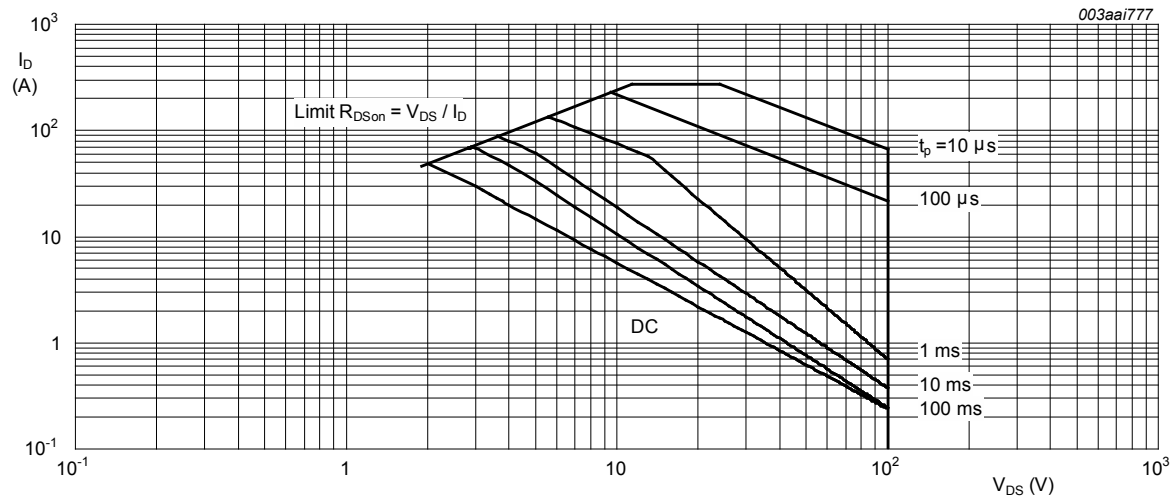


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

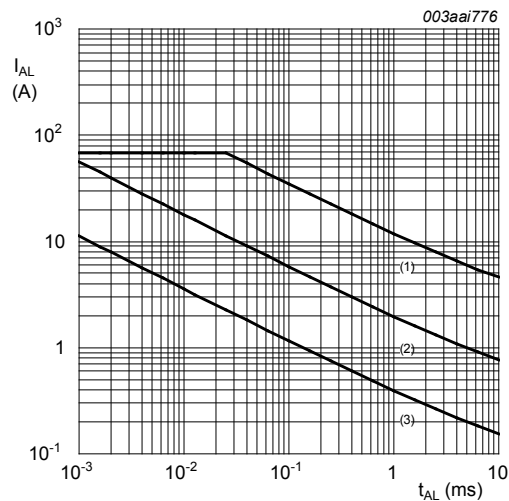


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j(init)} = 25^{\circ}C$; (2) $T_{j(init)} = 150^{\circ}C$; (3) Repetitive Avalanche

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	0.77	K/W

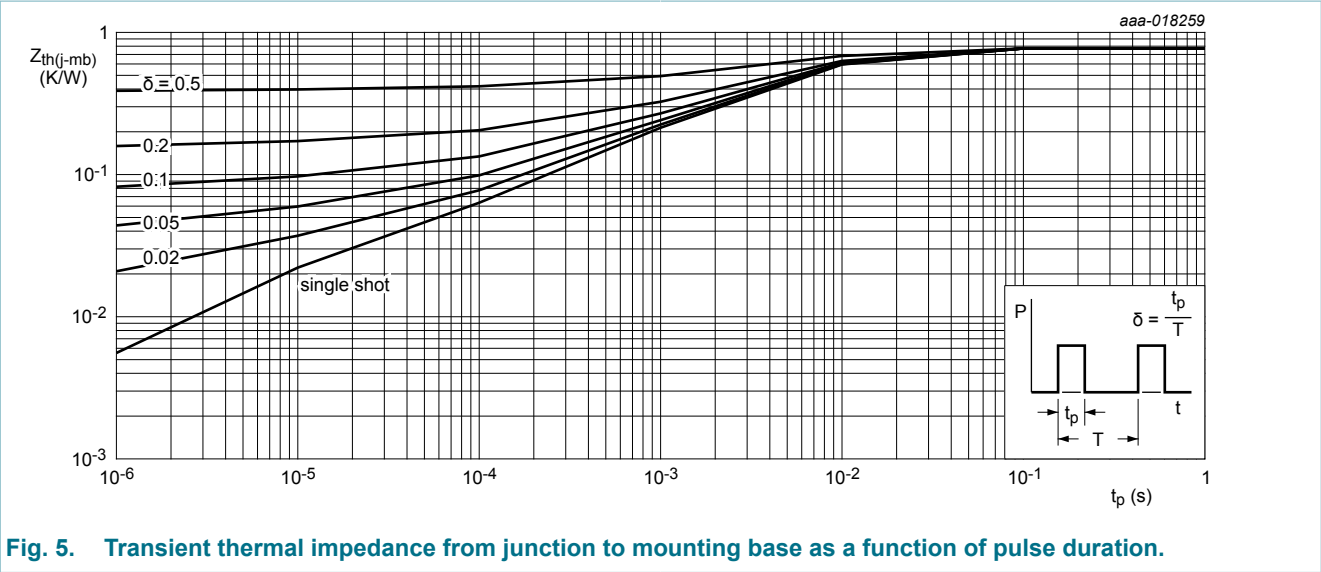


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration.

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C		100	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C		90	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 25 °C; Fig. 9 ; Fig. 10		1.4	1.7	2.1	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = -55 °C; Fig. 9		-	-	2.45	V
		I _D = 1 mA; V _{DS} =V _{GS} ; T _j = 175 °C; Fig. 9		0.5	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 100 V; V _{GS} = 0 V; T _j = 25 °C		-	0.11	10	μA
		V _{DS} = 100 V; V _{GS} = 0 V; T _j = 175 °C		-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C		-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 5 V; I _D = 20 A; T _j = 25 °C; Fig. 11		-	12.1	15	mΩ
		V _{GS} = 10 V; I _D = 20 A; T _j = 25 °C; Fig. 11		-	11.6	14.7	mΩ
		V _{GS} = 5 V; I _D = 20 A; T _j = 175 °C; Fig. 12 ; Fig. 11		-	-	41.4	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 20 A; V _{DS} = 80 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14		-	86.3	-	nC
		I _D = 20 A; V _{DS} = 80 V; V _{GS} = 5 V; Fig. 13 ; Fig. 14		-	45.8	-	nC
Q _{GS}	gate-source charge			-	11	-	nC

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Q _{GD}	gate-drain charge			-	16	-	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15		-	4604	6139	pF
C _{oss}	output capacitance			-	269	323	pF
C _{rss}	reverse transfer capacitance			-	156	213	pF
t _{d(on)}	turn-on delay time			-	21	-	ns
t _r	rise time	V _{DS} = 80 V; R _L = 4 Ω; V _{GS} = 5 V; R _{G(ext)} = 5 Ω		-	32	-	ns
t _{d(off)}	turn-off delay time			-	85	-	ns
t _f	fall time			-	59	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = 20 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16		-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 25 V		-	44	-	ns
Q _r	recovered charge			-	79	-	nC

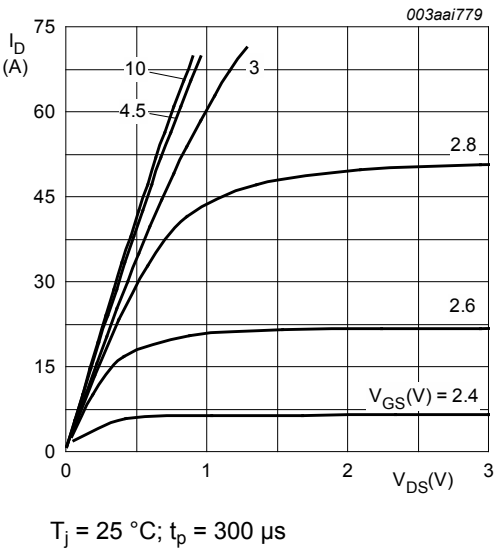


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

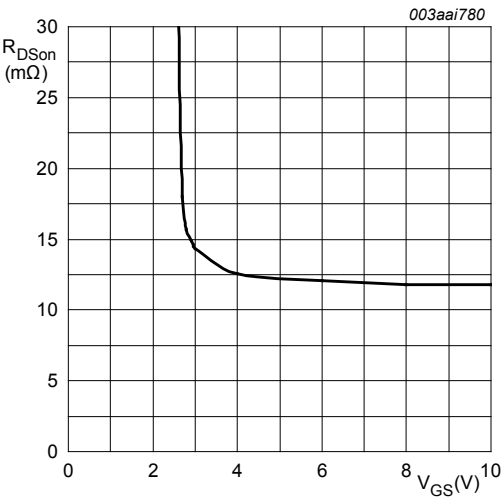


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

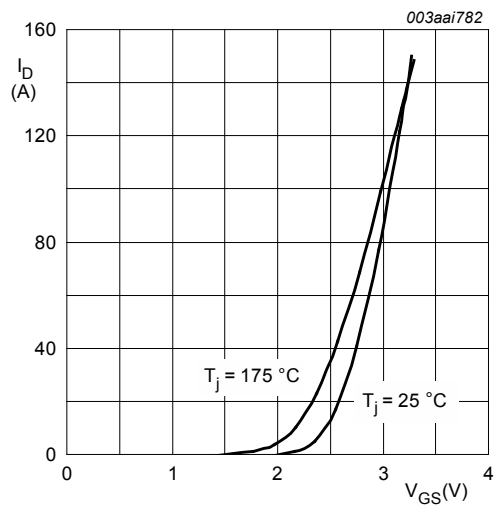


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10V$

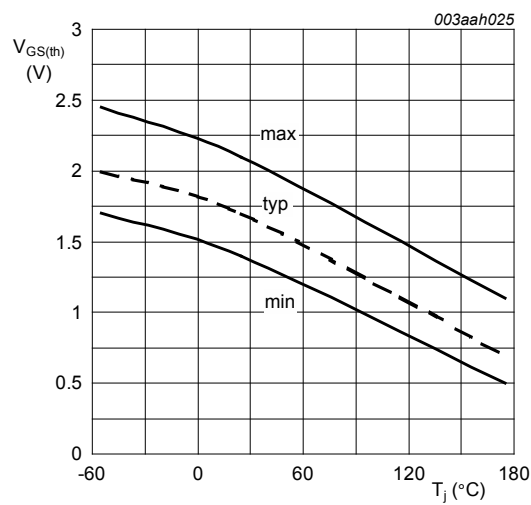


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

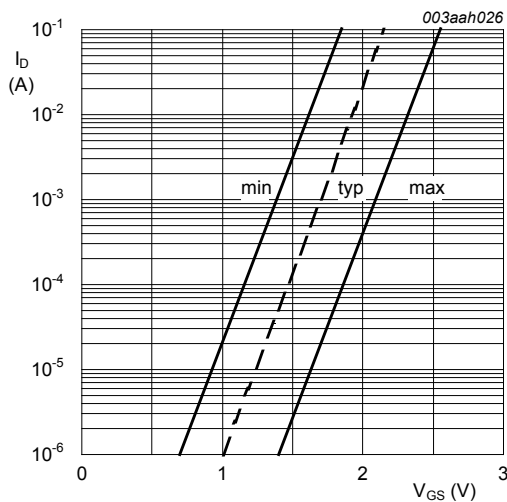


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_J = 25^\circ\text{C}; V_{DS} = 5V$

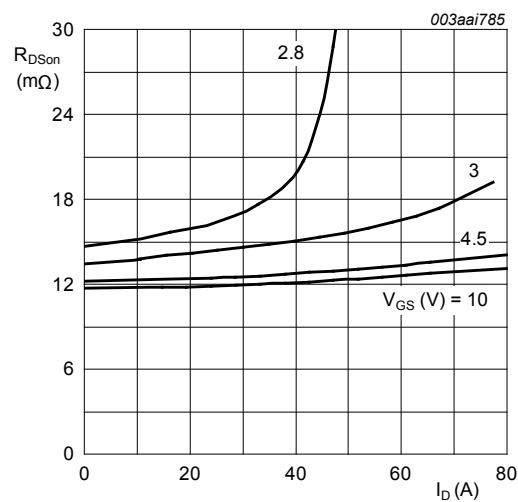


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

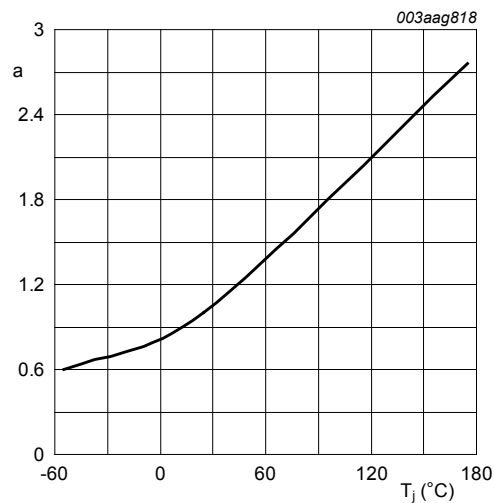


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25\text{ }^{\circ}\text{C})}$$

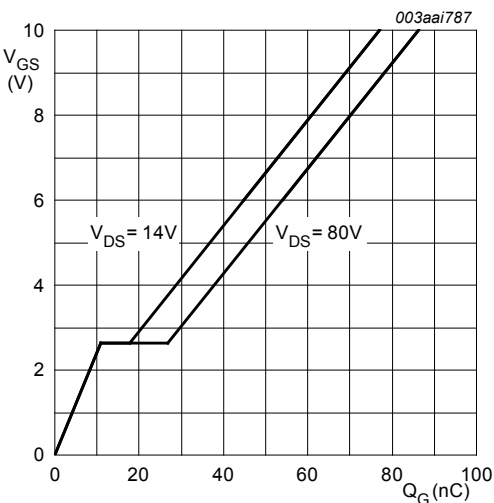


Fig. 14. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25\text{ }^{\circ}\text{C}; I_D = 20\text{ A}$$

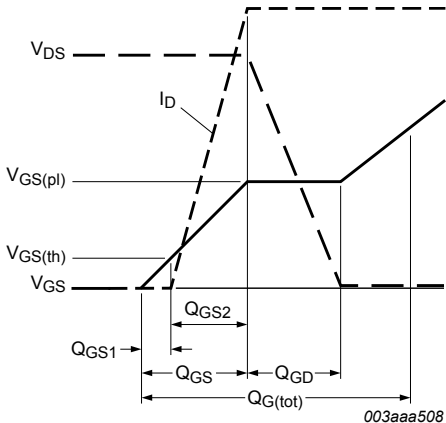


Fig. 13. Gate charge waveform definitions

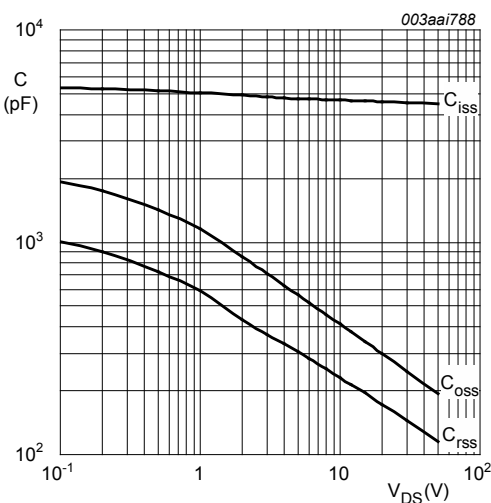


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$

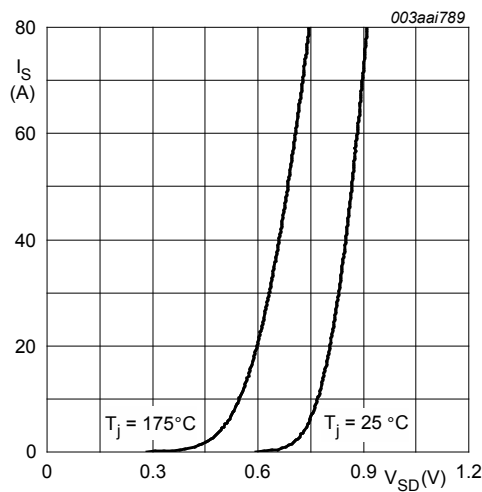


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$V_{GS} = 0V$

11. Package outline



Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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