74HC1G00; 74HCT1G00

2-input NAND gate

Rev. 8 — 20 June 2024 Product data sheet

1. General description

The 74HC1G00; 74HCT1G00 is a single 2-input NAND gate. Inputs include clamp diodes . This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- Input levels:
  - For 74HC1G00: CMOS level
  - For 74HCT1G00: TTL level
- Symmetrical output impedance
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD78 Class II Level B
- Balanced propagation delays
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC1G00GW 74HCT1G00GW	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm	SOT353-1
74HC1G00GV 74HCT1G00GV	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads	SOT753
74HC1G00GZ 74HCT1G00GZ	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm	SOT8065-1

4. Marking

Table 2. Marking codes

Type number	Marking [1]
74HC1G00GW	HA
74HCT1G00GW	TA
74HC1G00GV	H00
74HCT1G00GV	T00
74HC1G00GZ	HA
74HCT1G00GZ	TA

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

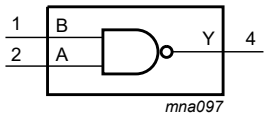


Fig. 1. Logic symbol

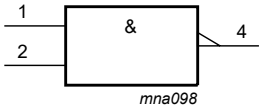


Fig. 2. IEC logic symbol

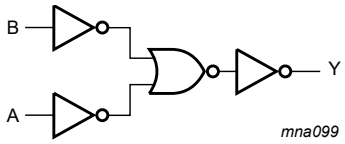
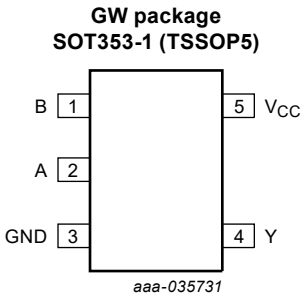
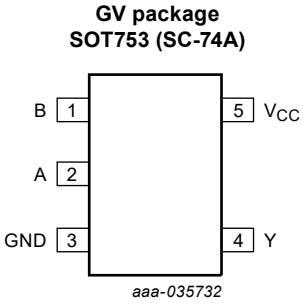


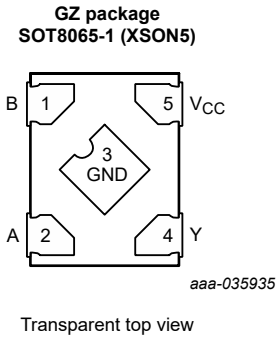
Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning







Transparent top view

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V_{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input		Output
A	**B**	**Y**
L	L	H
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	[1]	-	±12.5	mA
I_{CC}	supply current			-	25	mA
I_{GND}	ground current			-25	-	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	250	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.
For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.
For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G00			74HCT1G00			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	-	139	-	-	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at T_{amb} = 25 °C.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G00								
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	1.5	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	3.15	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	-	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	-	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	V
		I_O = -2.0 mA; V_{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
		I_O = -2.6 mA; V_{CC} = 6.0 V	5.63	5.81	-	5.2	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	V
		I_O = 2.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
		I_O = 2.6 mA; V_{CC} = 6.0 V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	1.0	-	1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	10	-	20	µA
C_I	input capacitance		-	1.5	-	-	-	pF
74HCT1G00								
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	V
		I_O = -2.0 mA; V_{CC} = 4.5 V	4.13	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}						
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	V
		I_O = 2.0 mA; V_{CC} = 4.5 V	-	0.15	0.33	-	0.4	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	1.0	-	1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	10	-	20	µA
ΔI_{CC}	additional supply current	per input; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	500	-	850	µA
C_I	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

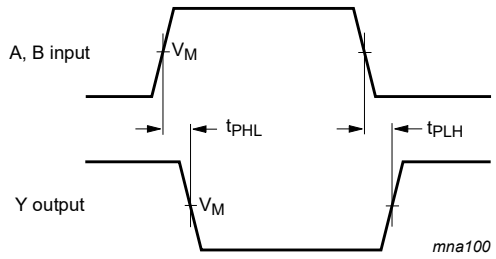
GND = 0 V; $t_r = t_f \leq 6.0$ ns; All typical values are measured at T_{amb} = 25 °C. For test circuit, see Fig. 5

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G00								
t_{pd}	propagation delay	A and B to Y; see Fig. 4 [1]						
		V_{CC} = 2.0 V; C_L = 50 pF	-	25	115	-	135	ns
		V_{CC} = 4.5 V; C_L = 50 pF	-	9	23	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	7	-	-	-	ns
		V_{CC} = 6.0 V; C_L = 50 pF	-	8	20	-	23	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} [2]	-	19	-	-	-	pF
74HCT1G00								
t_{pd}	propagation delay	A and B to Y; see Fig. 4 [1]						
		V_{CC} = 4.5 V; C_L = 50 pF	-	12	24	-	27	ns
		V_{CC} = 5.0 V; C_L = 15 pF	-	10	-	-	-	ns
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V [2]	-	21	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.

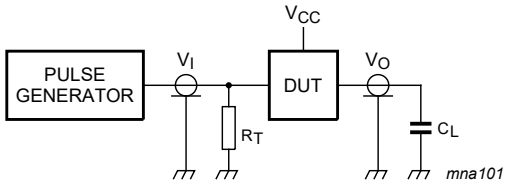
[2] C_{PD} is used to determine the dynamic power dissipation P_D (µW).
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; f_o = output frequency in MHz
C_L = output load capacitance in pF
V_{CC} = supply voltage in V
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

11.1. Waveforms and test circuit



For 74HC1G00:
$V_M = 0.5V_{CC}$; V_I = GND to V_{CC}
For 74HCT1G00:
V_M = 1.3 V; V_I = GND to 3.0 V

Fig. 4. Input to output propagation delays

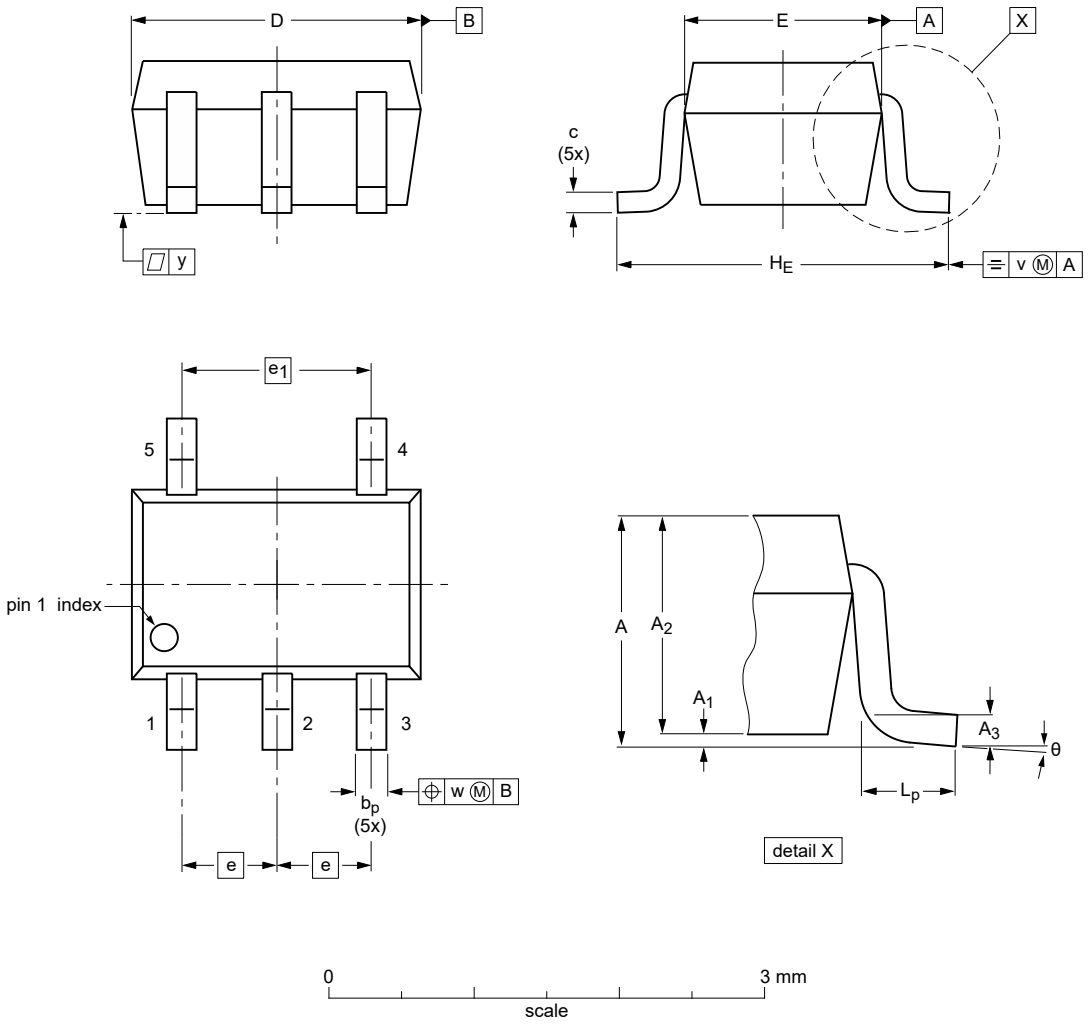


Test data is given in Table 8.
C_L = Load capacitance including jig and probe capacitance;
R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

12. Package outline

TSSOP5: plastic thin shrink small outline package; 5 leads; body width 1.25 mm **SOT353-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	e_1	H_E	L_p	v	w	y	θ
mm	max	1.1	0.1	1.0	0.15	0.30	0.25	2.2	1.35	0.65	1.3	2.4	0.46	0.3	0.1	0.1	8°
	min	0.8	0	0.8		0.15	0.08	1.8	1.15			1.8	0.26				0°

Note

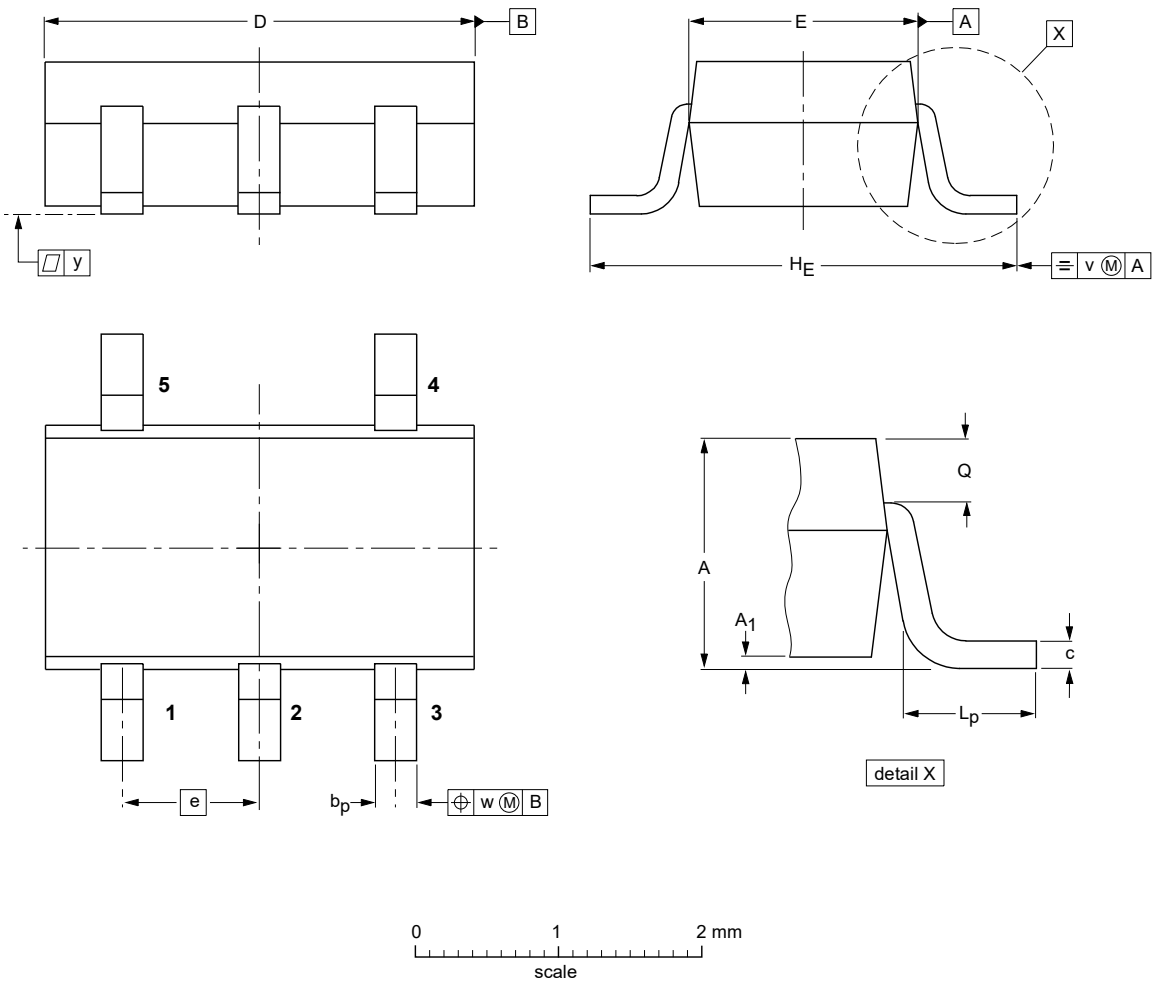
1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

sot353-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT353-1		MO-203	SC-88A		~~21-12-15~~ 21-12-16

Fig. 6. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads **SOT753**



DIMENSIONS (mm are the original dimensions)

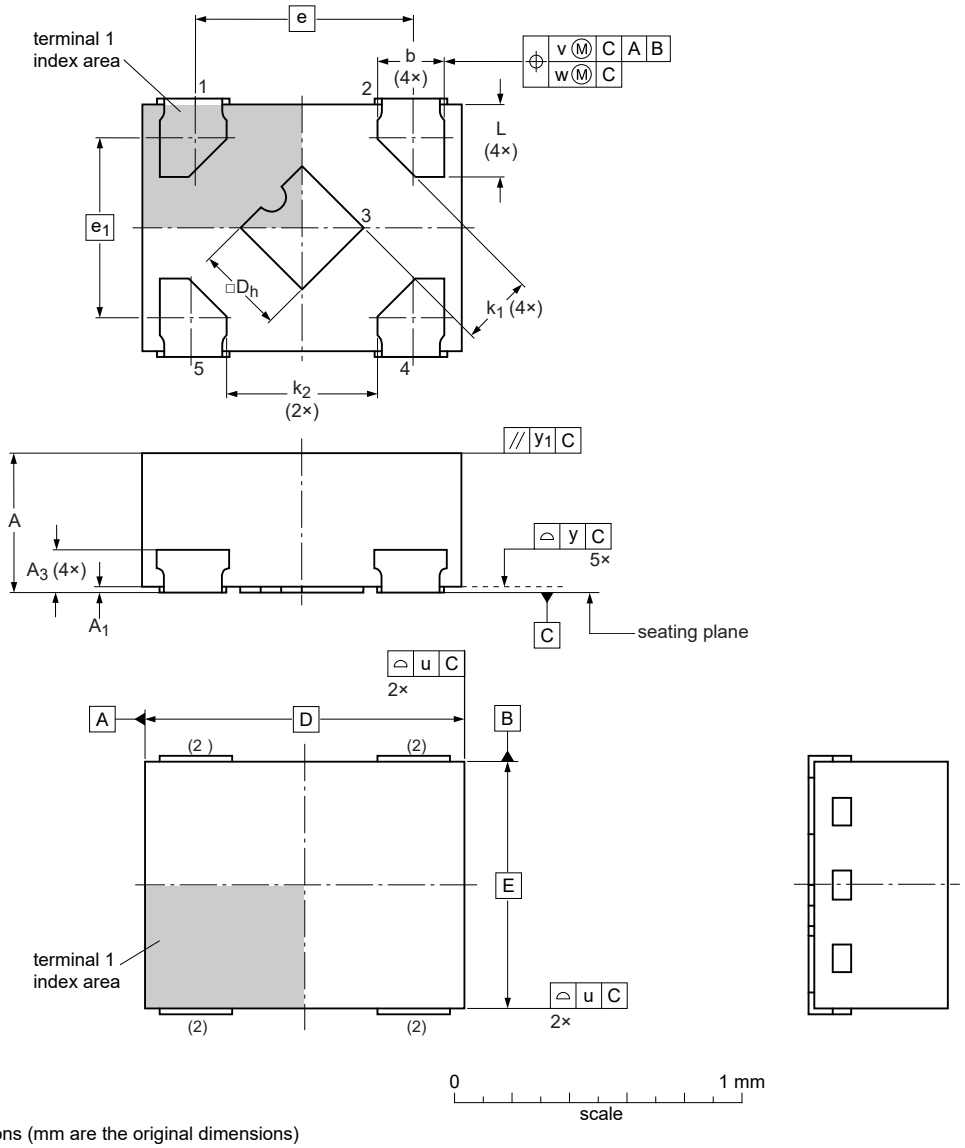
UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.100 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT753			SC-74A			~~02-04-16~~ 06-03-16

Fig. 7. Package outline SOT753 (SC-74A)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm

SOT8065-1



Dimensions (mm are the original dimensions)

Unit		A(1)	A1	A3	b	D(1)	Dh	E(1)	e	e1	k1	k2	L	u	v	w	y	y1
mm	max	0.50	0.040	0.135 (typ)	0.28	1.10	0.35	0.85	0.75	0.6		0.45	0.30	0.05	0.1	0.05	0.05	0.05
	nom	0.47	0.020		0.23		0.30				0.2		0.25					
	min	0.44	0.005		0.20		0.27						0.22					

Note:
1. Plastic or metal protrusions per side are not included.
2. Side wettable flanks (SWF), protrusion max. 0.02 mm.

sot8065-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8065-1		MO-340				~~24-07-09~~ 24-08-27

Fig. 8. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G00 v.8	20250314	Product data sheet	-	74HC_HCT1G00 v.7
Modifications:	• Type numbers 74HC1G00GZ and 74HCT1G00GZ (SOT8065-1/XSON5) added.			
74HC_HCT1G00 v.7	20240620	Product data sheet	-	74HC_HCT1G00 v.6
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard. • Table 5: P_{tot} total power dissipation corrected.			
74HC_HCT1G00 v.6	20220121	Product data sheet	-	74HC_HCT1G00 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Section 2 updated. • Table 5: Derating values for P_{tot} total power dissipation updated. • Fig. 6: Package outline drawing for SOT353-1 (TSSOP5) has been changed.			
74HC_HCT1G00 v.5	20130925	Product data sheet	-	74HC_HCT1G00 v.4
Modifications:	• Section 1 updated.			
74HC_HCT1G00 v.4	20070711	Product data sheet	-	74HC_HCT1G00 v.3
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package SOT353 changed to SOT353-1 in Table 1 and Fig. 6. • Quick reference data and Soldering sections removed. • Section 2 updated.			
74HC_HCT1G00 v.3	20020515	Product specification	-	74HC_HCT1G00 v.2
74HC_HCT1G00 v.2	20010302	Product specification	-	74HC_HCT1G00 v.1
74HC_HCT1G00 v.1	19980730	Preliminary specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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