

74LVC3G04-Q100

Triple inverter

Rev. 5 — 24 August 2023

Product data sheet

1. General description

The 74LVC3G04-Q100 is a triple inverter. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V environments.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

This device is fully specified for partial power down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the potentially damaging backflow current through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 1.65 V to 5.5 V
- 5 V tolerant outputs for interfacing with 5 V logic
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-7 (1.65 V to 1.95 V)
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ± 24 mA output drive ($V_{CC} = 3.0$ V)
- CMOS low power consumption
- Latch-up performance exceeds 250 mA
- Direct interface with TTL levels
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC3G04DP-Q100	-40 °C to +125 °C	TSSOP8	plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm	SOT505-2
74LVC3G04DC-Q100	-40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74LVC3G04DP-Q100	V04
74LVC3G04DC-Q100	V04

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

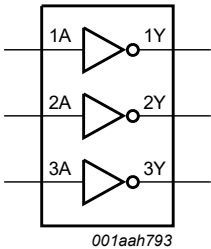


Fig. 1. Logic symbol

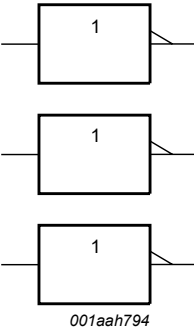


Fig. 2. IEC logic symbol

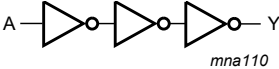


Fig. 3. Logic diagram (one driver)

6. Pinning information

6.1. Pinning

74LVC3G04

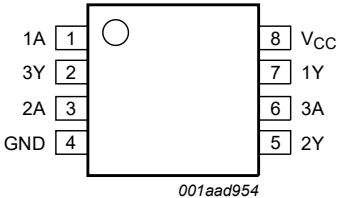


Fig. 4. Pin configuration SOT505-2 (TSSOP8) and SOT765-1 (VSSOP8)

6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
1A, 2A, 3A	1, 3, 6	data input
GND	4	ground (0 V)
1Y, 2Y, 3Y	7, 5, 2	data output
V _{CC}	8	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; L = LOW voltage level

Input nA	Output nY
L	H
H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
V _O	output voltage	Active mode [1]	-0.5	V _{CC} + 0.5	V
		Power-down mode; V _{CC} = 0 V [1]	-0.5	+6.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	250	mW
T _{stg}	storage temperature		-65	+150	°C

- [1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT505-2 (TSSOP8) package: P_{tot} derates linearly with 4.6 mW/K above 96 °C.
For SOT765-1 (VSSOP8) package: P_{tot} derates linearly with 4.9 mW/K above 99 °C.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		1.65	5.5	V
V _I	input voltage		0	5.5	V
V _O	output voltage	Active mode	0	V _{CC}	V
		Power-down mode; V _{CC} = 0 V	0	5.5	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 1.65 V to 2.7 V	-	20	ns/V
		V _{CC} = 2.7 V to 5.5 V	-	10	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
T_{amb} = -40 °C to +85 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	1.2	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.9	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	2.2	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.3	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.45	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.30	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.55	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	±0.1	±1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	±0.1	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	0.1	4	µA
ΔI _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	5	500	µA
C _I	input capacitance	V _{CC} = 3.3 V; V _I = GND to V _{CC}	-	2.5	-	pF
T_{amb} = -40 °C to +125 °C						
V _{IH}	HIGH-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}	-	-	V
		V _{CC} = 2.3 V to 2.7 V	1.7	-	-	V
		V _{CC} = 2.7 V to 3.6 V	2.0	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.65 V to 1.95 V	-	-	0.35 × V _{CC}	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V _{CC} = 2.7 V to 3.6 V	-	-	0.8	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3 × V _{CC}	V

Symbol	Parameter	Conditions	Min	Typ[1]	Max	Unit
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 µA; V _{CC} = 1.65 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -4 mA; V _{CC} = 1.65 V	0.95	-	-	V
		I _O = -8 mA; V _{CC} = 2.3 V	1.7	-	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	1.9	-	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	2.0	-	-	V
		I _O = -32 mA; V _{CC} = 4.5 V	3.4	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 µA; V _{CC} = 1.65 V to 5.5 V	-	-	0.10	V
		I _O = 4 mA; V _{CC} = 1.65 V	-	-	0.70	V
		I _O = 8 mA; V _{CC} = 2.3 V	-	-	0.45	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	-	0.60	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	-	0.80	V
		I _O = 32 mA; V _{CC} = 4.5 V	-	-	0.80	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	±1	µA
I _{OFF}	power-off leakage current	V _{CC} = 0 V; V _I or V _O = 5.5 V	-	-	±2	µA
I _{CC}	supply current	V _I = 5.5 V or GND; V _{CC} = 1.65 V to 5.5 V; I _O = 0 A	-	-	4	µA
ΔI _{CC}	additional supply current	per pin; V _{CC} = 2.3 V to 5.5 V; V _I = V _{CC} - 0.6 V; I _O = 0 A	-	-	500	µA

[1] All typical values are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.

11. Dynamic characteristics

Table 8. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 6.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nA to nY; see Fig. 5 [2]						
		V _{CC} = 1.65 V to 1.95 V	1.0	3.5	8.0	1.0	9.5	ns
		V _{CC} = 2.3 V to 2.7 V	0.5	2.2	4.4	0.5	5.4	ns
		V _{CC} = 2.7 V	0.5	2.7	5.2	0.5	7.0	ns
		V _{CC} = 3.0 V to 3.6 V	0.5	2.7	4.1	0.5	5.5	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	1.9	3.2	0.5	3.8	ns
C _{PD}	power dissipation capacitance	V _I = GND to V _{CC} ; V _{CC} = 3.3 V [3]	-	13.5	-	-	-	pF

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 1.8 V, 2.5 V, 2.7 V, 3.3 V and 5.0 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

Σ(C_L × V_{CC}² × f_o) = sum of outputs.

11.1. Waveform and test circuit

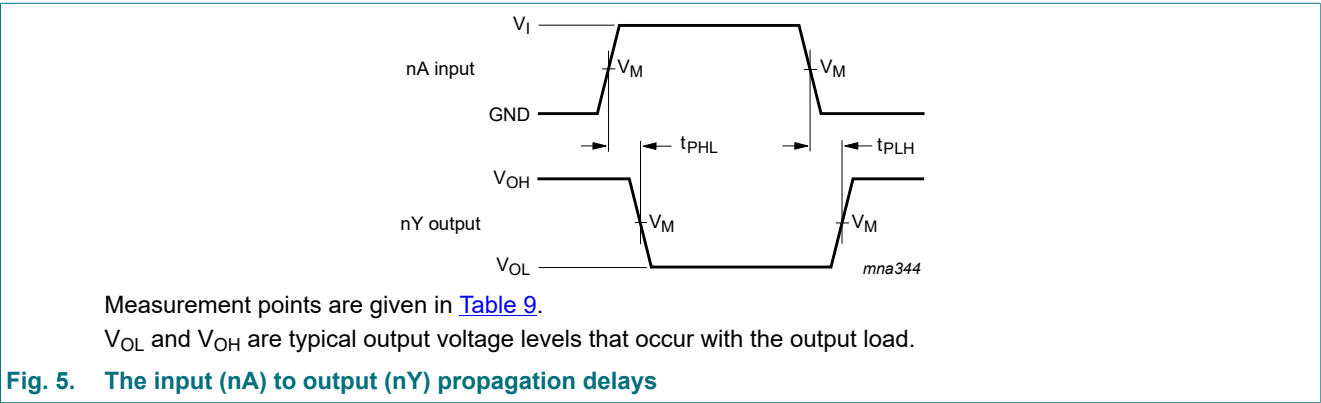


Table 9. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
1.65 V to 1.95 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.3 V to 2.7 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$
2.7 V	1.5 V	1.5 V
3.0 V to 3.6 V	1.5 V	1.5 V
4.5 V to 5.5 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$

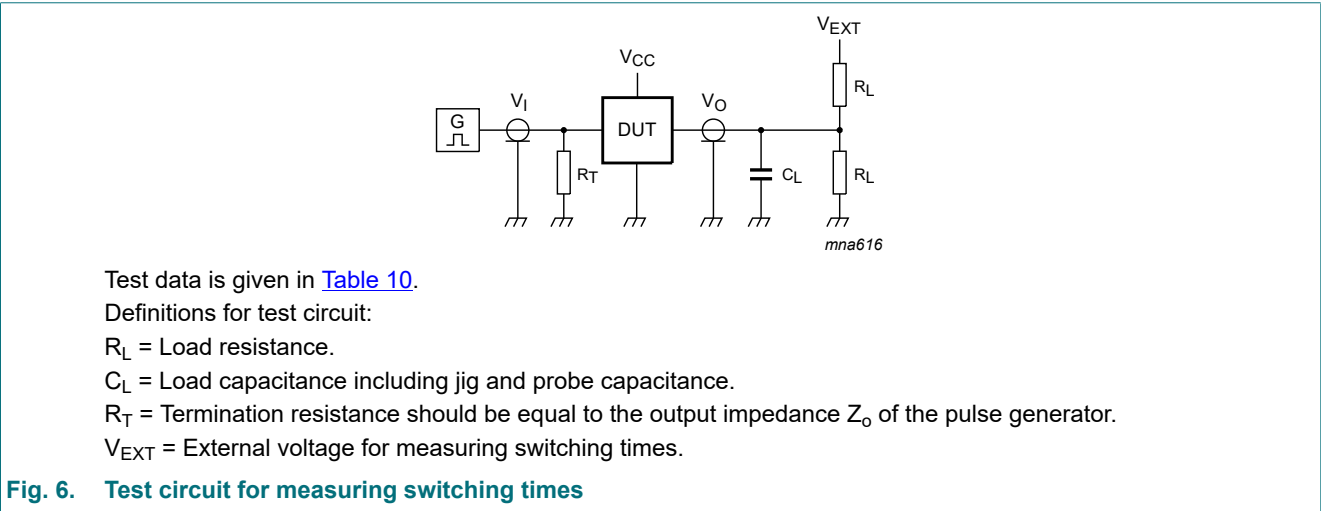


Table 10. Test data

Supply voltage	Input		Load		V_{EXT}
V_{CC}	V_I	$t_r = t_f$	C_L	R_L	t_{PLH}, t_{PHL}
1.65 V to 1.95 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	1 k Ω	open
2.3 V to 2.7 V	V_{CC}	$\leq 2.0 \text{ ns}$	30 pF	500 Ω	open
2.7 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open
3.0 V to 3.6 V	2.7 V	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open
4.5 V to 5.5 V	V_{CC}	$\leq 2.5 \text{ ns}$	50 pF	500 Ω	open

12. Package outline

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 3 mm; lead length 0.5 mm SOT505-2

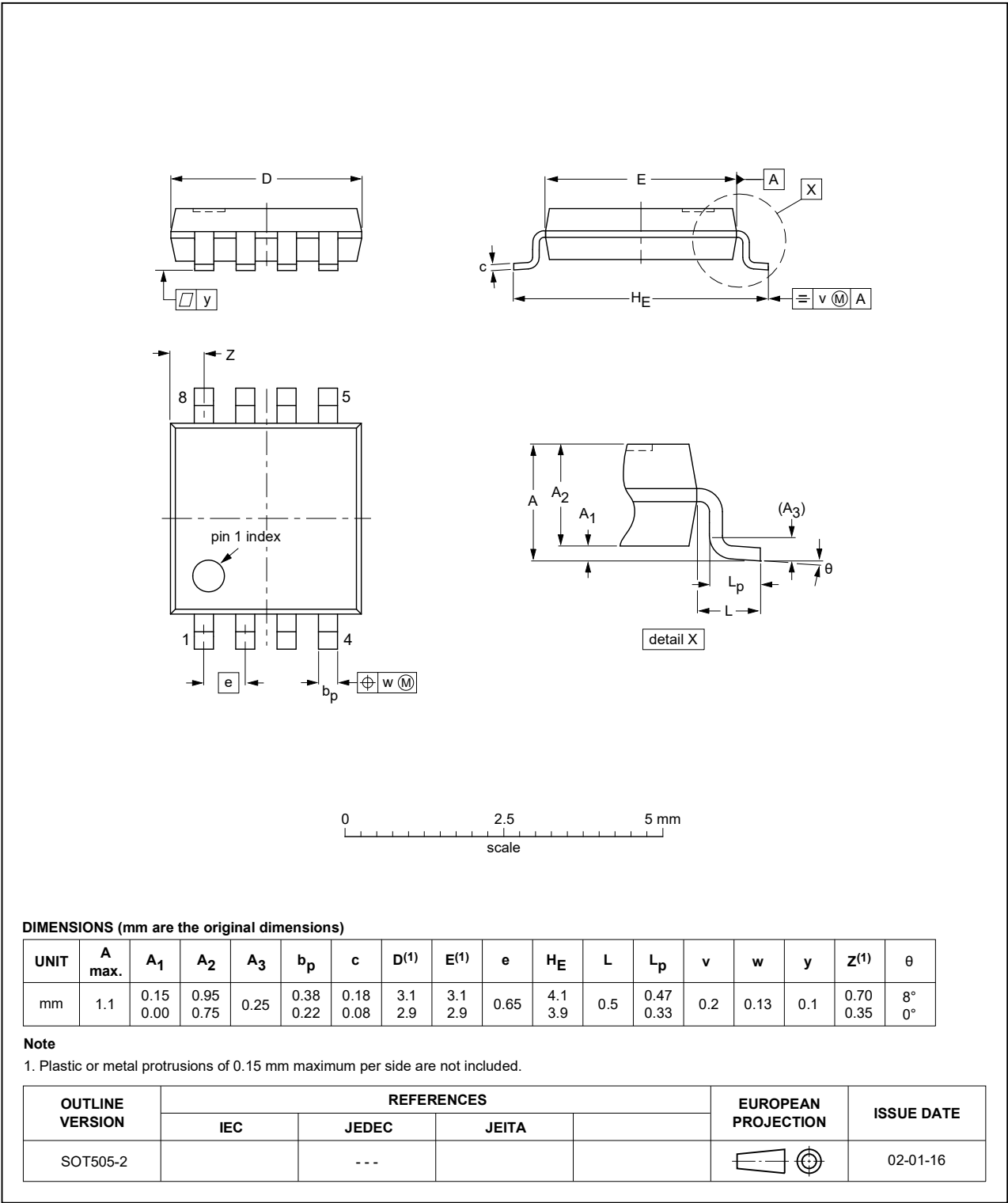


Fig. 7. Package outline SOT505-2 (TSSOP8)

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm

SOT765-1

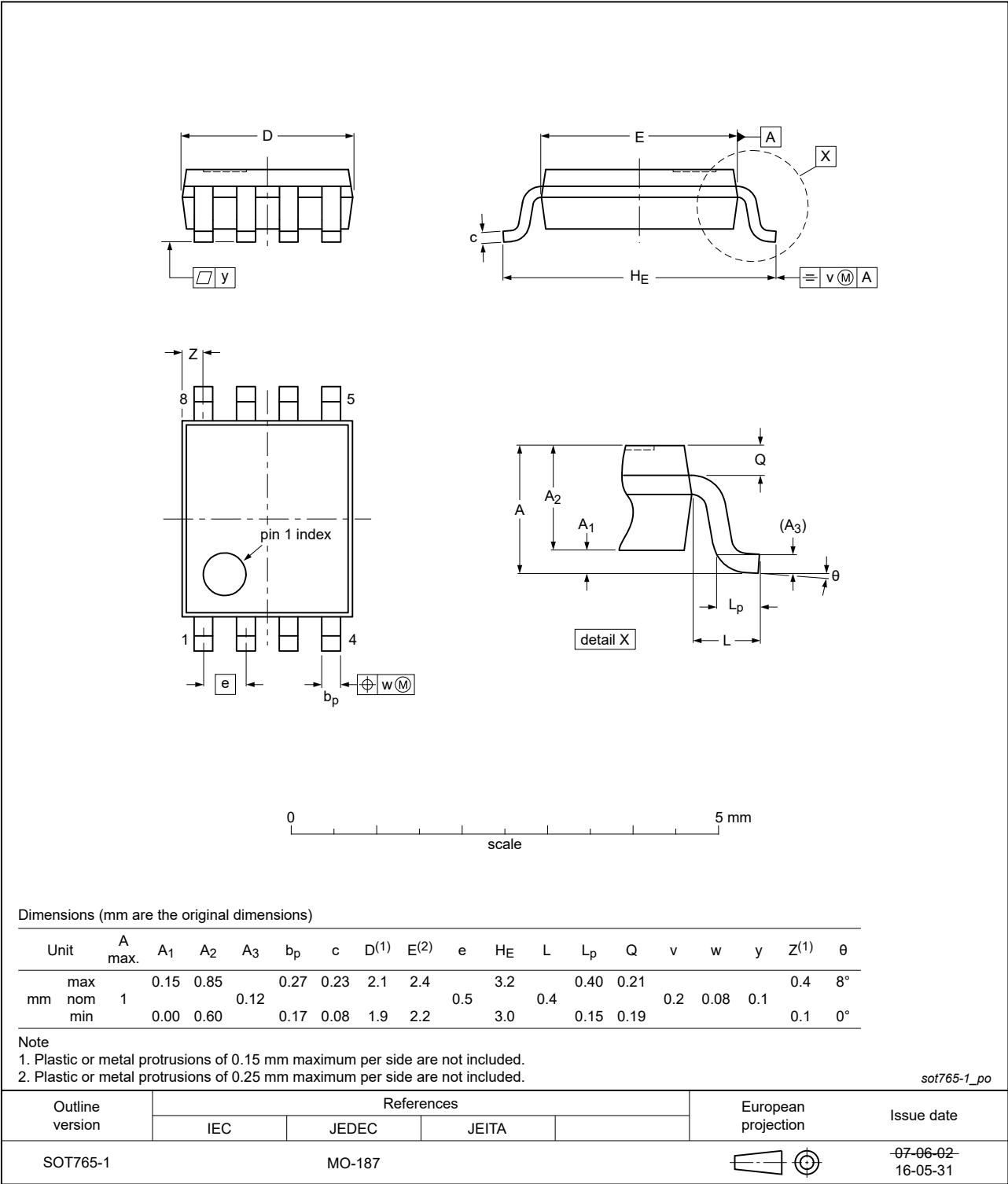


Fig. 8. Package outline SOT765-1 (VSSOP8)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC3G04_Q100 v.5	20230824	Product data sheet	-	74LVC3G04_Q100 v.4
Modifications:	<ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard.			
74LVC3G04_Q100 v.4	20210416	Product data sheet	-	74LVC3G04_Q100 v.3
Modifications:	<ul style="list-style-type: none">Section 1 updated.Section 8: Derating values for P_{tot} total power dissipation updated.			
74LVC3G04_Q100 v.3	20181102	Product data sheet	-	74LVC3G04_Q100 v.2
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.			
74LVC3G04_Q100 v.2	20161214	Product data sheet	-	74LVC3G04_Q100 v.1
Modifications:	<ul style="list-style-type: none">Table 7: The maximum limits for leakage current and supply current have changed.			
74LVC3G04_Q100 v.1	20130514	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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