74HC193; 74HCT193

Presettable synchronous 4-bit binary up/down counter

Rev. 8 — 14 March 2024 Product data sheet

1. General description

The 74HC193; 74HCT193 is a 4-bit synchronous binary up/down counter. Separate up/down clocks, CPU and CPD respectively, simplify operation. The outputs change state synchronously with the LOW-to-HIGH transition of either clock input. If the CPU clock is pulsed while CPD is held HIGH, the device will count up. If the CPD clock is pulsed while CPU is held HIGH, the device will count down. Only one clock input can be held HIGH at any time to guarantee predictable behavior. The device can be cleared at any time by the asynchronous master reset input (MR); it may also be loaded in parallel by activating the asynchronous parallel load input ($\overline{PL}$). The terminal count up ($\overline{TCU}$) and terminal count down ($\overline{TCD}$) outputs are normally HIGH. When the circuit has reached the maximum count state of 15, the next HIGH-to-LOW transition of CPU will cause $\overline{TCU}$ to go LOW. $\overline{TCU}$ will stay LOW until CPU goes HIGH again, duplicating the count up clock. Likewise, the $\overline{TCD}$ output will go LOW when the circuit is in the zero state and the CPD goes LOW. The terminal count outputs can be used as the clock input signals to the next higher order circuit in a multistage counter, since they duplicate the clock waveforms. Multistage counters will not be fully synchronous, since there is a slight delay time difference added for each stage that is added. The counter may be preset by the asynchronous parallel load capability of the circuit. Information present on the parallel data inputs (D0 to D3) is loaded into the counter and appears on the outputs (Q0 to Q3) regardless of the conditions of the clock inputs when the parallel load ($\overline{PL}$) input is LOW. A HIGH level on the master reset (MR) input will disable the parallel load gates, override both clock inputs and set all outputs (Q0 to Q3) LOW. If one of the clock inputs is LOW during and after a reset or load operation, the next LOW-to-HIGH transition of that clock will be interpreted as a legitimate signal and will be counted. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Input levels:
  - For 74HC193: CMOS level
  - For 74HCT193: TTL level
- Synchronous reversible 4-bit binary counting
- Asynchronous parallel load
- Asynchronous reset
- Expandable without external logic
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C.

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC193D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HCT193D				
74HC193PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74HCT193PW				

4. Functional diagram

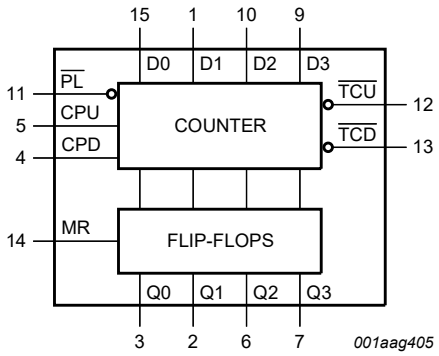


Fig. 1. Functional diagram

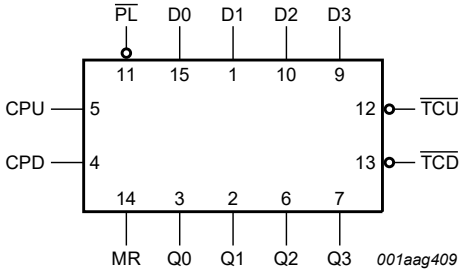


Fig. 2. Logic symbol

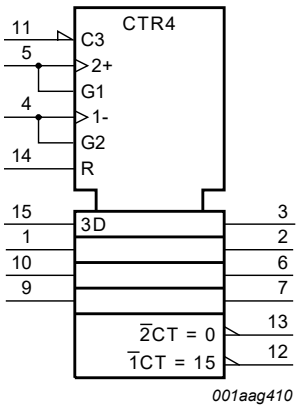


Fig. 3. IEC logic symbol

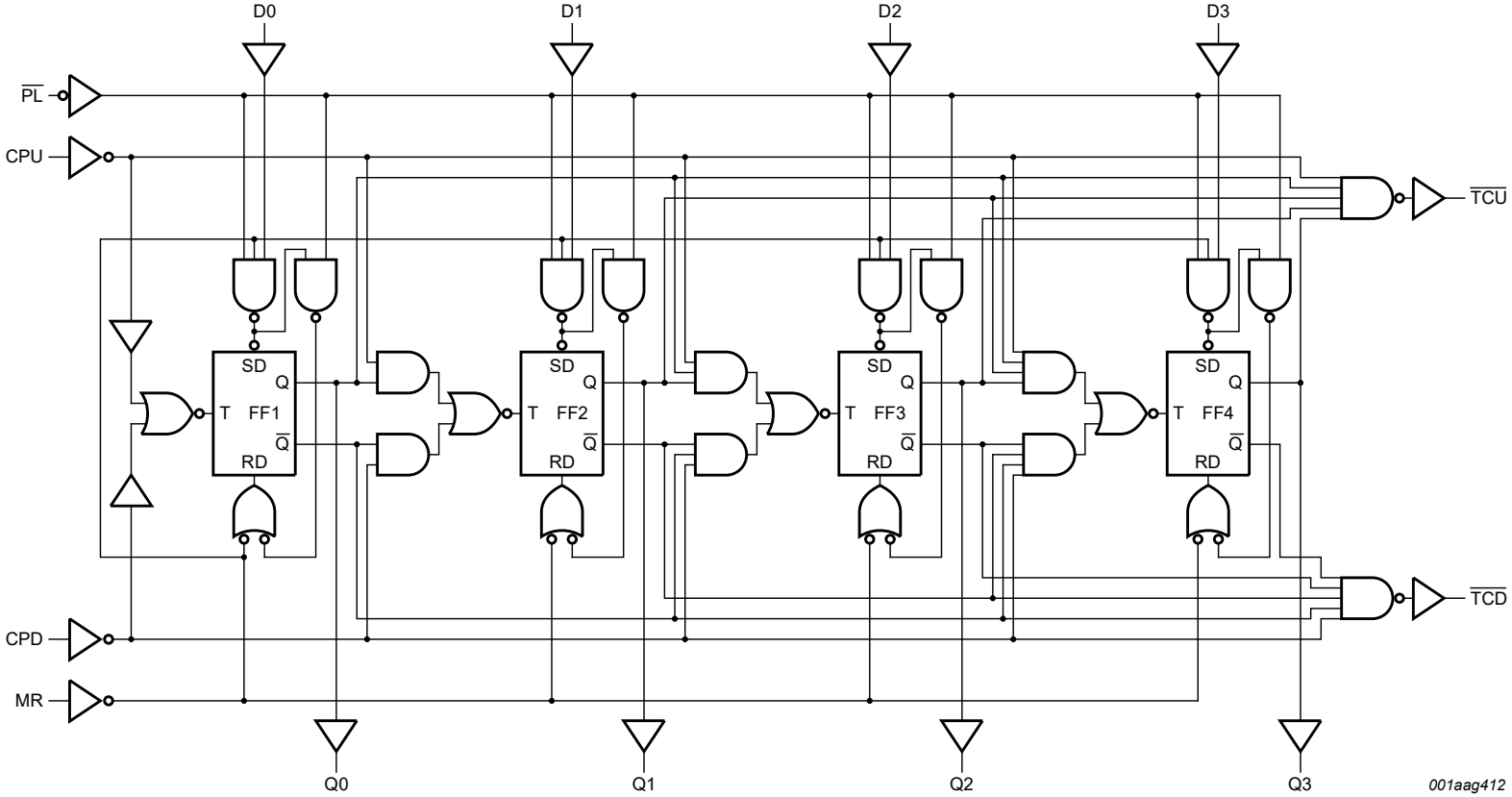


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning

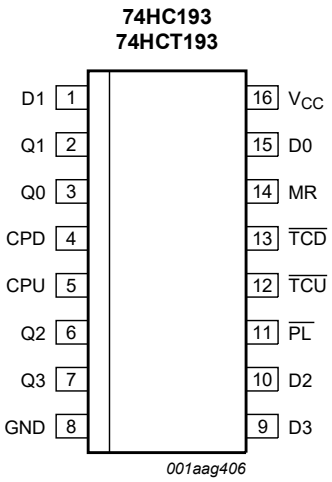


Fig. 5. Pin configuration for SOT109-1 (SO16)

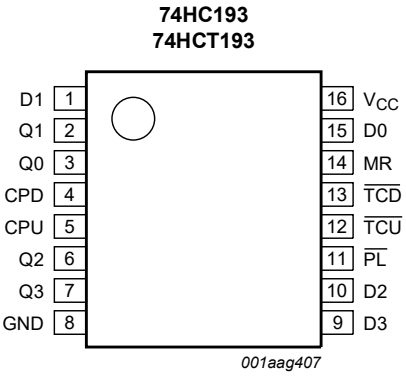


Fig. 6. Pin configuration for SOT403-1 (TSSOP16)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
D0, D1, D2, D3	15, 1, 10, 9	data input
Q0, Q1, Q2, Q3	3, 2, 6, 7	flip-flop output
CPD	4	count down clock input; LOW-to-HIGH, edge triggered
CPU	5	count up clock input; LOW-to-HIGH, edge triggered
GND	8	ground (0 V)
$\overline{PL}$	11	asynchronous parallel load input (active LOW)
$\overline{TCU}$	12	terminal count up (carry) output (active LOW)
$\overline{TCD}$	13	terminal count down (borrow) output (active LOW)
MR	14	asynchronous master reset input (active HIGH)
V_{CC}	16	supply voltage

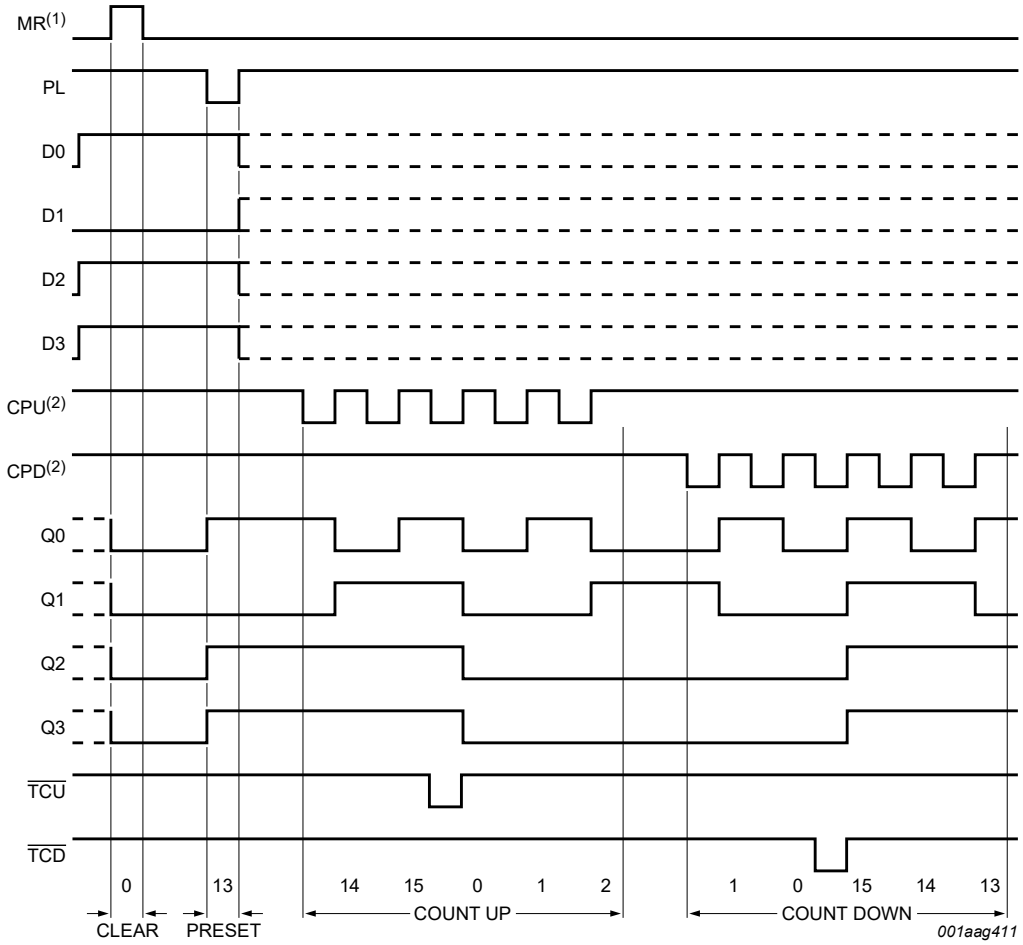
6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = LOW-to-HIGH clock transition.

Operating mode	Inputs								Outputs					
	MR	$\overline{PL}$	CPU	CPD	D0	D1	D2	D3	Q0	Q1	Q2	Q3	$\overline{TCU}$	$\overline{TCD}$
Reset (clear)	H	X	X	L	X	X	X	X	L	L	L	L	H	L
	H	X	X	H	X	X	X	X	L	L	L	L	H	H
Parallel load	L	L	X	L	L	L	L	L	L	L	L	L	H	L
	L	L	X	H	L	L	L	L	L	L	L	L	H	H
	L	L	L	X	H	H	H	H	H	H	H	H	L	H
	L	L	H	X	H	H	H	H	H	H	H	H	H	H
Count up	L	H	↑	H	X	X	X	X	count up				H [1]	H
Count down	L	H	H	↑	X	X	X	X	count down				H	H [2]

[1] $\overline{TCU}$ = CPU at terminal count up (HHHH)
[2] $\overline{TCD}$ = CPD at terminal count down (LLLL).



(1) Clear overrides load, data and count inputs.

(2) When counting up, the count down clock input (CPD) must be HIGH, when counting down the count up clock input (CPU) must be HIGH.

Sequence:

Clear (reset outputs to zero);

Load (preset) to binary thirteen;

Count up to fourteen, fifteen, terminal count up, zero, one and two;

Count down to one, zero, terminal count down, fifteen, fourteen and thirteen.

Fig. 7. Typical clear, load and count sequence

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	$V_O = -0.5$ V to $V_{CC} + 0.5$ V		-	±25	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			-	-50	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation		[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC193			74HCT193			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics type 74HC193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}	-	-	-	
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	2.0	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	4.5	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	6.0	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	0	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	0	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	0.16	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 6.0 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	µA
C_i	input capacitance		-	3.5	-	pF

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.84	-	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.34	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.33	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.33	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	80	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = -20 µA; V_{CC} = 2.0 V	1.9	-	-	V
		I_O = -20 µA; V_{CC} = 4.5 V	4.4	-	-	V
		I_O = -20 µA; V_{CC} = 6.0 V	5.9	-	-	V
		I_O = -4.0 mA; V_{CC} = 4.5 V	3.7	-	-	V
		I_O = -5.2 mA; V_{CC} = 6.0 V	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 2.0 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 4.5 V	-	-	0.1	V
		I_O = 20 µA; V_{CC} = 6.0 V	-	-	0.1	V
		I_O = 4.0 mA; V_{CC} = 4.5 V	-	-	0.4	V
		I_O = 5.2 mA; V_{CC} = 6.0 V	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	160	µA

Table 7. Static characteristics type 74HCT193

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = -20 µA	4.4	4.5	-	V
		I_O = -4.0 mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	0	0.1	V
		I_O = 4.0 mA	-	0.15	0.26	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±0.1	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pin Dn	-	35	126	µA
		pins CPU, CPD	-	140	504	µA
		pin $\overline{PL}$	-	65	234	µA
		pin MR	-	105	378	µA
C_i	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = -20 µA	4.4	-	-	V
		I_O = -4.0 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.33	V
I_I	input leakage current	V_I = V_{CC} or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	V_I = V_{CC} or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_I = V_{CC} - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pin Dn	-	-	157.5	µA
		pins CPU, CPD	-	-	630	µA
		pin $\overline{PL}$	-	-	292.5	µA
		pin MR	-	-	472.5	µA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = -20 µA	4.4	-	-	V
		I_O = -4.0 mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}; V_{CC} = 4.5 V				
		I_O = 20 µA	-	-	0.1	V
		I_O = 4.0 mA	-	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	160	µA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC}$ - 2.1 V; other inputs at V_{CC} or GND; I_O = 0 A; V_{CC} = 4.5 V to 5.5 V				
		pin Dn	-	-	171.5	µA
		pins CPU, CPD	-	-	686	µA
		pin $\overline{PL}$	-	-	318.5	µA
		pin MR	-	-	514.5	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics type 74HC193

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CPU, CPD to Qn; see Fig. 8 [1]	-							
		V_{CC} = 2.0 V	-	63	215	-	270	-	325	ns
		V_{CC} = 4.5 V	-	23	43	-	54	-	65	ns
		V_{CC} = 6.0 V	-	18	37	-	46	-	55	ns
		CPU to $\overline{TCU}$; see Fig. 9								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		CPD to $\overline{TCD}$; see Fig. 9								
		V_{CC} = 2.0 V	-	39	125	-	155	-	190	ns
		V_{CC} = 4.5 V	-	14	25	-	31	-	38	ns
		V_{CC} = 6.0 V	-	11	21	-	26	-	32	ns
		$\overline{PL}$ to Qn; see Fig. 10								
		V_{CC} = 2.0 V	-	69	220	-	275	-	330	ns
		V_{CC} = 4.5 V	-	25	44	-	55	-	66	ns
		V_{CC} = 6.0 V	-	20	37	-	47	-	56	ns
		MR to Qn; see Fig. 11								
		V_{CC} = 2.0 V	-	58	200	-	250	-	300	ns
		V_{CC} = 4.5 V	-	21	40	-	50	-	60	ns
		V_{CC} = 6.0 V	-	17	34		43	-	51	ns
		Dn to Qn; see Fig. 10								
		V_{CC} = 2.0 V	-	69	210	-	265	-	315	ns
		V_{CC} = 4.5 V	-	25	42	-	53	-	63	ns
		V_{CC} = 6.0 V	-	20	36	-	45	-	54	ns
		$\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns
		MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 2.0 V	-	74	285	-	355	-	430	ns
		V_{CC} = 4.5 V	-	27	57	-	71	-	86	ns
		V_{CC} = 6.0 V	-	22	48	-	60	-	73	ns
		Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 2.0 V	-	80	290	-	365	-	435	ns
		V_{CC} = 4.5 V	-	29	58	-	73	-	87	ns
		V_{CC} = 6.0 V	-	23	49	-	62	-	74	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{THL}	HIGH to LOW output transition time	see Fig. 11								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_{TLH}	LOW to HIGH output transition time	see Fig. 11								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
t_W	pulse width	CPU, CPD; HIGH or LOW; see Fig. 8								
		V_{CC} = 2.0 V	100	22	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
		MR HIGH; see Fig. 11								
		V_{CC} = 2.0 V	100	25	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	9	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	7	-	21	-	26	-	ns
		$\overline{PL}$ LOW; see Fig. 10								
		V_{CC} = 2.0 V	100	19	-	125	-	150	-	ns
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		V_{CC} = 6.0 V	17	6	-	21	-	26	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CPU, CPD; see Fig. 10								
		V_{CC} = 2.0 V	50	8	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	3	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	2	-	11	-	13	-	ns
		MR to CPU, CPD; see Fig. 11								
		V_{CC} = 2.0 V	50	0	-	65	-	75	-	ns
		V_{CC} = 4.5 V	10	0	-	13	-	15	-	ns
		V_{CC} = 6.0 V	9	0	-	11	-	13	-	ns
t_{su}	set-up time	Dn to $\overline{PL}$; see Fig. 12; CPU = CPD = HIGH								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	14	6	-	17	-	20	-	ns
t_h	hold time	Dn to $\overline{PL}$; see Fig. 12								
		V_{CC} = 2.0 V	0	-14	-	0	-	0	-	ns
		V_{CC} = 4.5 V	0	-5	-	0	-	0	-	ns
		V_{CC} = 6.0 V	0	-4	-	0		0	-	ns
		CPU to CPD, CPD to CPU; see Fig. 14								
		V_{CC} = 2.0 V	80	22	-	100	-	120	-	ns
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
		V_{CC} = 6.0 V	8	6	-	17	-	20	-	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
f_{max}	maximum frequency	CPU, CPD; see Fig. 8								
		V_{CC} = 2.0 V	4.0	13.5	-	3.2	-	2.6	-	MHz
		V_{CC} = 4.5 V	20	41	-	16	-	13	-	MHz
		V_{CC} = 6.0 V	24	49	-	19	-	15	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC}; V_{CC} = 5 V; [2] f_i = 1 MHz	-	24	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.
[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

Table 9. Dynamic characteristics type 74HCT193

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_{pd}	propagation delay	CPU, CPD to Qn; see Fig. 8 [1]								
		V_{CC} = 4.5 V	-	23	43	-	54	-	65	ns
		CPU to $\overline{TCU}$; see Fig. 9								
		V_{CC} = 4.5 V	-	15	27	-	34	-	41	ns
		CPD to $\overline{TCD}$; see Fig. 9								
		V_{CC} = 4.5 V	-	15	27	-	34	-	41	ns
		$\overline{PL}$ to Qn; see Fig. 10								
		V_{CC} = 4.5 V	-	26	46	-	58	-	69	ns
		MR to Qn; see Fig. 11								
		V_{CC} = 4.5 V	-	22	40	-	50	-	60	ns
		Dn to Qn; see Fig. 10								
		V_{CC} = 4.5 V	-	27	46	-	58	-	69	ns
		$\overline{PL}$ to $\overline{TCU}$, $\overline{PL}$ to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 4.5 V	-	31	55	-	69	-	83	ns
		MR to $\overline{TCU}$, MR to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 4.5 V	-	29	55	-	69	-	83	ns
		Dn to $\overline{TCU}$, Dn to $\overline{TCD}$; see Fig. 13								
		V_{CC} = 4.5 V	-	32	58	-	73	-	87	ns
t_{THL}	HIGH to LOW output transition time	see Fig. 11								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
t_{TLH}	LOW to HIGH output transition time	see Fig. 11								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
t_W	pulse width	CPU, CPD; HIGH or LOW; see Fig. 8								
		V_{CC} = 4.5 V	25	11	-	31	-	38	-	ns
		MR HIGH; see Fig. 11								
		V_{CC} = 4.5 V	20	7	-	25	-	30	-	ns
		$\overline{PL}$ LOW; see Fig. 10								
		V_{CC} = 4.5 V	20	8	-	25	-	30	-	ns
t_{rec}	recovery time	$\overline{PL}$ to CPU, CPD; see Fig. 10								
		V_{CC} = 4.5 V	10	2	-	13	-	15	-	ns
		MR to CPU, CPD; see Fig. 11								
		V_{CC} = 4.5 V	10	0	-	13	-	15	-	ns
t_{su}	set-up time	Dn to $\overline{PL}$; see Fig. 12; CPU = CPD = HIGH								
		V_{CC} = 4.5 V	16	8	-	20	-	24	-	ns
t_h	hold time	Dn to $\overline{PL}$; see Fig. 12								
		V_{CC} = 4.5 V	0	-6	-	0	-	0	-	ns
		CPU to CPD, CPD to CPU; see Fig. 14								
		V_{CC} = 4.5 V	16	7	-	20	-	24	-	ns
f_{max}	maximum frequency	CPU, CPD; see Fig. 8								
		V_{CC} = 4.5 V	20	43	-	16	-	13	-	MHz
C_{PD}	power dissipation capacitance	V_I = GND to V_{CC} - 1.5 V; V_{CC} = 5 V; f_i = 1 MHz [2]	-	26	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PHL} and t_{PLH}.

[2] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

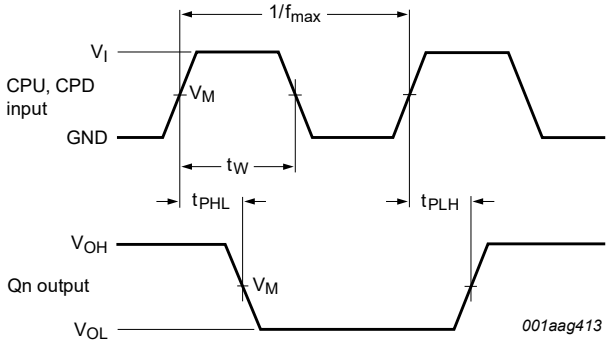
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

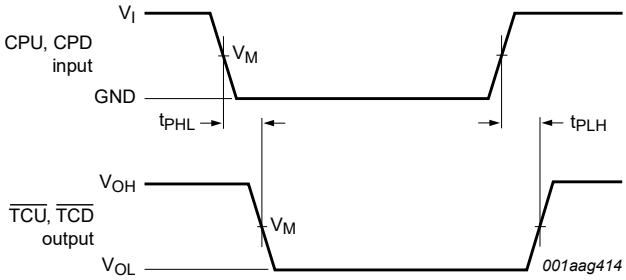
10.1. Waveforms and test circuit



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

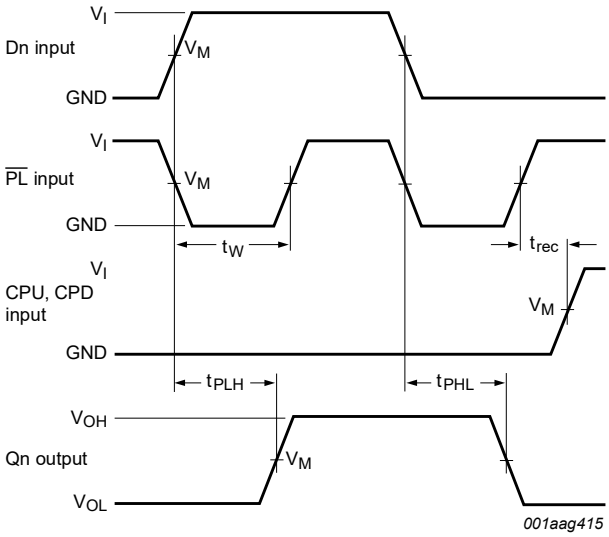
Fig. 8. The clock (CPU, CPD) to output (Qn) propagation delays, the clock pulse width, and the maximum clock pulse frequency



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

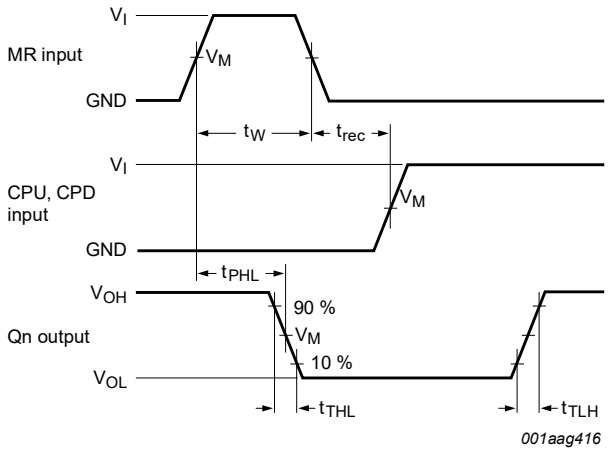
Fig. 9. The clock (CPU, CPD) to terminal count output ($\overline{TCU}$, $\overline{TCD}$) propagation delays



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

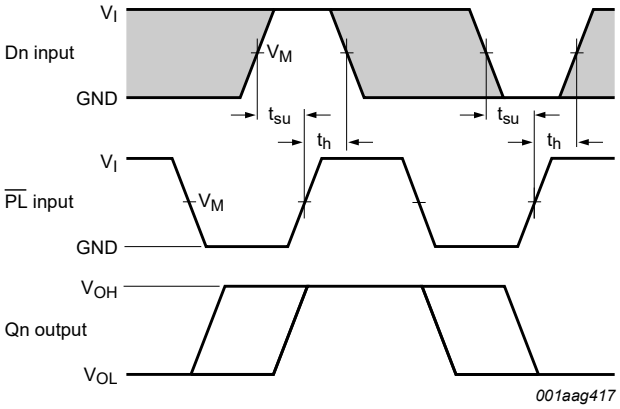
Fig. 10. The parallel load input ($\overline{PL}$) and data (Dn) to Qn output propagation delays and $\overline{PL}$ removal time to clock input (CPU, CPD)



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 11. The master reset input (MR) pulse width, MR to Qn propagation delays, MR to CPU, CPD removal time and output transition times

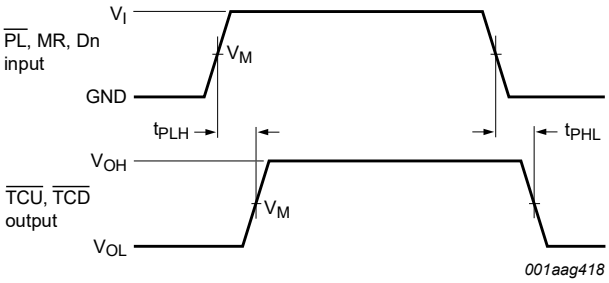


Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

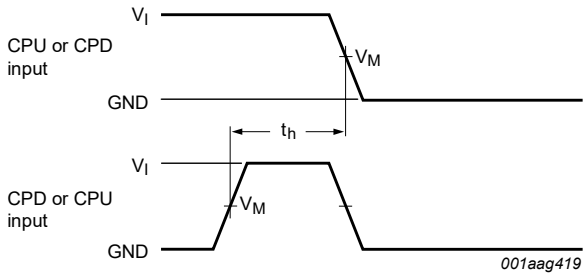
Fig. 12. The data input (Dn) to parallel load input ($\overline{PL}$) set-up and hold times



Measurement points are given in Table 10.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 13. The data input (Dn), parallel load input ($\overline{PL}$) and the master reset input (MR) to the terminal count outputs ($\overline{TCU}$, $\overline{TCD}$) propagation delays

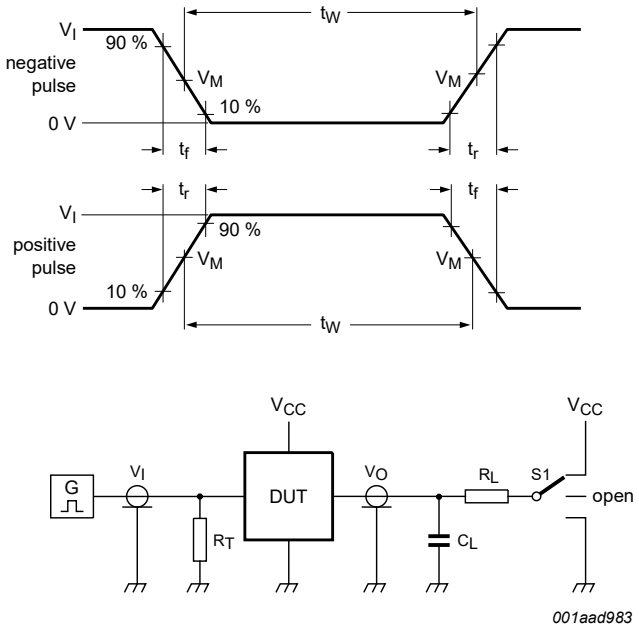


Measurement points are given in Table 10.

Fig. 14. The CPU to CPD or CPD to CPU hold times

Table 10. Measurement points

Type	Input		Output
	V_M	V_I	V_M
74HC193	0.5 × V_{CC}	GND to V_{CC}	0.5 × V_{CC}
74HCT193	1.3 V	GND to 3 V	1.3 V



Test data is given in Table 11.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistor

S1 = Test selection switch

Fig. 15. Test circuit for measuring switching times

Table 11. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC193	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT193	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information

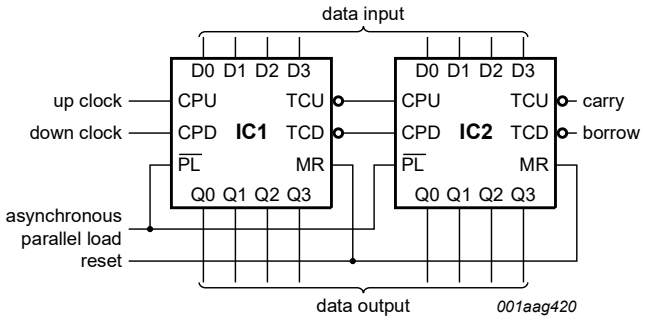
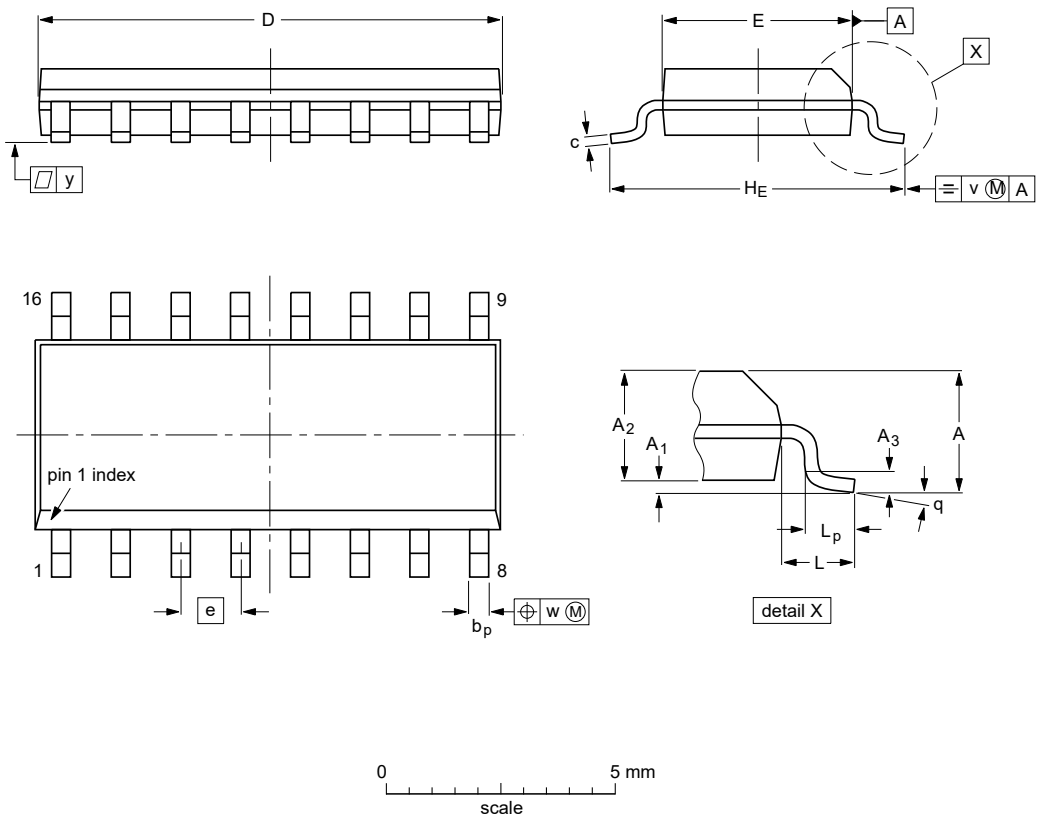


Fig. 16. Application for cascaded up/down counter with parallel load

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**



Dimensions (inch dimensions are derived from the original mm dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.75	0.25			0.51	0.25	10.0	4.0		6.2		1.27				8°
	nom				0.25					1.27		1.05		0.2	0.25	0.1	
	min		0.10	1.25		0.31	0.10	9.8	3.8		5.8		0.4				0°
inches	max	0.069	0.010			0.020	0.010	0.394	0.16		0.244		0.05				8°
	nom				0.01					0.05		0.041		0.008	0.01	0.004	
	min		0.004	0.049		0.012	0.004	0.386	0.15		0.228		0.016				0°

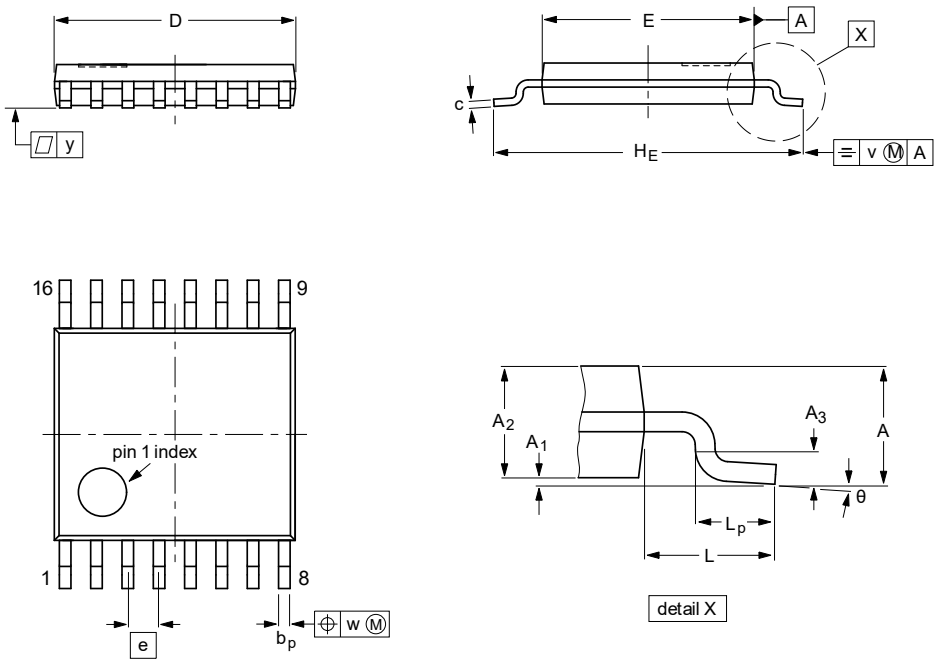
Note
1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

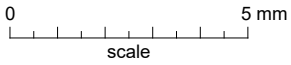
sot109-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT109-1		MS-012				~~03-02-19~~ 23-10-27

Fig. 17. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**





Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	θ
mm	max	1.20	0.15	1.05		0.30	0.2	5.1	4.5		6.6		0.75				8°
	nom				0.25					0.65		1		0.2	0.1	0.1	
	min		0.05	0.80		0.19	0.09	4.9	4.3		6.2		0.45				0°

Note
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot403-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~03-02-18~~ 23-10-27

Fig. 18. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT193 v.8	20240314	Product data sheet	-	74HC_HCT193 v.7
Modifications:	• Fig. 17, Fig. 18: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153. • Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT193 v.7	20210910	Product data sheet	-	74HC_HCT193 v.6
Modifications:	• Section 2 updated. • Type number 74HCT193DB (SOT338-1/SSOP16) removed.			
74HC_HCT193 v.6	20210205	Product data sheet	-	74HC_HCT193 v.5
Modifications:	• Type number 74HC193DB (SOT338-1/SSOP16) removed. • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT193 v.5	20160129	Product data sheet	-	74HC_HCT193 v.4
Modifications:	• Type numbers 74HC193N and 74HCT193N (SOT38-4) removed.			
74HC_HCT193 v.4	20130624	Product data sheet	-	74HC_HCT193 v.3
Modifications:	• General description updated.			
74HC_HCT193 v.3	20070523	Product data sheet	-	74HC_HCT193_CNV v.2
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Family specification included.			
74HC_HCT193_CNV v.2	19970828	Product specification	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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