



PSMN011-60HL

N-channel 60 V, 11.5 mOhm, logic level MOSFET in LPAK56D using TrenchMOS technology

30 September 2022

Product data sheet

1. General description

Dual logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology.

2. Features and benefits

- Dual MOSFET
- Repetitive avalanche rated
- High reliability LPAK56D package
- Copper-clip, solder die attach
- Qualified to 175 °C

3. Applications

- Brushless DC motor control
- DC-to-DC converters
- High-performance synchronous rectification
- High performance and high efficiency server power supply

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	60	V
I_D	drain current	$V_{GS} = 5\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	-	35	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	-	68	W
T_j	junction temperature			-55	-	175	°C
Static characteristics FET1 and FET2							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 25\text{ °C}$; Fig. 11		-	9.5	11.5	mΩ
		$V_{GS} = 5\text{ V}$; $I_D = 15\text{ A}$; $T_j = 175\text{ °C}$; Fig. 11 ; Fig. 12		-	21.5	26	mΩ
Dynamic characteristics FET1 and FET2							
Q_{GD}	gate-drain charge	$I_D = 15\text{ A}$; $V_{DS} = 48\text{ V}$; $V_{GS} = 5\text{ V}$; $T_j = 25\text{ °C}$; Fig. 13 ; Fig. 14		-	8.27	-	nC
$Q_{G(tot)}$	total gate charge			-	24.5	-	nC
Avalanche Ruggedness FET1 and FET2							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 35\text{ A}$; $V_{sup} \leq 60\text{ V}$; $V_{GS} = 5\text{ V}$; $T_{j(init)} = 25\text{ °C}$; Fig. 4	[2] [3]	-	-	118	mJ

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode FET1 and FET2						
Q_r	recovered charge	$I_S = 15 \text{ A}$; $di_S/dt = -100 \text{ A}/\mu\text{s}$; $V_{GS} = 0 \text{ V}$; $V_{DS} = 30 \text{ V}$; $T_j = 25 \text{ }^\circ\text{C}$	-	18.1	-	nC

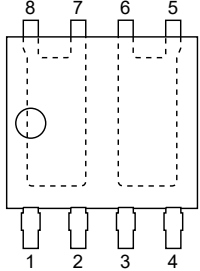
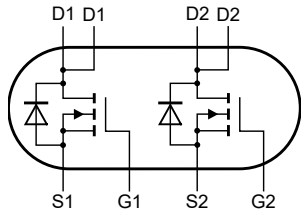
[1] Continuous current is limited by package.

[2] Refer to application note AN10273 for further information

[3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D; Dual LFPAK (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
PSMN011-60HL	LFPAK56D; Dual LFPAK	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN011-60HL	11RL60H

8. Limiting values

Table 5. Limiting values

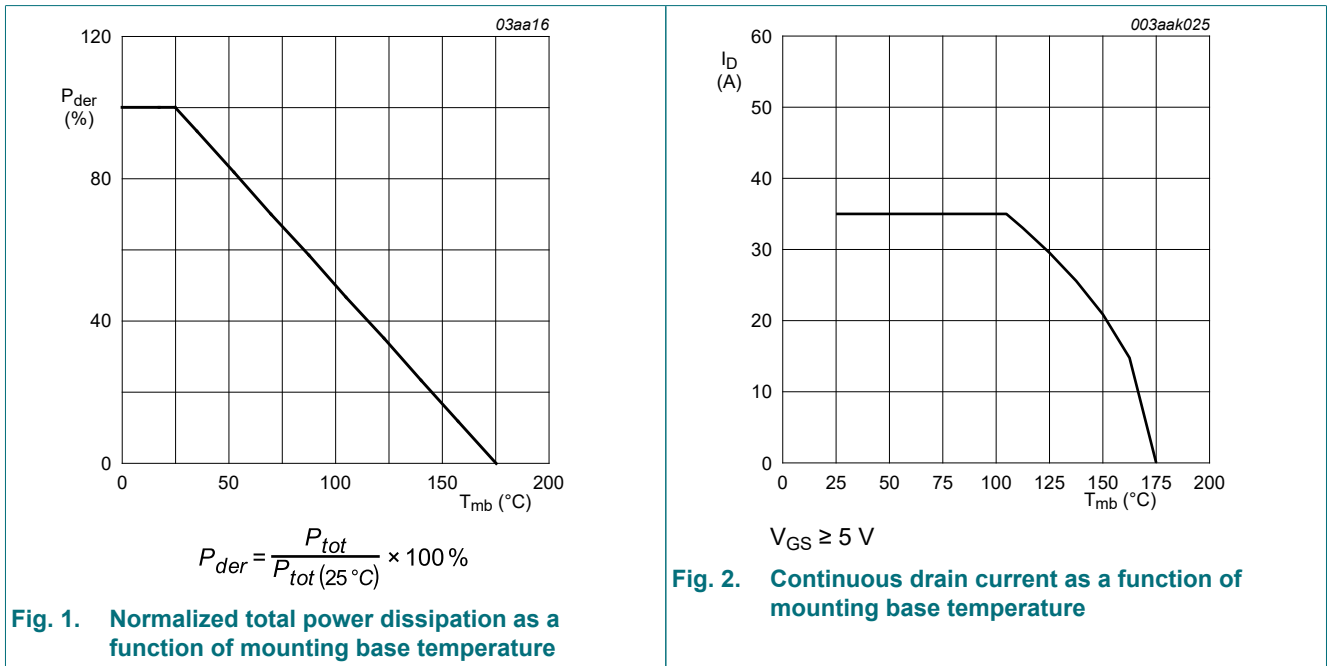
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25 \text{ }^\circ\text{C} \leq T_j \leq 175 \text{ }^\circ\text{C}$	-	60	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20 \text{ k}\Omega$	-	60	V
V_{GS}	gate-source voltage	DC; $T_j \leq 175 \text{ }^\circ\text{C}$	-10	10	V
		Pulsed; $T_j \leq 175 \text{ }^\circ\text{C}$	[1] [2] -15	15	V
P_{tot}	total power dissipation	$T_{mb} = 25 \text{ }^\circ\text{C}$; Fig. 1	-	68	W

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Symbol	Parameter	Conditions		Min	Max	Unit
I _D	drain current	V _{GS} = 5 V; T _{mb} = 25 °C; Fig. 2	[3]	-	35	A
		V _{GS} = 5 V; T _{mb} = 100 °C; Fig. 2	[3]	-	35	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	204	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode FET1 and FET2						
I _S	source current	T _{mb} = 25 °C	[3]	-	35	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	204	A
Avalanche Ruggedness FET1 and FET2						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 35 A; V _{sup} ≤ 60 V; V _{GS} = 5 V; T _{j(init)} = 25 °C; Fig. 4	[4] [5]	-	118	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm
- [2] Significantly longer life times are achieved by lowering T_j and/or V_{GS}
- [3] Continuous current is limited by package.
- [4] Refer to application note AN10273 for further information
- [5] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



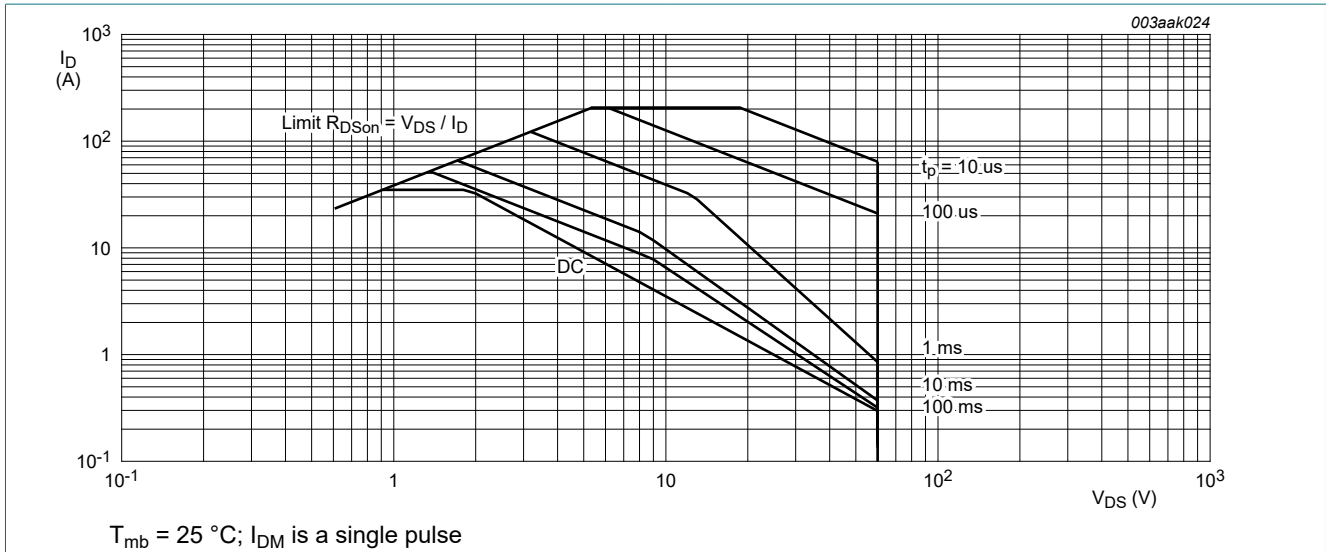


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

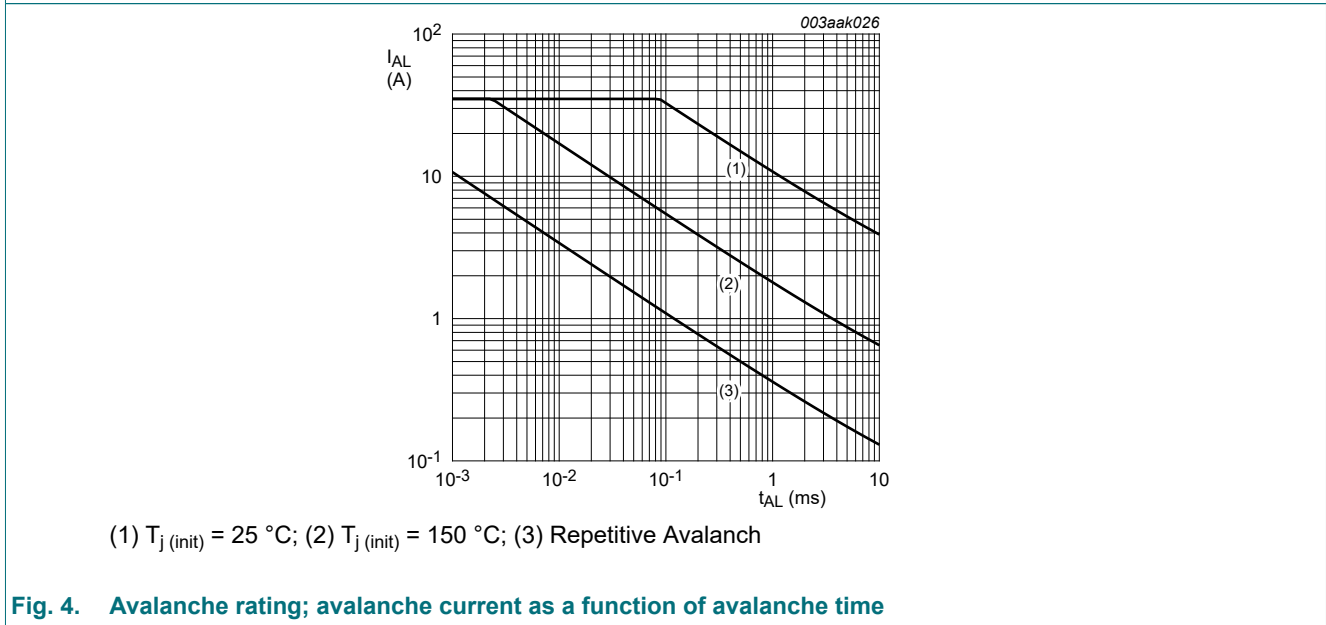


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.21	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

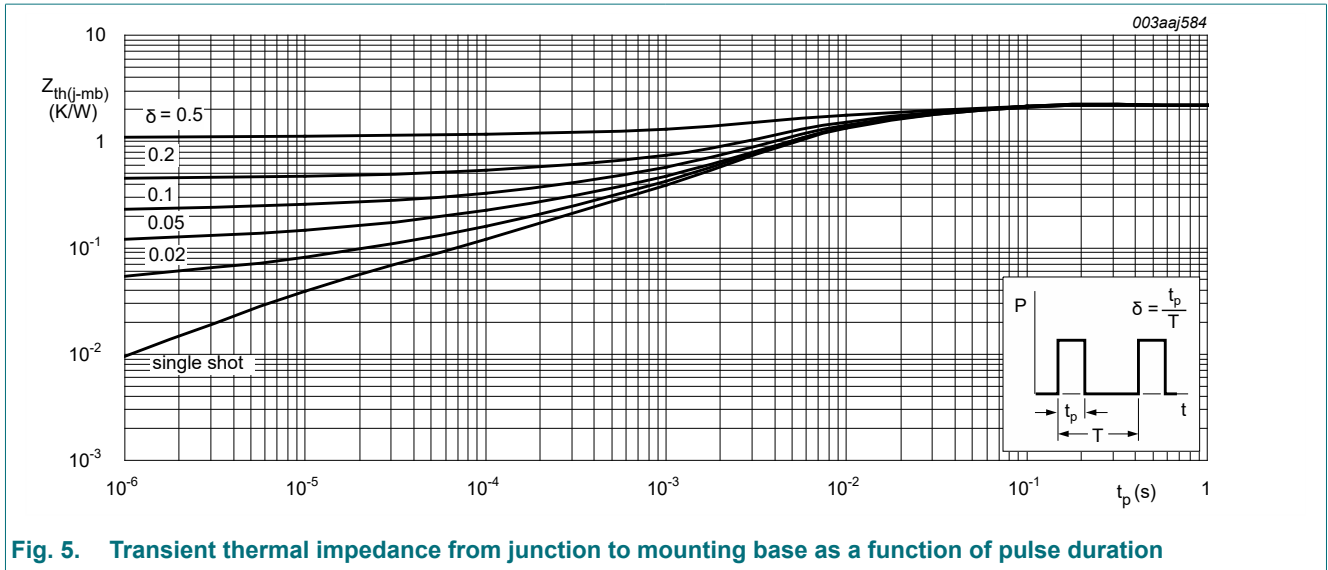


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

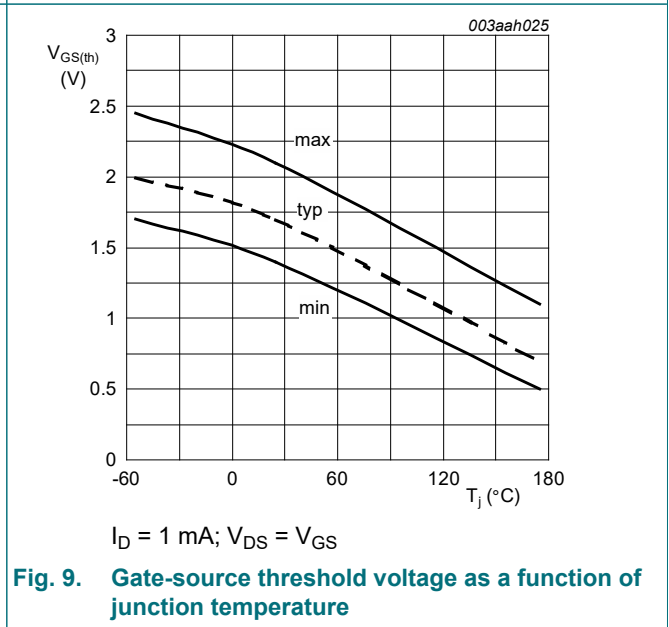
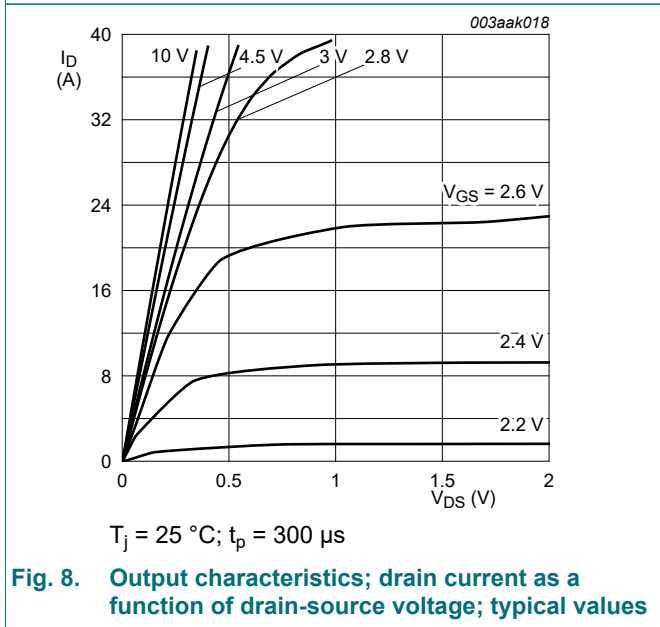
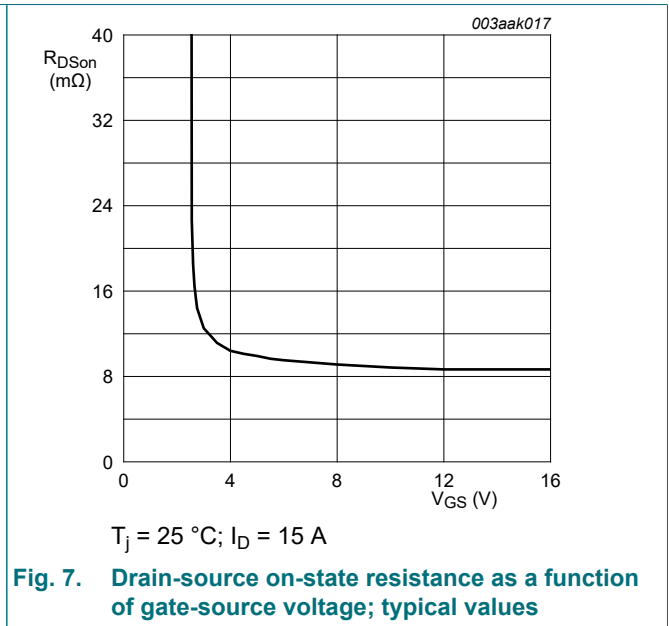
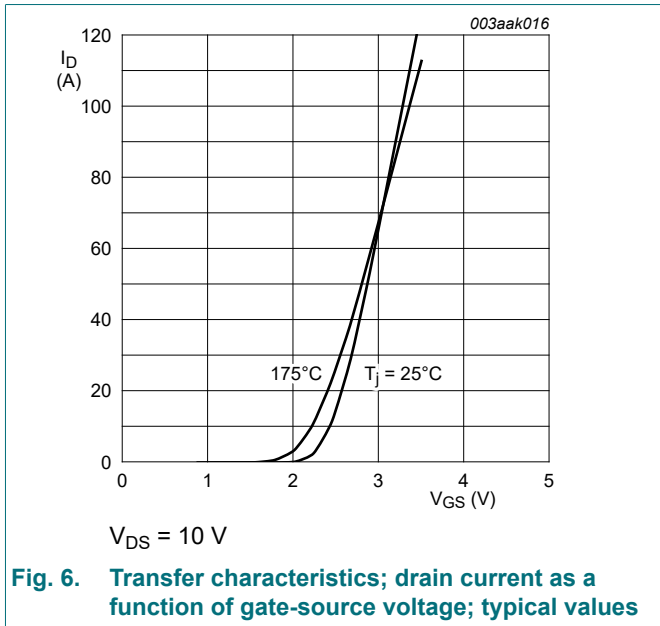
10. Characteristics

Table 7. Characteristics

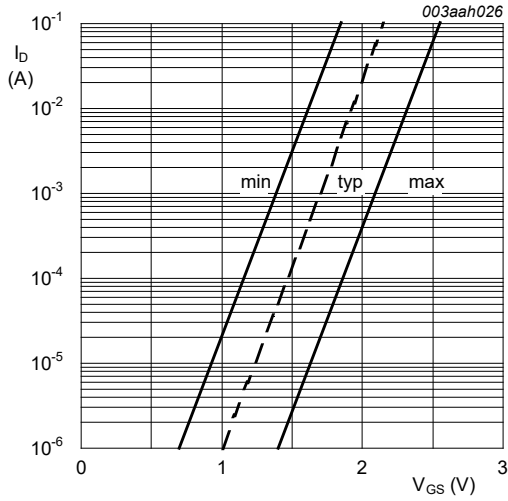
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics FET1 and FET2						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ C$; Fig. 9; Fig. 10	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ C$; Fig. 9; Fig. 10	0.5	-	-	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ C$; Fig. 9; Fig. 10	-	-	2.45	V
I_{DSS}	drain leakage current	$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.02	1	μA
		$V_{DS} = 60 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	-	500	μA
I_{GSS}	gate leakage current	$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	9.5	11.5	m Ω
		$V_{GS} = 5 \text{ V}; I_D = 15 \text{ A}; T_j = 175 \text{ }^\circ C$; Fig. 11; Fig. 12	-	21.5	26	m Ω
		$V_{GS} = 10 \text{ V}; I_D = 15 \text{ A}; T_j = 25 \text{ }^\circ C$; Fig. 11	-	8.5	10.7	m Ω
Dynamic characteristics FET1 and FET2						
$Q_{G(tot)}$	total gate charge	$I_D = 15 \text{ A}; V_{DS} = 48 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ C$; Fig. 13; Fig. 14	-	24.5	-	nC
Q_{GS}	gate-source charge		-	5.4	-	nC
Q_{GD}	gate-drain charge		-	8.27	-	nC
C_{iss}	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ C$; Fig. 15	-	2602	3470	pF
C_{oss}	output capacitance		-	237	284	pF
C_{rss}	reverse transfer capacitance		-	126	173	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 48 \text{ V}; R_L = 3.2 \text{ } \Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ C$	-	15.1	-	ns
t_r	rise time		-	28	-	ns

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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(off)}$	turn-off delay time		-	31.5	-	ns
t_f	fall time		-	25.3	-	ns
Source-drain diode FET1 and FET2						
V_{SD}	source-drain voltage	$I_S = 10\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 16	-	0.78	1.2	V
t_{rr}	reverse recovery time	$I_S = 15\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$;	-	22.6	-	ns
Q_r	recovered charge	$V_{DS} = 30\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$	-	18.1	-	nC

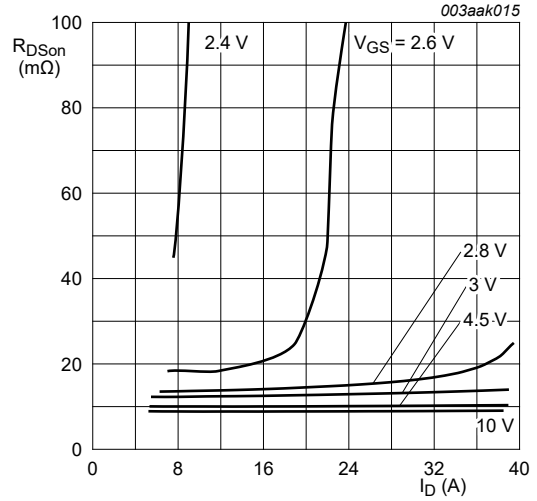


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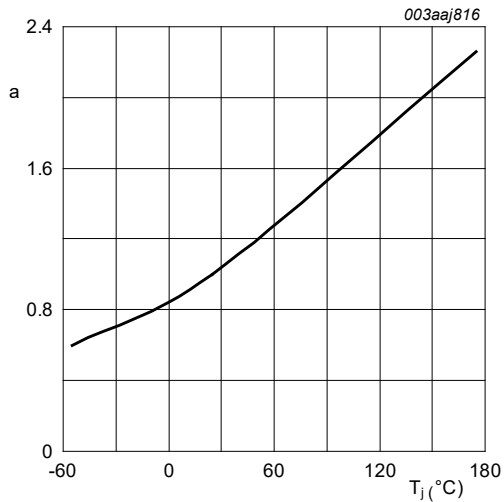
$T_j = 25\text{ }^\circ\text{C}; V_{DS} = 5\text{ V}$

Fig. 10. Sub-threshold drain current as a function of gate-source voltage



$T_j = 25\text{ }^\circ\text{C}; t_p = 300\text{ }\mu\text{s}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon.(25^\circ\text{C})}}$$

Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

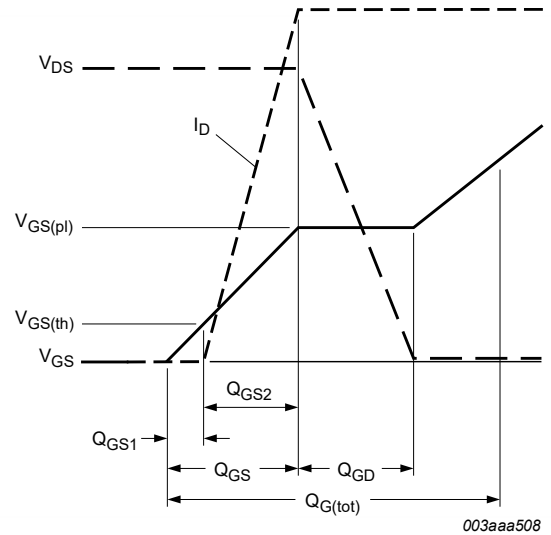
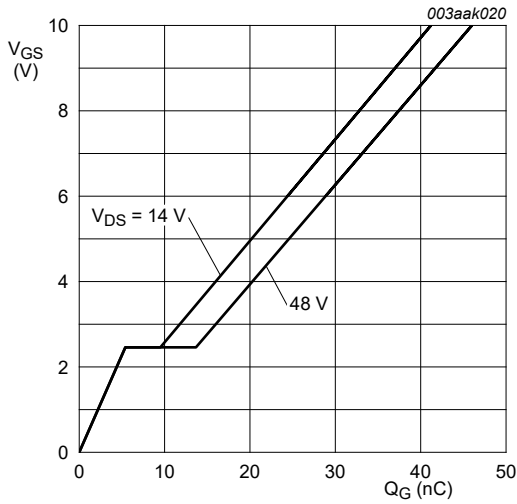


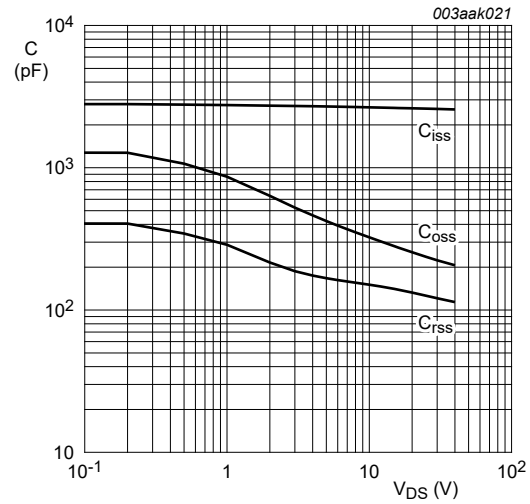
Fig. 13. Gate charge waveform definitions

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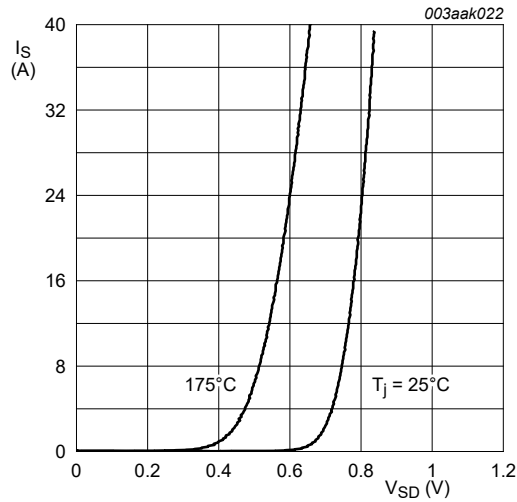
$T_j = 25\text{ }^\circ\text{C}; I_D = 15\text{ A}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0\text{ V}$

Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

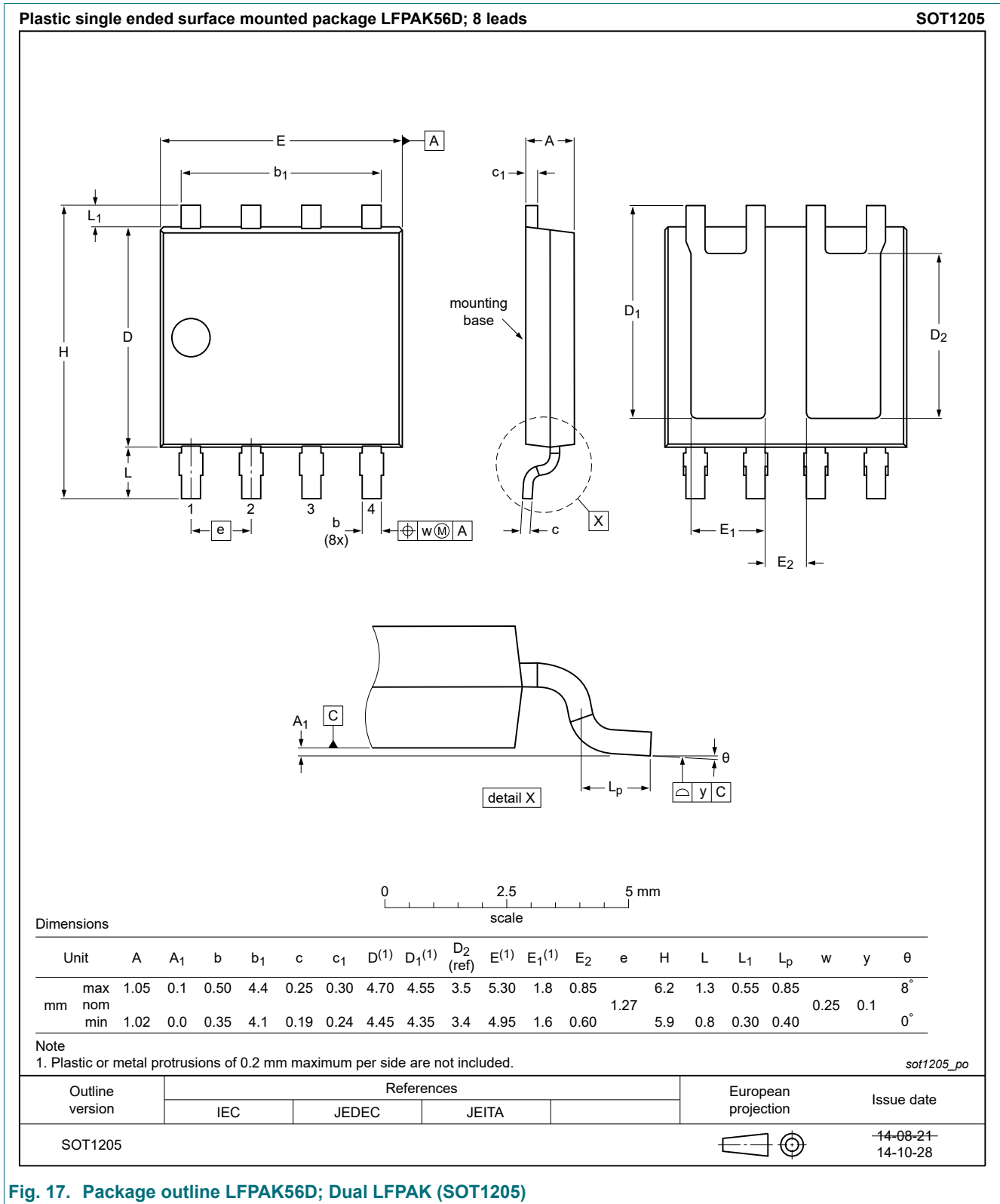


Fig. 17. Package outline LPAK56D; Dual LPAK (SOT1205)

12. Soldering

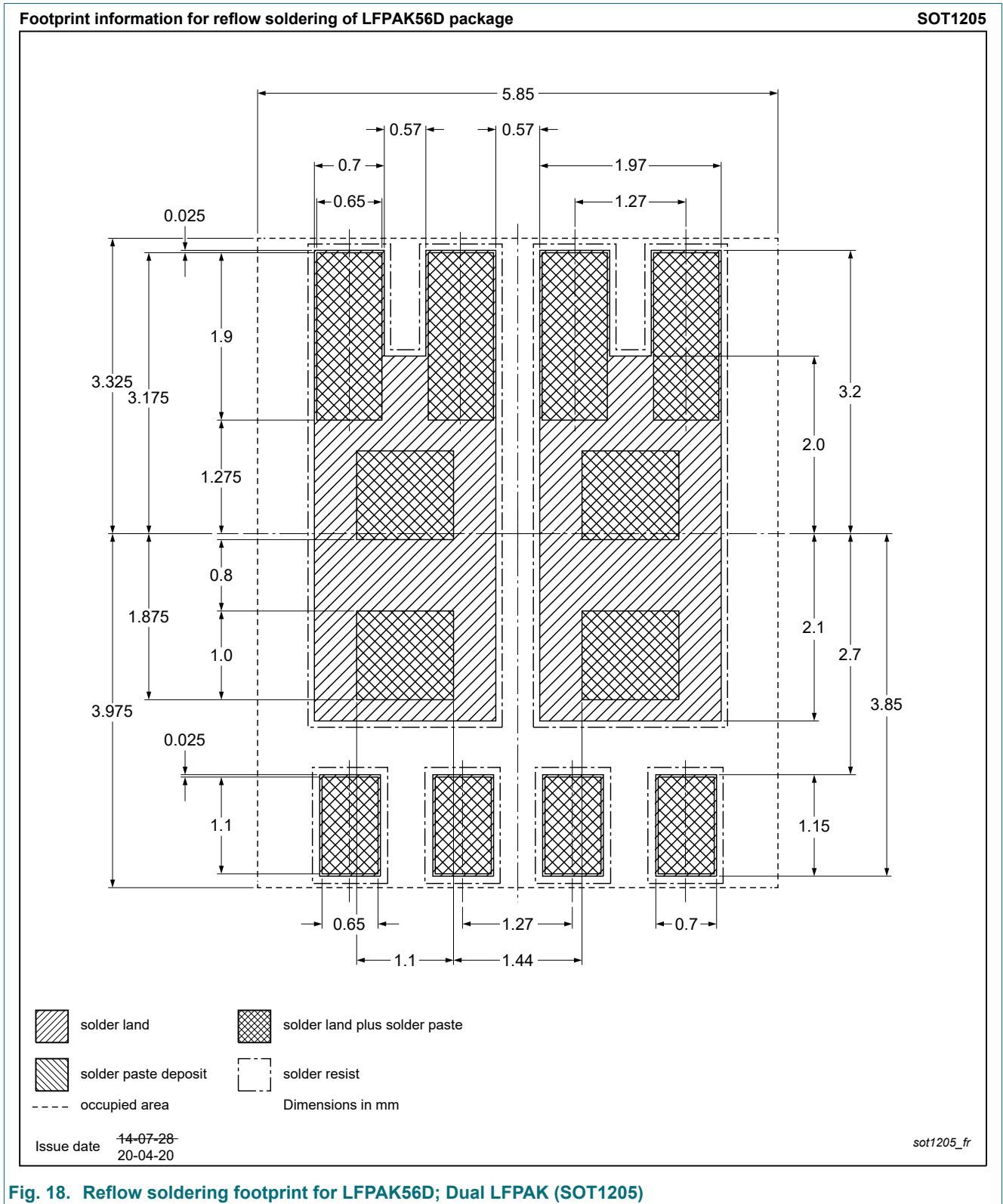


Fig. 18. Reflow soldering footprint for LPAK56D; Dual LPAK (SOT1205)

13. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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