



PESD2ETH-AD

Ultra low capacitance double rail-to-rail ESD protection diode

14 December 2017

Product data sheet

1. General description

Ultra low capacitance double rail-to-rail ElectroStatic Discharge (ESD) protection diode in a small SOT457 Surface-Mounted Device (SMD) plastic package.

The device is designed to protect two high-speed data lines or high frequency signal lines from the damage caused by ESD and other transients.

The device integrates two ultra low capacitance rail-to-rail diodes and one additional ESD protection diode to ensure signal line protection even if no supply voltage is available.

2. Features and benefits

- ESD protection of two high-speed data lines
- ultra low capacitance: $C_D = 2$ pF
- ISO 10605 (330 pF, 2 k Ω) up to 23 kV
- ESD protection up to 12 kV (IEC61000-4-2)
- AEC-Q101 qualified

3. Applications

- 100BASE-T1 / OPEN Alliance BroadR-Reach automotive Ethernet
- Low-Voltage Differential Signaling (LVDS) automotive
- USB 2.0 automotive

4. Quick reference data

Table 1. Quick reference data

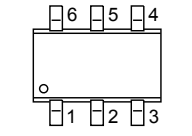
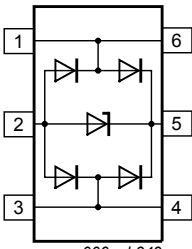
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{RWM}	reverse standoff voltage	$T_{amb} = 25$ °C		-	-	5.5	V
Zener diode							
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	[1]	-	20	-	pF
Per channel							
C_d	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	[2]	-	2	2.3	pF

[1] Measured from pin 5 to ground.

[2] Measured from pin 4 or 6 to ground.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I/O 1	input/output 1	 TSOP6 (SOT457)	 006aab349
2	GND	ground		
3	I/O 2	input/output 2		
4	I/O 2	input/output 2		
5	V _{CC}	supply voltage		
6	I/O 1	input/output 1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD2ETH-AD	TSOP6	plastic, surface-mounted package (SC-74)	SOT457

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD2ETH-AD	L9

8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	3.5	A
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
V _{ESD}	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[3] [2]	-	12	kV
		MIL-STD-883 (human body model)		-	10	kV

- [1] According to IEC61000-4-5.
[2] Measured from pin 1,3,4 or 6 to GND.
[3] Device stressed with ten non-repetitive ESD pulses.

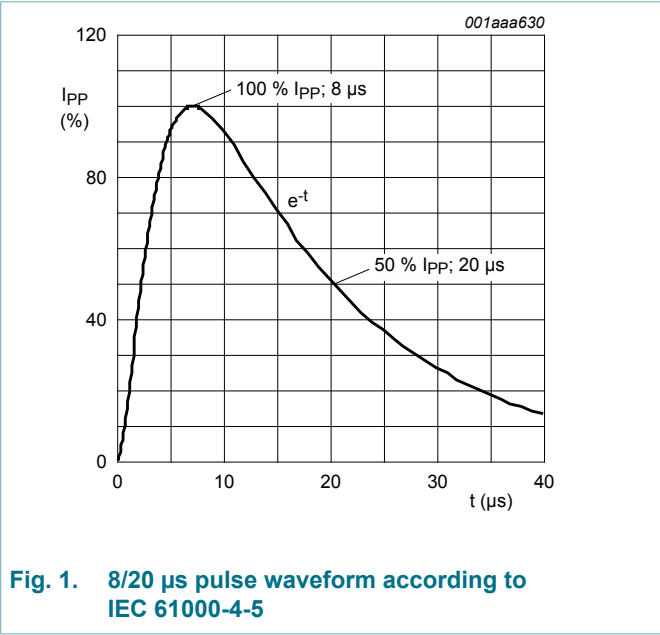


Fig. 1. 8/20 μs pulse waveform according to IEC 61000-4-5

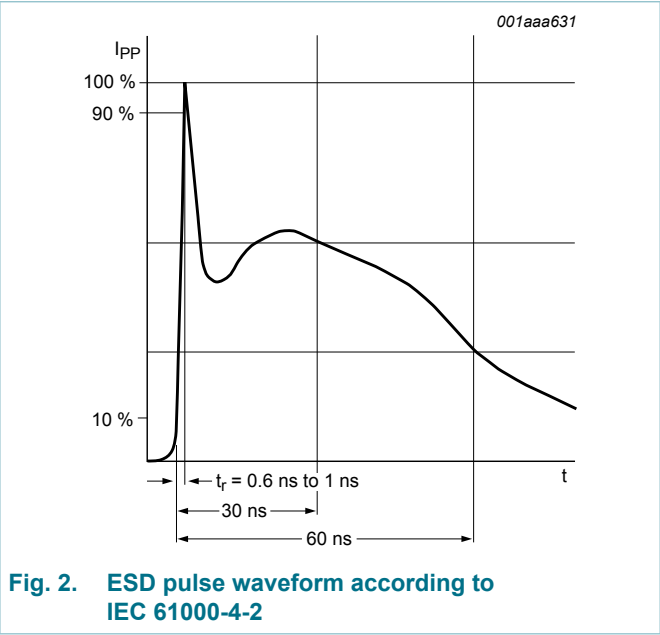


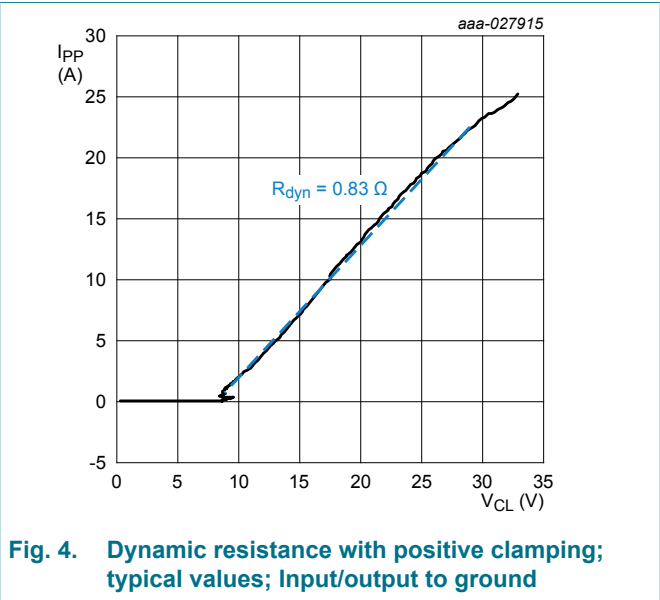
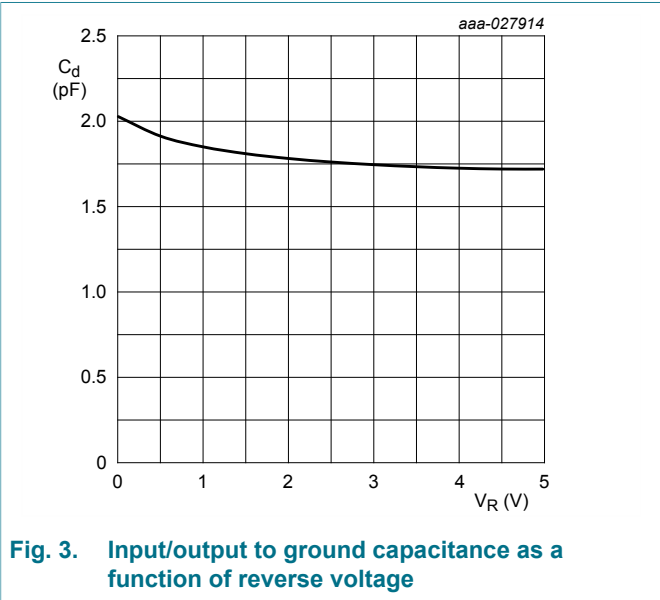
Fig. 2. ESD pulse waveform according to IEC 61000-4-2

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	5.5	V
V _F	forward voltage	I _F = 1 mA; T _{amb} = 25 °C		-	0.7	-	V
I _{RM}	reverse leakage current	V _R = 5.5 V; T _{amb} = 25 °C	[1]	-	1	100	nA
V _{CL}	clamping voltage	I _{PPM} = 3.5 A; 8/20 μs; T _{amb} = 25 °C	[1]	-	12.3	-	V
R _{dyn}	dynamic resistance	I _R = 10 A; T _{amb} = 25 °C	[1] [2]	-	0.83	-	Ω
Zener diode							
V _{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C	[3]	6	-	9	V
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[3]	-	20	-	pF
Per channel							
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C	[4]	-	2	2.3	pF

- [1] Measured from pin 1,3,4 or 6 to GND.
[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t_p = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.
[3] Measured from pin 5 to ground.
[4] Measured from pin 4 or 6 to ground.



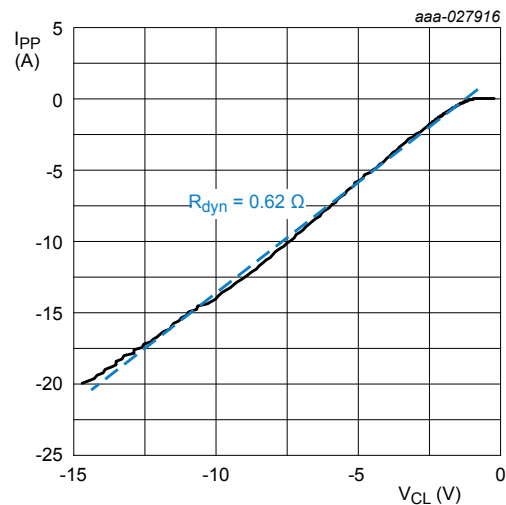


Fig. 5. Dynamic resistance with negative clamping; typical values; Input/output to ground

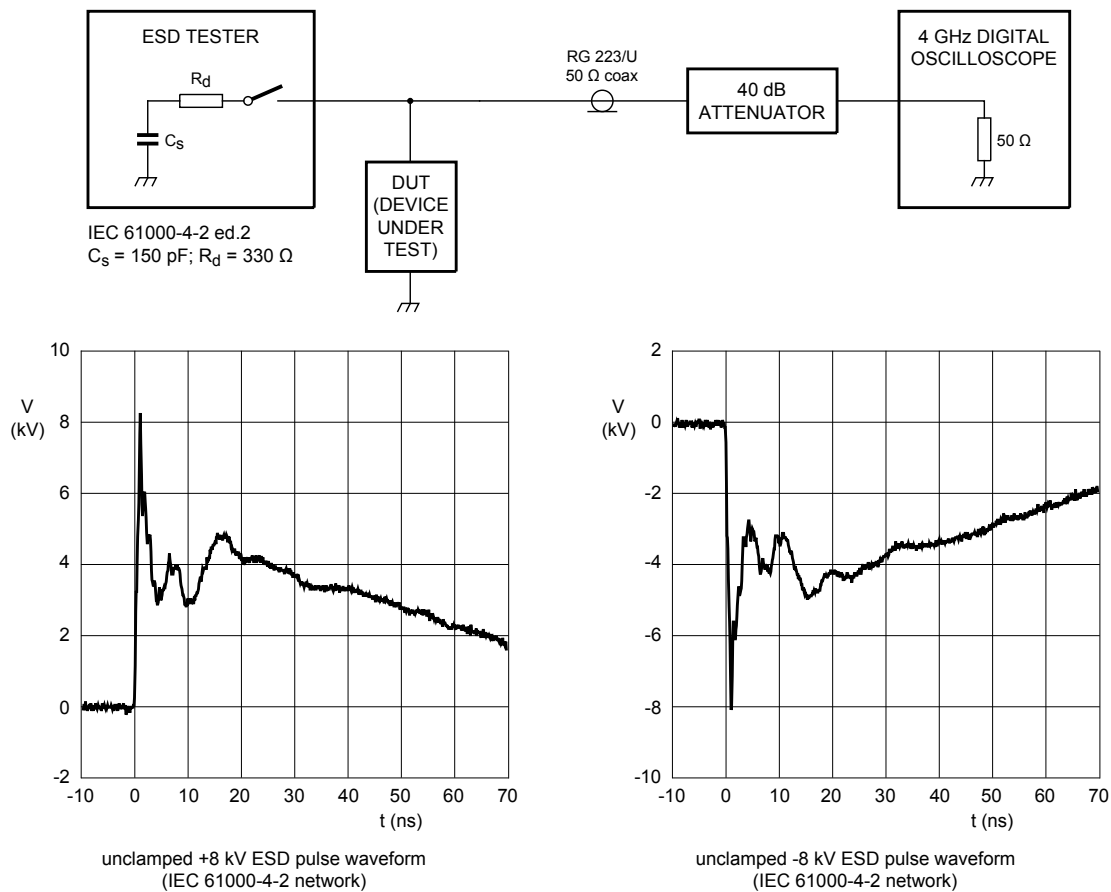


Fig. 6. ESD clamping test setup and waveforms

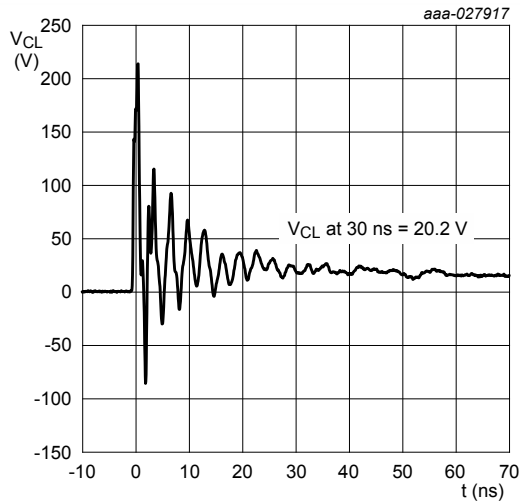


Fig. 7. Clamped +8kV pulse waveform (IEC61000-4-2 network)

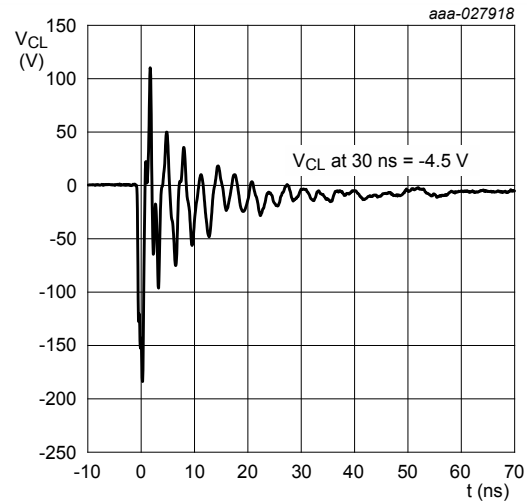


Fig. 8. Clamped -8kV pulse waveform (IEC61000-4-2 network)

10. Application information

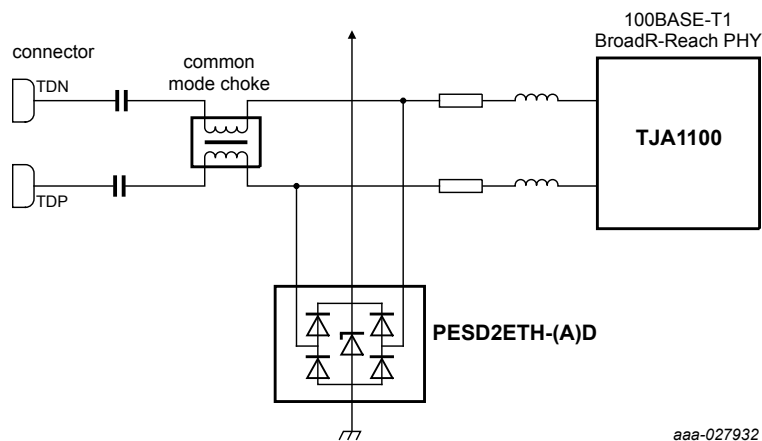


Fig. 9. Application diagram: BroadR-Reach PHY / 100BASE-T1

Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

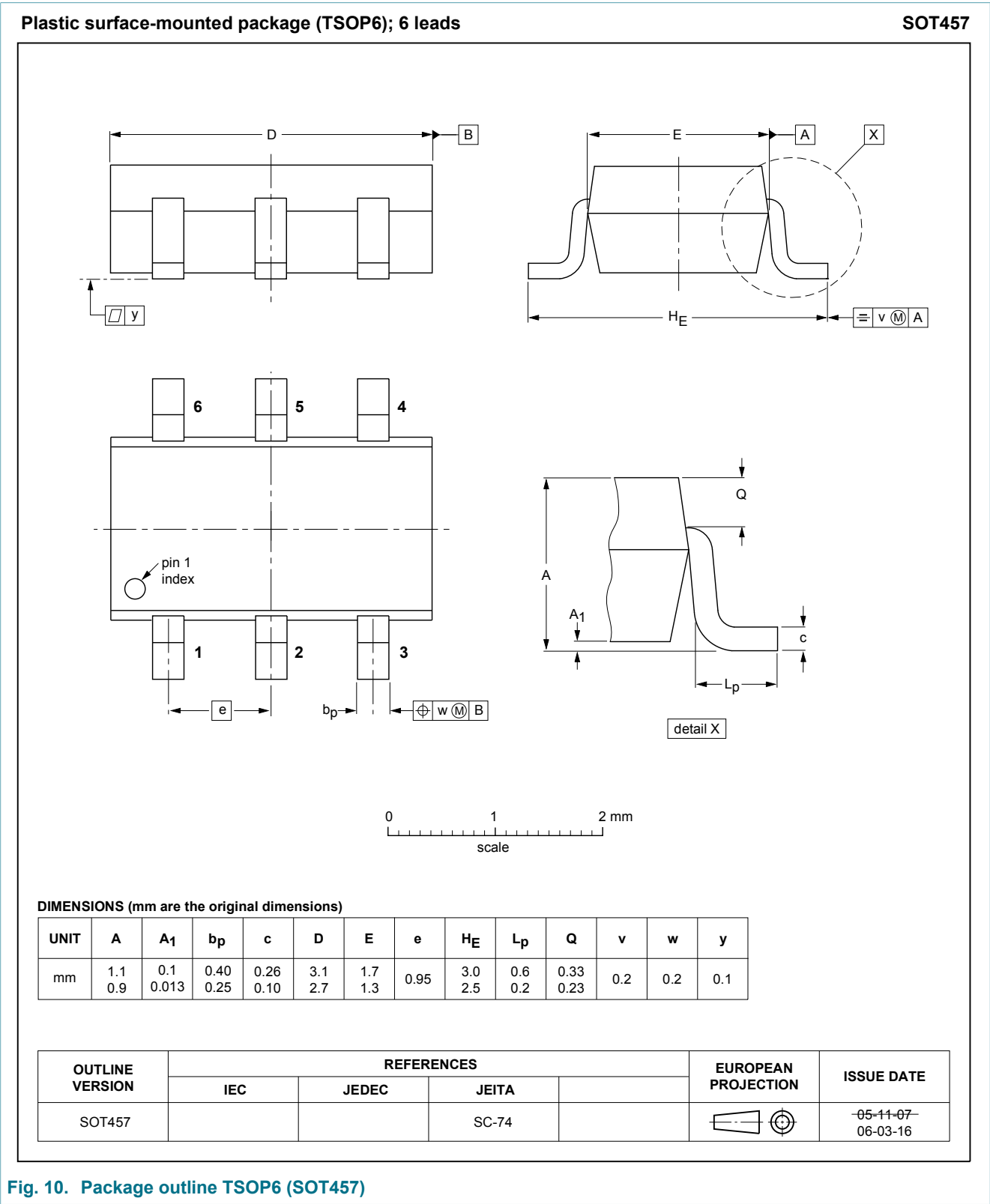


Fig. 10. Package outline TSOP6 (SOT457)

13. Soldering

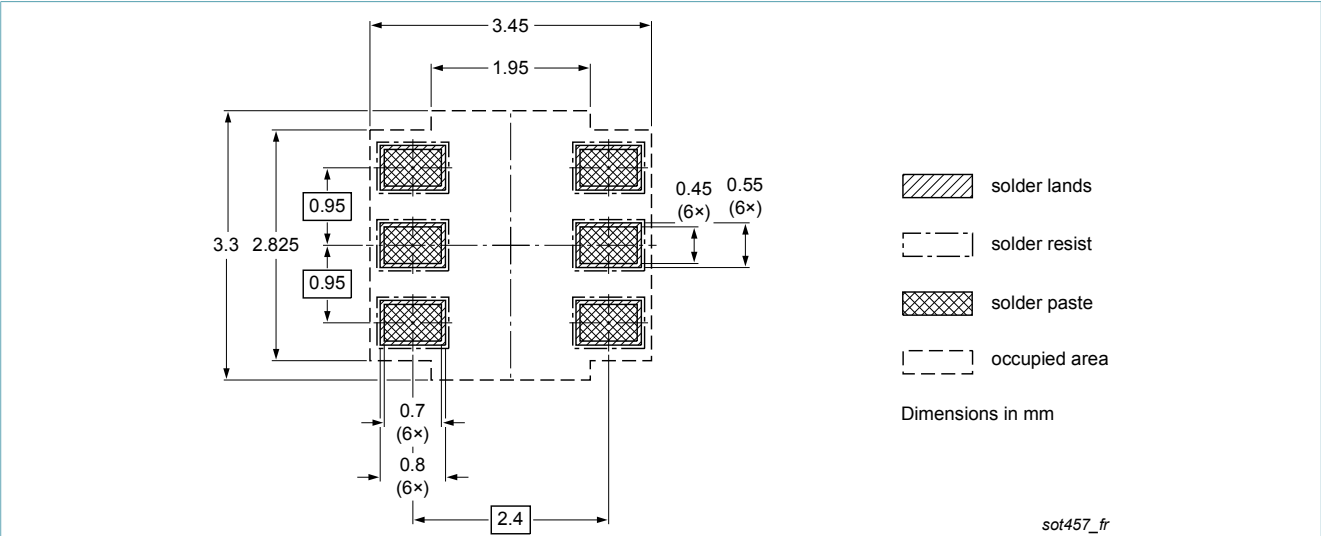


Fig. 11. Reflow soldering footprint for TSOP6 (SOT457)

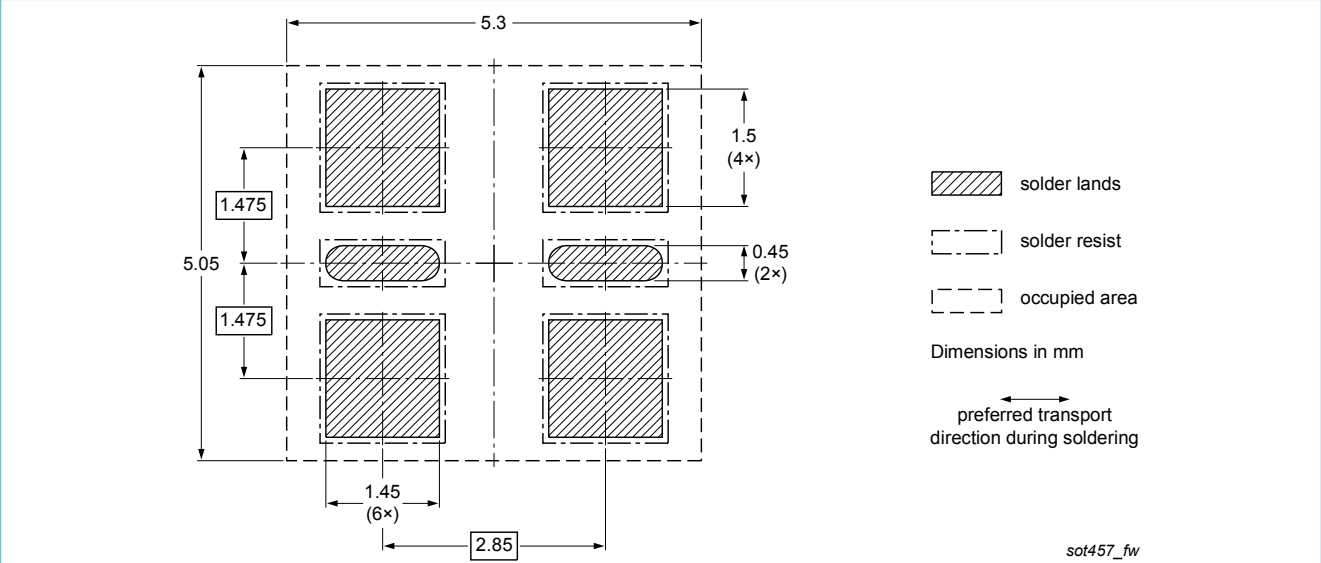


Fig. 12. Wave soldering footprint for TSOP6 (SOT457)

14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD2ETH-AD v.1	20171214	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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