

74CBTLV3244

8-bit bus switch with 4-bit output enables

Rev. 6 — 24 June 2024

Product data sheet

1. General description

The 74CBTLV3244 is a dual 4-pole, single-throw bus switch. The device features two output enable inputs (\overline{nOE}) that each control four switch channels. The switches are disabled when the associated \overline{nOE} input is HIGH. Schmitt trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

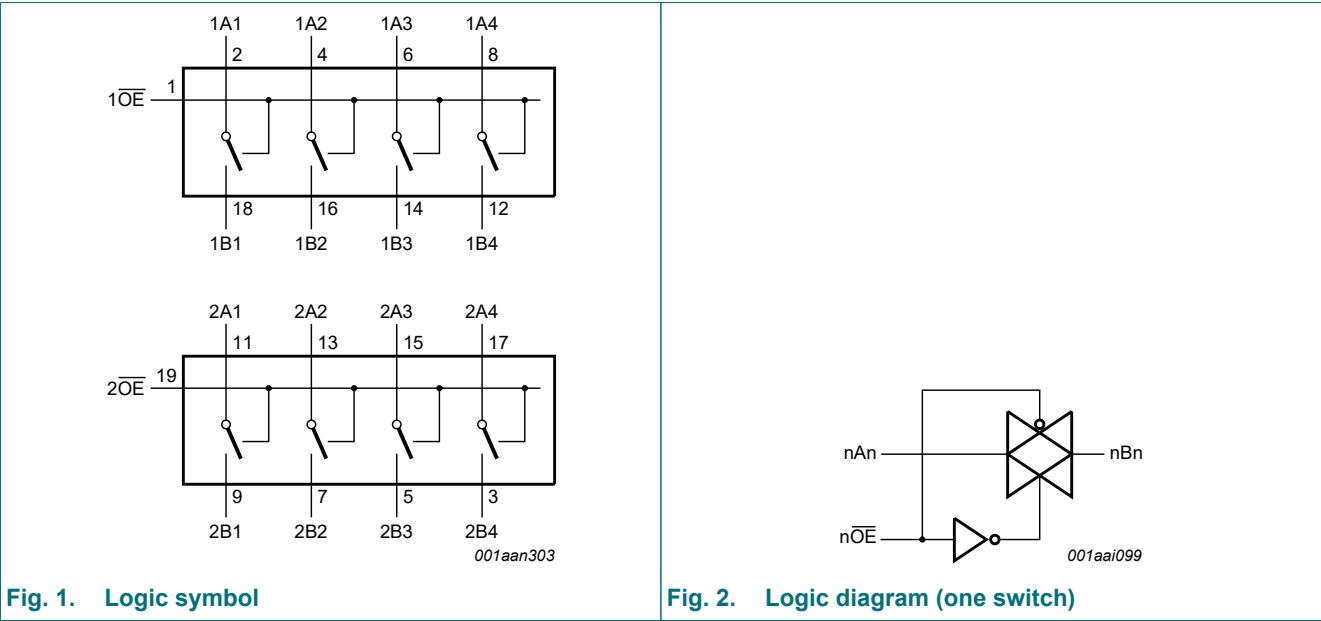
- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

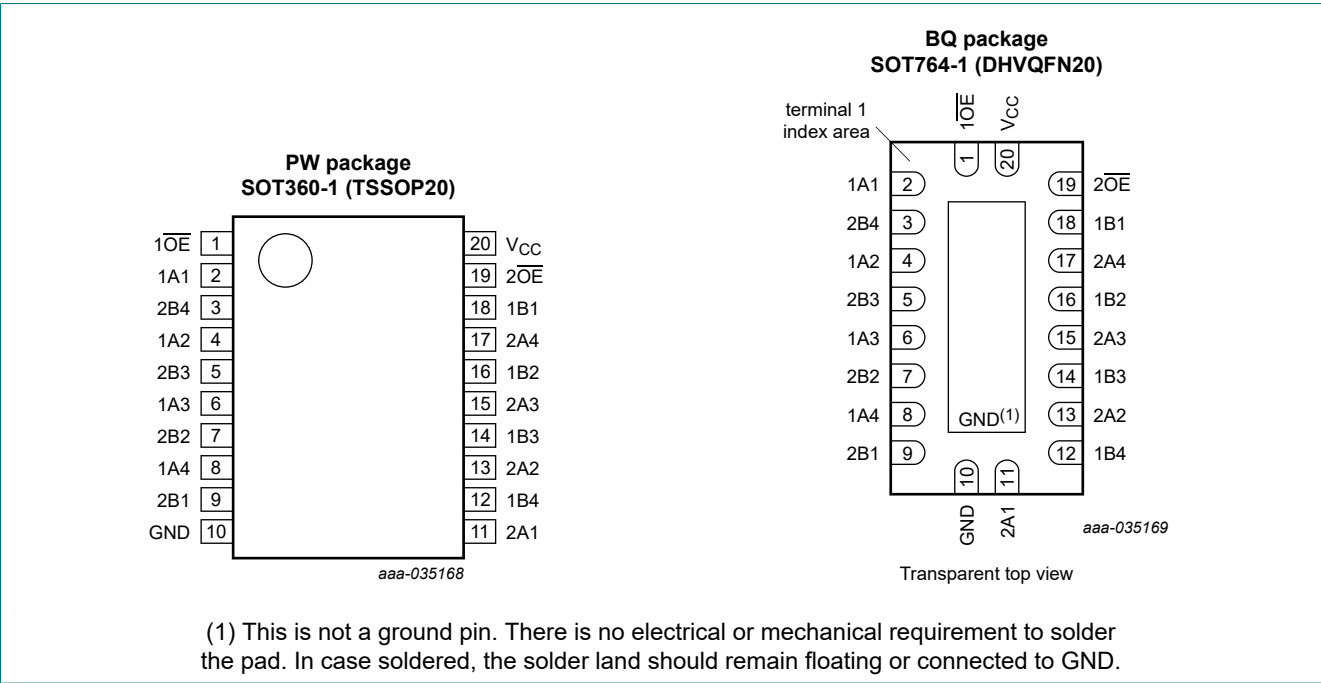
| Type number | Package | | | |
|-------------------------------|-------------------|----------|--|--------------------------|
| | Temperature range | Name | Description | Version |
| 74CBTLV3244PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74CBTLV3244BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--------------------|----------------|----------------------------------|
| 1OE, 2OE | 1, 19 | output enable input (active LOW) |
| 1A1, 1A2, 1A3, 1A4 | 2, 4, 6, 8 | data input/output (A port) |
| 2B1, 2B2, 2B3, 2B4 | 9, 7, 5, 3 | data input/output (B port) |
| GND | 10 | ground (0 V) |
| 2A1, 2A2, 2A3, 2A4 | 11, 13, 15, 17 | data input/output (A port) |
| 1B1, 1B2, 1B3, 1B4 | 18, 16, 14, 12 | data input/output (B port) |
| V _{CC} | 20 | positive supply voltage |

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

| Input | Input/output |
|-------|--------------|
| nOE | nAn, nBn |
| L | nAn = nBn |
| H | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|--|------|-----------------------|------|
| V _{CC} | supply voltage | | -0.5 | +4.6 | V |
| V _I | input voltage | [1] | -0.5 | +4.6 | V |
| V _{SW} | switch voltage | enable and disable mode [1] | -0.5 | V _{CC} + 0.5 | V |
| I _{IK} | input clamping current | V _I < -0.5 V | -50 | - | mA |
| I _{SK} | switch clamping current | V _I < -0.5 V | -50 | - | mA |
| I _{SW} | switch current | V _{SW} = 0 V to V _{CC} | - | ±128 | mA |
| I _{CC} | supply current | | - | +100 | mA |
| I _{GND} | ground current | | -100 | - | mA |
| T _{stg} | storage temperature | | -65 | +150 | °C |
| P _{tot} | total power dissipation | T _{amb} = -40 °C to +125 °C [2] | - | 500 | mW |

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT360-1 (TSSOP20) package: P_{tot} derates linearly with 10.0 mW/K above 100 °C.
For SOT764-1 (DHVQFN20) package: P_{tot} derates linearly with 12.9 mW/K above 111 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------------------|--------------------------------------|-----|-----------------|------|
| V _{CC} | supply voltage | | 2.3 | 3.6 | V |
| V _I | input voltage | | 0 | 3.6 | V |
| V _{SW} | switch voltage | enable and disable mode | 0 | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.3 V to 3.6 V [1] | - | 200 | ns/V |

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

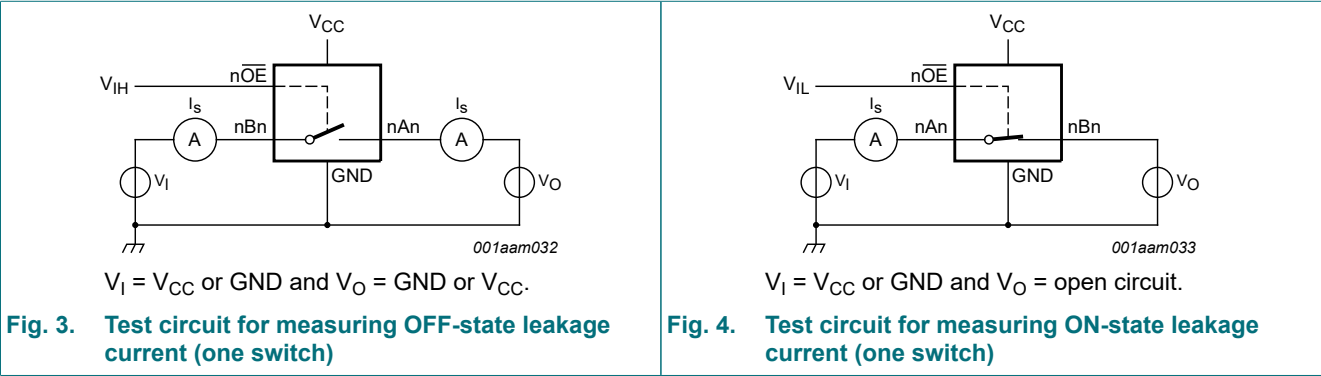
At recommended operating conditions voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|---------------------|---------------------------|---|------------------|---------|-----|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.3 V to 2.7 V | 1.7 | - | - | 1.7 | - | V |
| | | V _{CC} = 3.0 V to 3.6 V | 2.0 | - | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.3 V to 2.7 V | - | - | 0.7 | - | 0.7 | V |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 0.9 | - | 0.9 | V |
| I _I | input leakage current | pin n $\overline{\text{OE}}$; V _I = GND to V _{CC} ; V _{CC} = 3.6 V | - | - | ±1 | - | ±20 | μA |
| I _{S(OFF)} | OFF-state leakage current | V _{CC} = 3.6 V; see Fig. 3 | - | - | ±1 | - | ±20 | μA |
| I _{S(ON)} | ON-state leakage current | V _{CC} = 3.6 V; see Fig. 4 | - | - | ±1 | - | ±20 | μA |
| I _{OFF} | power-off leakage current | V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V | - | - | ±10 | - | ±50 | μA |
| I _{CC} | supply current | V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V | - | - | 10 | - | 50 | μA |
| ΔI _{CC} | additional supply current | pin n $\overline{\text{OE}}$; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V [2] | - | - | 300 | - | 2000 | μA |
| C _I | input capacitance | pin n $\overline{\text{OE}}$; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 0.9 | - | - | - | pF |
| C _{S(OFF)} | OFF-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 5.2 | - | - | - | pF |
| C _{S(ON)} | ON-state capacitance | V _{CC} = 3.3 V; V _I = 0 V to 3.3 V | - | 14.3 | - | - | - | pF |

[1] All typical values are measured at T_{amb} = 25 °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits



9.2. ON resistance

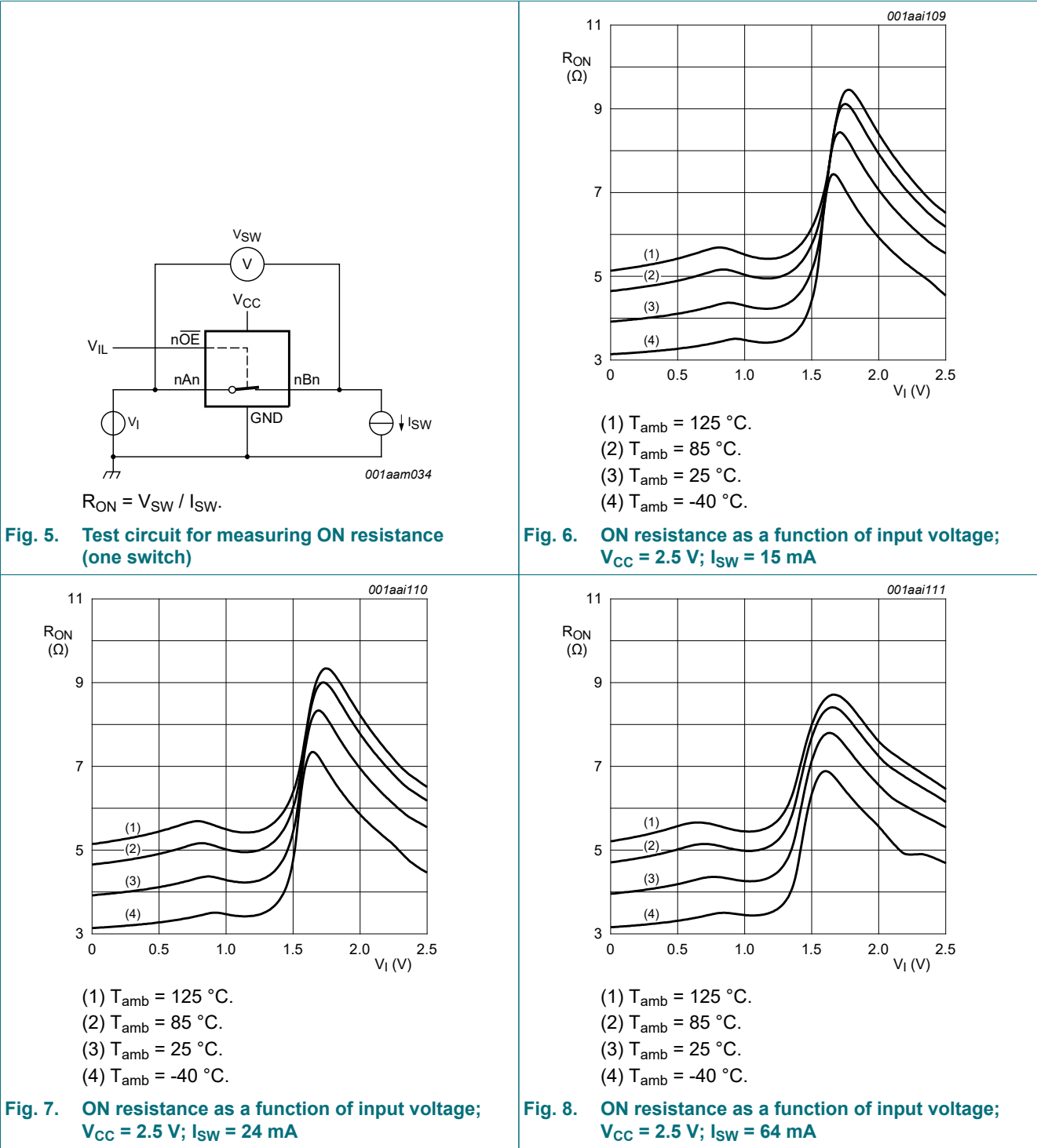
Table 7. Resistance R_{ON}
At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 5.

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|----------|---------------|---|------------------|---------|-----|-------------------|------|----------|
| | | | Min | Typ [1] | Max | Min | Max | |
| R_{ON} | ON resistance | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$; see Fig. 6 to Fig. 8. [2] | | | | | | |
| | | $I_{SW} = 64\text{ mA}$; $V_I = 0\text{ V}$ | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | $I_{SW} = 24\text{ mA}$; $V_I = 0\text{ V}$ | - | 4.2 | 8.0 | - | 15.0 | Ω |
| | | $I_{SW} = 15\text{ mA}$; $V_I = 1.7\text{ V}$ | - | 8.4 | 40 | - | 60.0 | Ω |
| | | $V_{CC} = 3.0\text{ V to }3.6\text{ V}$; see Fig. 9 to Fig. 11. | | | | | | |
| | | $I_{SW} = 64\text{ mA}$; $V_I = 0\text{ V}$ | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | $I_{SW} = 24\text{ mA}$; $V_I = 0\text{ V}$ | - | 4.0 | 7.0 | - | 11.0 | Ω |
| | | $I_{SW} = 15\text{ mA}$; $V_I = 2.4\text{ V}$ | - | 6.2 | 15 | - | 25.5 | Ω |

[1] Typical values are measured at $T_{amb} = 25\text{ °C}$ and nominal V_{CC} .

[2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs



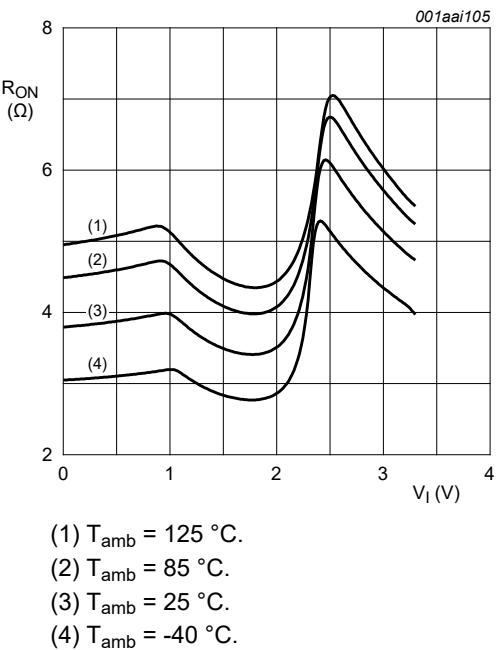


Fig. 9. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 15\text{ mA}$

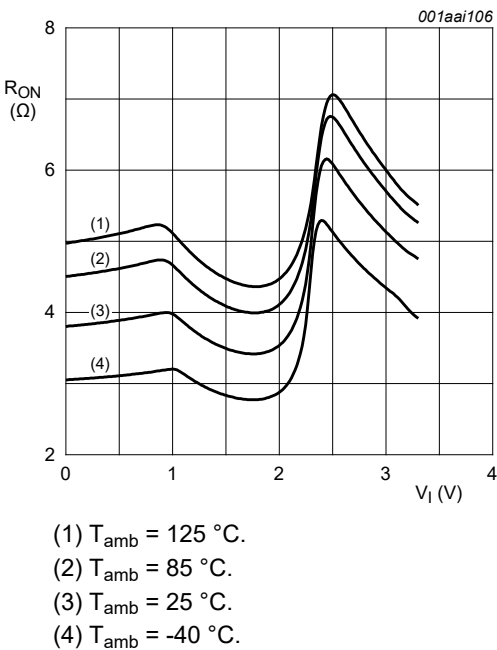


Fig. 10. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 24\text{ mA}$

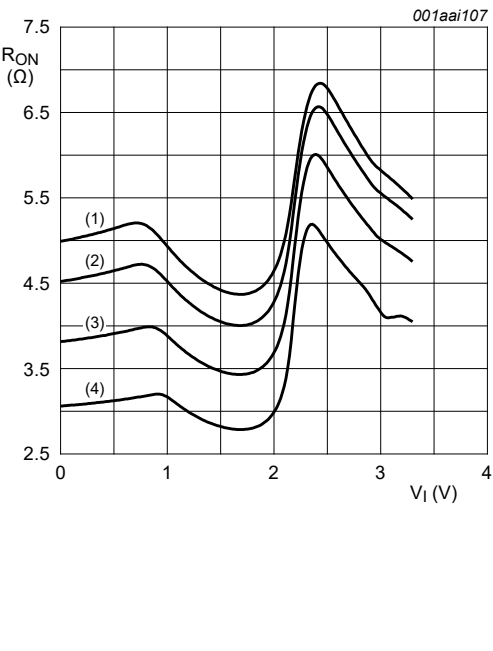


Fig. 11. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

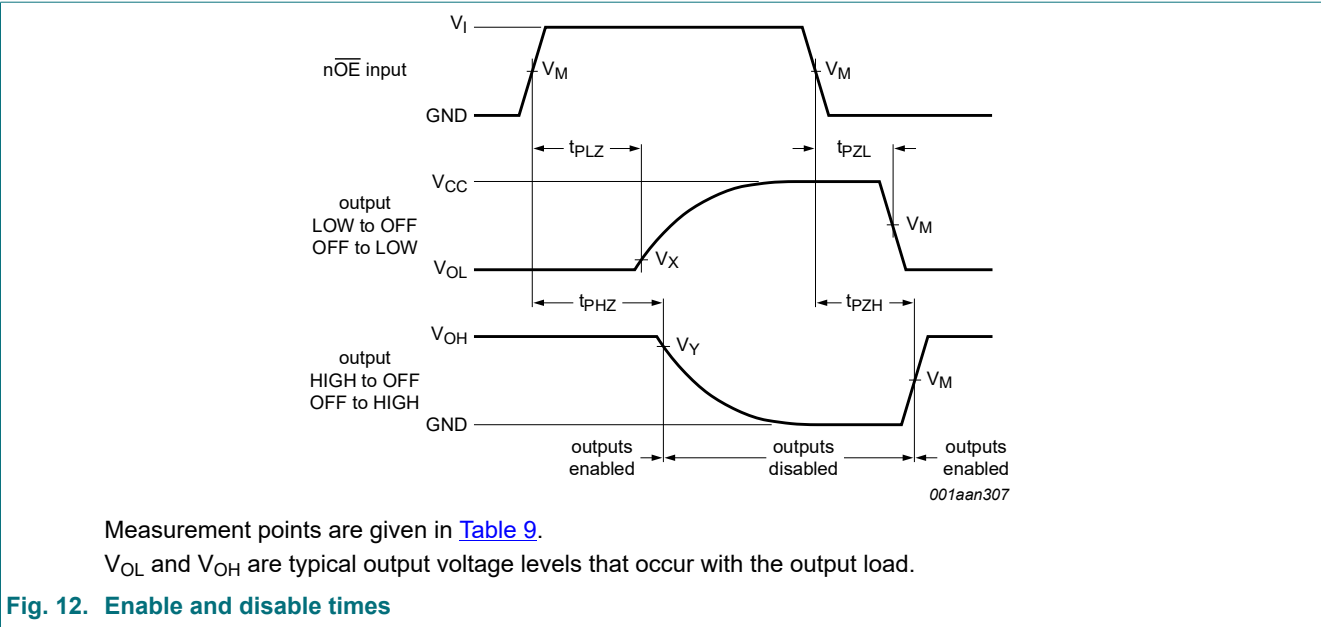
10. Dynamic characteristics

Table 8. Dynamic characteristics
GND = 0 V; for test circuit see Fig. 14

| Symbol | Parameter | Conditions | -40 °C to +85 °C | | | -40 °C to +125 °C | | Unit |
|------------------|-------------------|---|------------------|---------|------|-------------------|------|------|
| | | | Min | Typ [1] | Max | Min | Max | |
| t _{pd} | propagation delay | nAn to nBn or nBn to nAn; see Fig. 13 [2] [3] | | | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | - | - | 0.13 | - | 0.20 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | - | - | 0.20 | - | 0.31 | ns |
| t _{en} | enable time | nOE to nAn or nBn; see Fig. 12 [4] | | | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 3.0 | 5.0 | 1.0 | 7.0 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 2.6 | 4.3 | 1.0 | 6.0 | ns |
| t _{dis} | disable time | nOE to nAn or nBn; see Fig. 12 [5] | | | | | | |
| | | V _{CC} = 2.3 V to 2.7 V | 1.0 | 2.6 | 5.5 | 1.0 | 7.5 | ns |
| | | V _{CC} = 3.0 V to 3.6 V | 1.0 | 3.2 | 5.5 | 1.0 | 7.5 | ns |

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
[2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
[3] t_{pd} is the same as t_{PLH} and t_{PHL}.
[4] t_{en} is the same as t_{PZH} and t_{PZL}.
[5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1. Waveforms and test circuit



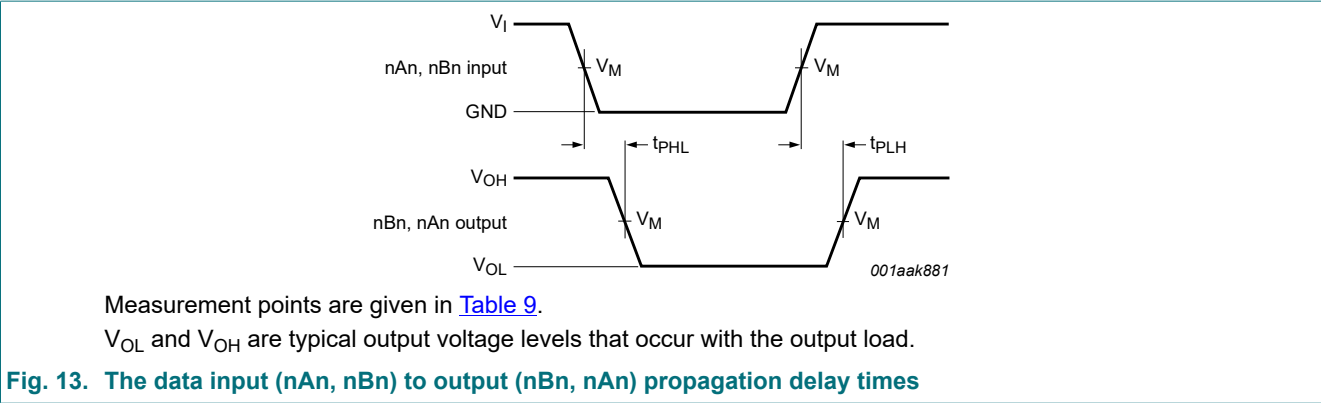


Table 9. Measurement points

| Supply voltage | Input | | | Output | | |
|----------------|---------------------|----------|---------------|---------------------|-------------------|-------------------|
| V_{CC} | V_M | V_I | $t_r = t_f$ | V_M | V_X | V_Y |
| 2.3 V to 2.7 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.0 ns | $0.5 \times V_{CC}$ | $V_{OL} + 0.15$ V | $V_{OH} - 0.15$ V |
| 3.0 V to 3.6 V | $0.5 \times V_{CC}$ | V_{CC} | ≤ 2.0 ns | $0.5 \times V_{CC}$ | $V_{OL} + 0.3$ V | $V_{OH} - 0.3$ V |

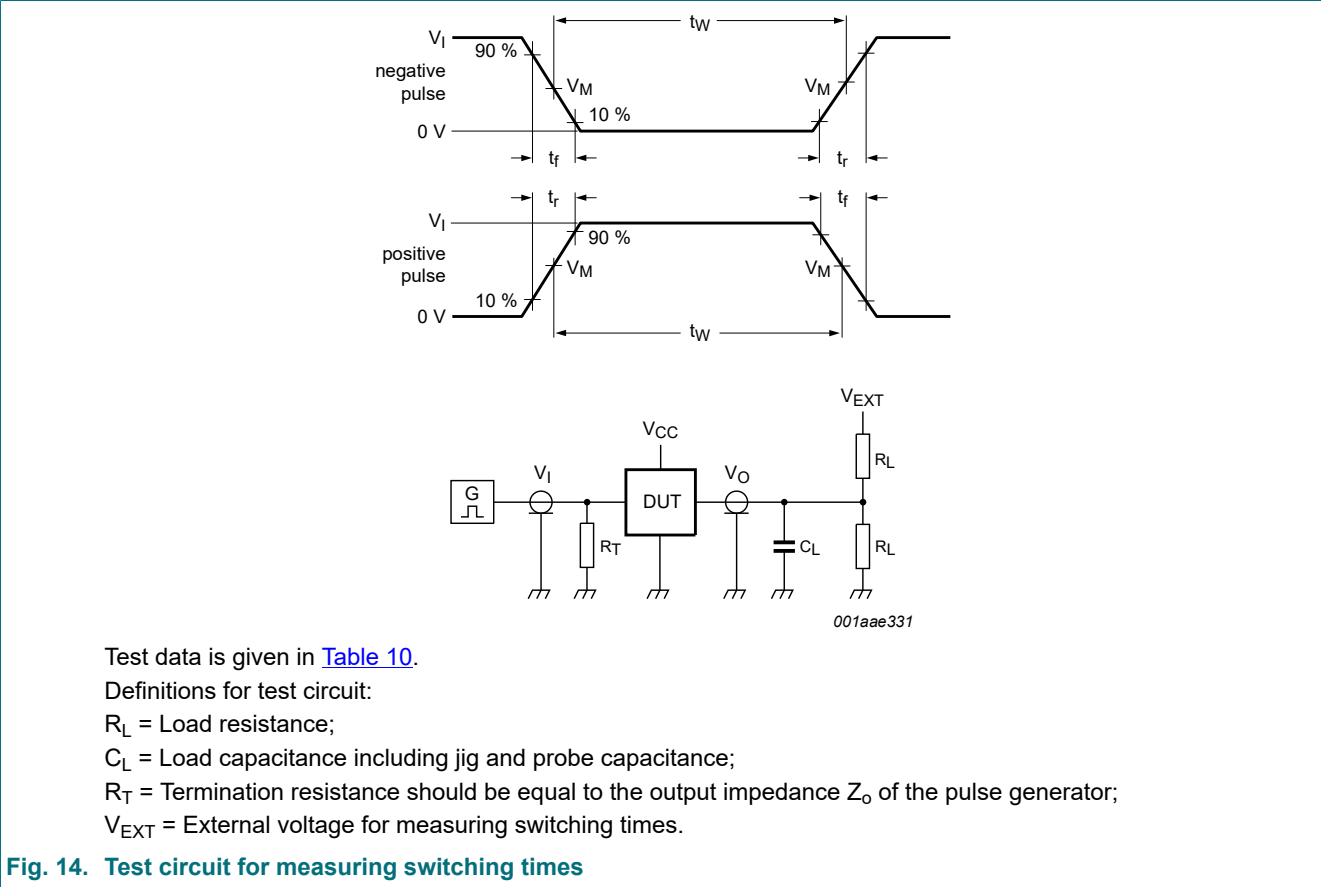


Table 10. Test data

| Supply voltage | Load | | V_{EXT} | | |
|----------------|-------|--------------|--------------------|--------------------|--------------------|
| V_{CC} | C_L | R_L | t_{PLH}, t_{PHL} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 2.3 V to 2.7 V | 30 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |
| 3.0 V to 3.6 V | 50 pF | 500 Ω | open | GND | $2 \times V_{CC}$ |

10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND or } V_{CC}$; $t_r = t_f \leq 2.5 \text{ ns}$.

| Symbol | Parameter | Conditions | T _{amb} = 25 °C | | | Unit |
|---------------------|--------------------------|---|--------------------------|-----|-----|------|
| | | | Min | Typ | Max | |
| f _(-3dB) | -3 dB frequency response | V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 15 [1] | - | 406 | - | MHz |

[1] f_i is biased at 0.5V_{CC}.

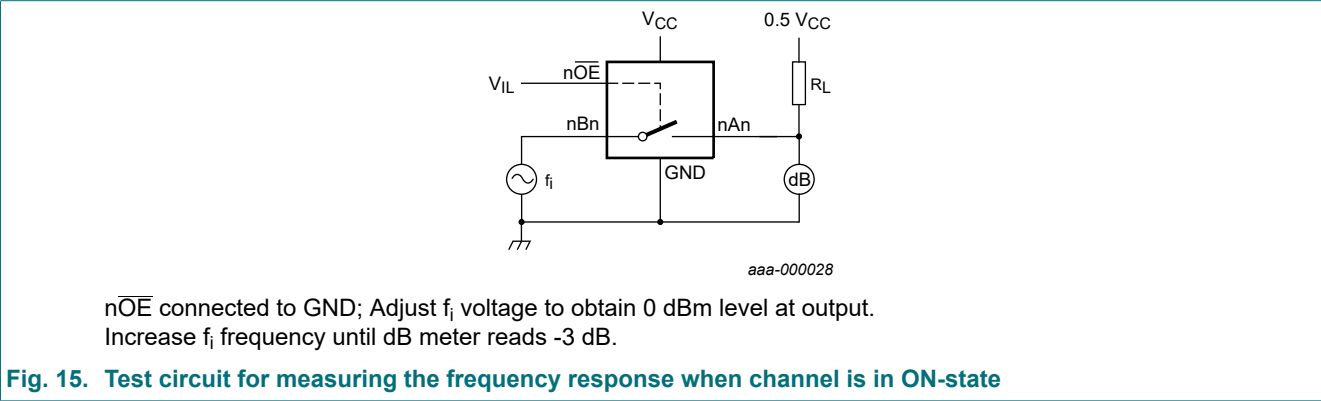


Fig. 15. Test circuit for measuring the frequency response when channel is in ON-state

11. Package outline

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

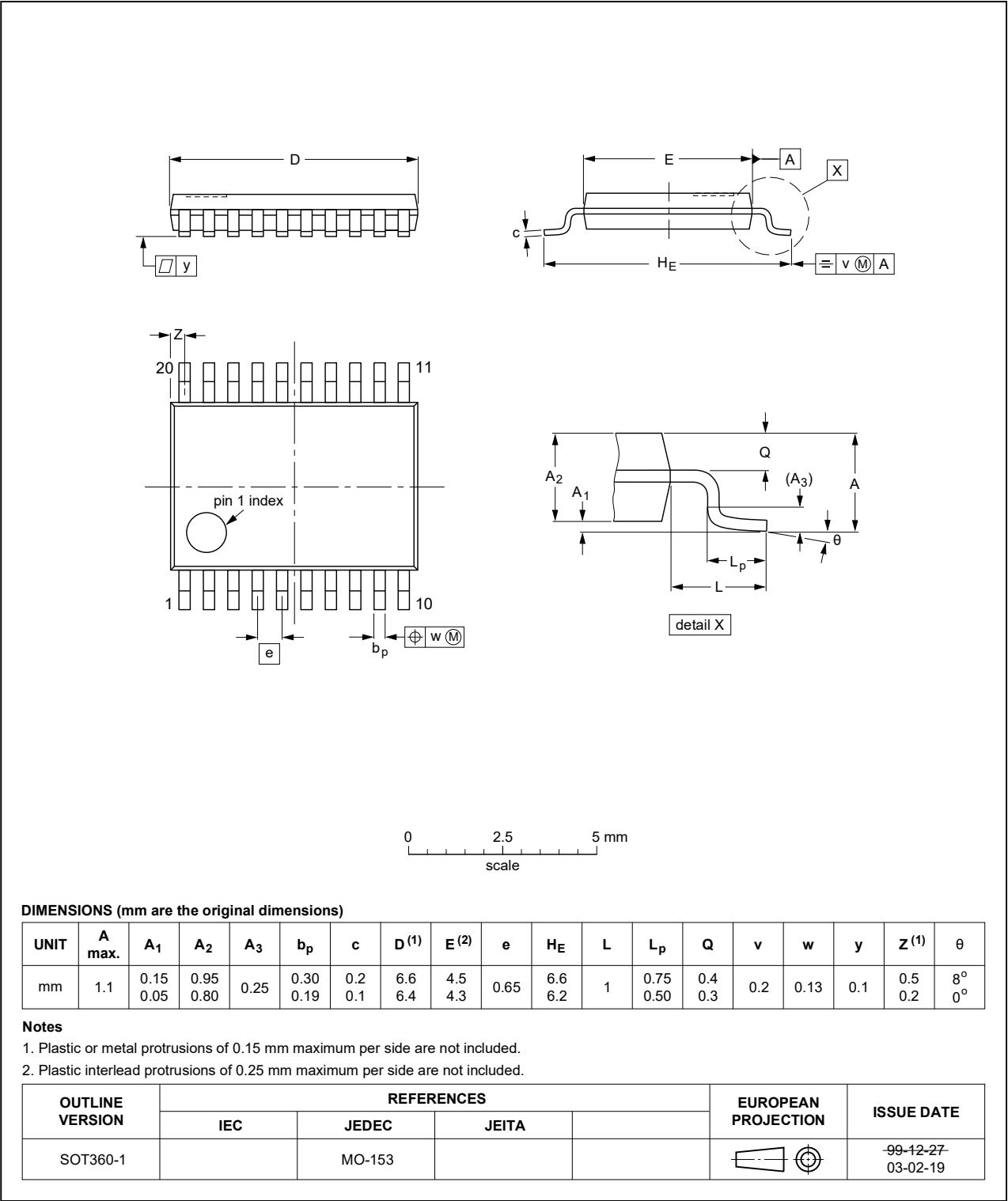


Fig. 16. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

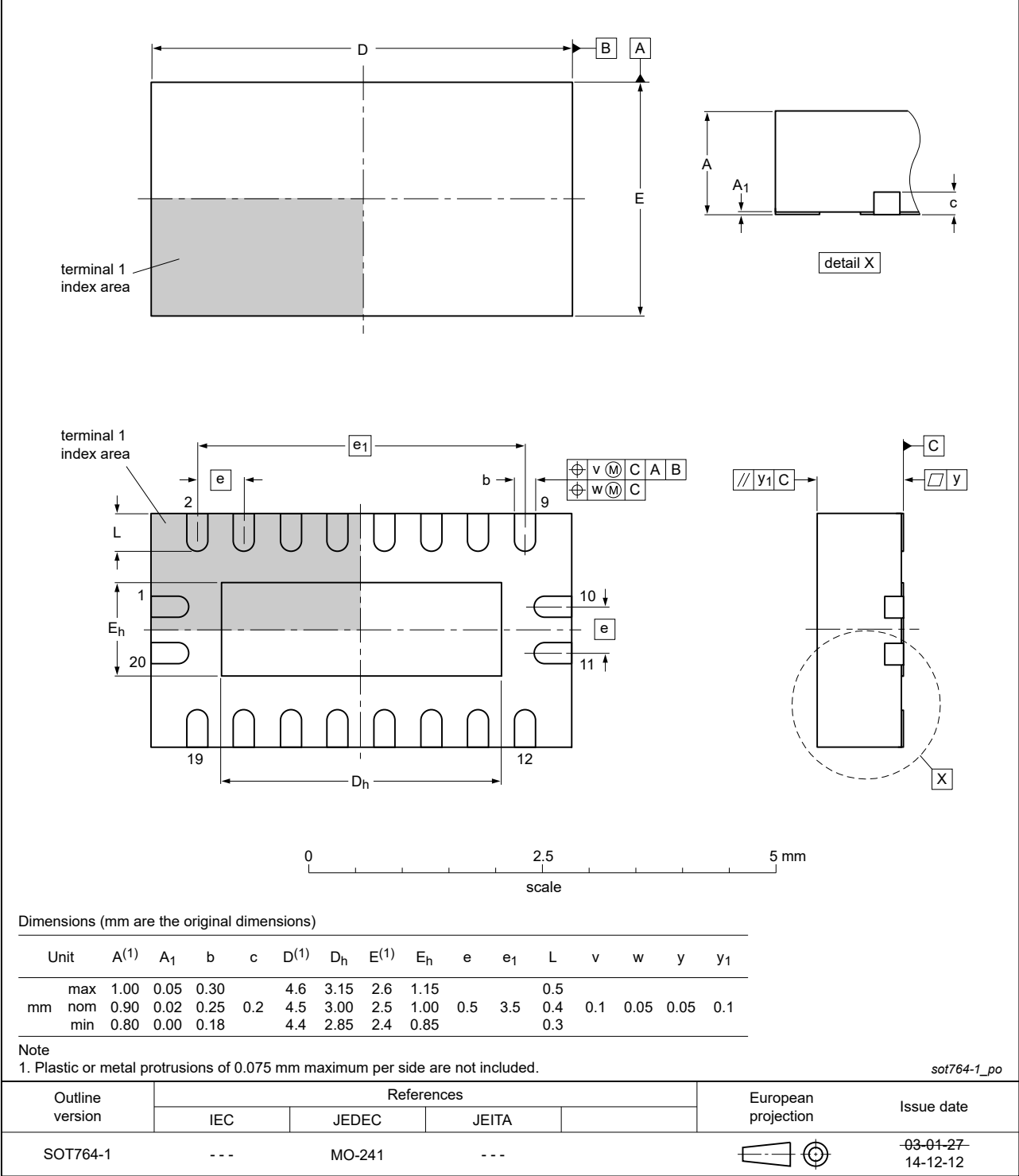


Fig. 17. Package outline SOT764-1 (DHVQFN20)

12. Abbreviations

Table 12. Abbreviations

| Acronym | Description |
|---------|---|
| ANSI | American National Standards Institute |
| CDM | Charged Device Model |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| ESDA | ElectroStatic Discharge Association |
| HBM | Human Body Model |
| JEDEC | Joint Electron Device Engineering Council |

13. Revision history

Table 13. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|---|--------------------|---------------|-----------------|
| 74CBTLV3244 v.6 | 20240624 | Product data sheet | - | 74CBTLV3244 v.5 |
| Modifications: | <ul style="list-style-type: none">Section 2: ESD specification updated according to the latest JEDEC standard. | | | |
| 74CBTLV3244 v.5 | 20221213 | Product data sheet | - | 74CBTLV3244 v.4 |
| Modifications: | <ul style="list-style-type: none">Errata in Section 5.1 corrected.Table 4: Derating values for P_{tot} total power dissipation updated. | | | |
| 74CBTLV3244 v.4 | 20190408 | Product data sheet | - | 74CBTLV3244 v.3 |
| Modifications: | <ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Type number 74CBTLV3244DS (SOT724-1) removed.Typo corrected in Table 2. | | | |
| 74CBTLV3244 v.3 | 20161108 | Product data sheet | - | 74CBTLV3244 v.2 |
| Modifications: | <ul style="list-style-type: none">Section 10.2 added. | | | |
| 74CBTLV3244 v.2 | 20111215 | Product data sheet | - | 74CBTLV3244 v.1 |
| Modifications: | <ul style="list-style-type: none">Legal pages updated. | | | |
| 74CBTLV3244 v.1 | 20101228 | Product data sheet | - | - |

14. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
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