50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

27 October 2022

Product data sheet

1. General description

NPN Resistor-Equipped Transistor (RET) in a leadless ultra small SOT883 (SC-101) Surface-Mounted Device (SMD) plastic package.

PNP complement: PDTA124EM

2. Features and benefits

- · 100 mA output current capability
- · Built-in bias resistors
- · Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

3. Applications

- · Digital application in automotive and industrial segments
- · Cost-saving alternative for BC847 series in digital applications
- · Controlling IC inputs
- · Switching loads

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{CEO}	collector-emitter voltage	open base		-	-	50	V
Io	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	

[1] See "Section 11: Test information" for resistor calculation and test conditions.



50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	I	input (base)	3	
2	GND	ground (emitter)		
3	0	output (collector)	Transparent top view DFN1006-3 (SOT883)	GND————————————————————————————————————

6. Ordering information

Table 3. Ordering information

Type number	Type number Package					
	Name	Description	Version			
PDTC124EM		plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	<u>SOT883</u>			

7. Marking

Table 4. Marking codes

Type number	Marking code
PDTC124EM	DX

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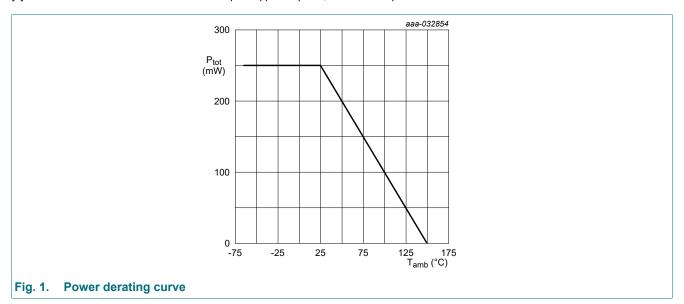
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{CBO}	collector-base voltage	open emitter		-	50	V
V _{CEO}	collector-emitter voltage	open base		-	50	V
V _{EBO}	emitter-base voltage	open collector		-	10	V
VI	input voltage	positive		-	40	V
		negative		-	-10	V
Io	output current			-	100	mA
P _{tot}	total power dissipation	T _{amb} ≤ 25 °C	[1] [2]	-	250	mW
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C

- [1] Reflow soldering is the only recommended soldering method.
- [2] Device mounted on an FR4 PCB with 70 µm copper strip line, standard footprint.



50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
R _{th(j-a)}	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	500	K/W

- Reflow soldering is the only recommended soldering method.
- Device mounted on an FR4 PCB with 70 µm copper strip line, standard footprint.

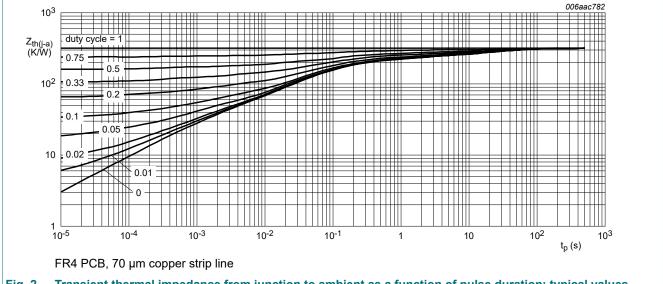


Fig. 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

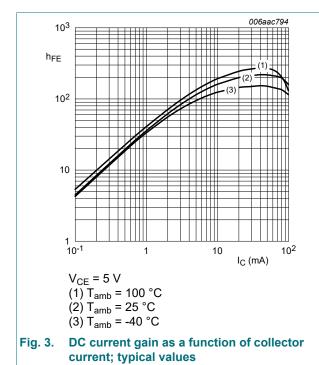
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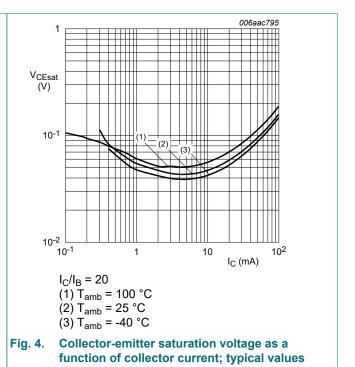
10. Characteristics

Table 7. Characteristics

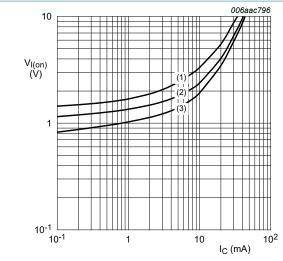
Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{(BR)CBO}	collector-base breakdown voltage	$I_C = 100 \ \mu A; I_E = 0 \ A; T_{amb} = 25 \ ^{\circ}C$		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	$I_C = 2 \text{ mA}; I_B = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		50	-	-	V
I _{CBO}	collector-base cut-off current	V _{CB} = 50 V; I _E = 0 A; T _{amb} = 25 °C		-	-	100	nA
I _{CEO}	collector-emitter cut-off	V _{CE} = 30 V; I _B = 0 A; T _{amb} = 25 °C		-	-	100	nA
	current	V _{CE} = 30 V; I _B = 0 A; T _j = 150 °C		-	-	5	μΑ
I _{EBO}	emitter-base cut-off current	$V_{EB} = 5 \text{ V}; I_{C} = 0 \text{ A}; T_{amb} = 25 \text{ °C}$		-	-	180	μA
h _{FE}	DC current gain	V _{CE} = 5 V; I _C = 5 mA; T _{amb} = 25 °C		60	-	-	
V _{CEsat}	collector-emitter saturation voltage	$I_C = 10 \text{ mA}; I_B = 0.5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		-	-	100	mV
$V_{I(off)}$	off-state input voltage	V _{CE} = 5 V; I _C = 100 μA; T _{amb} = 25 °C		-	1.1	0.8	V
V _{I(on)}	on-state input voltage	$V_{CE} = 0.3 \text{ V}; I_{C} = 5 \text{ mA}; T_{amb} = 25 ^{\circ}\text{C}$		2.5	1.7	-	V
R1	bias resistor 1 (input)		[1]	15.4	22	28.6	kΩ
R2/R1	bias resistor ratio		[1]	0.8	1	1.2	
C _c	collector capacitance	$V_{CB} = 10 \text{ V}; I_E = 0 \text{ A}; i_e = 0 \text{ A}; f = 1 \text{ MHz}; $ $T_{amb} = 25 ^{\circ}\text{C}$		-	-	2.5	pF
f _T	transition frequency	V_{CE} = 5 V; I_{C} = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz

- [1] See "Section 11: Test information" for resistor calculation and test conditions.
- [2] Characteristics of built-in transistor.





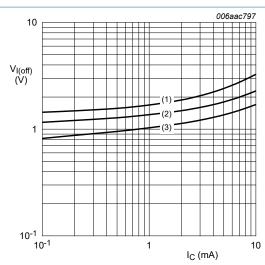
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 $V_{CE} = 0.3 V$

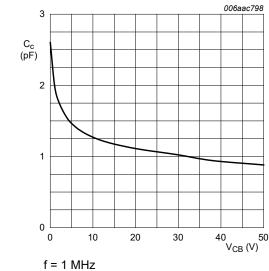
(1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C





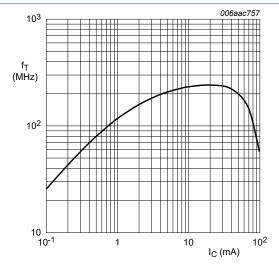
V_{CE} = 5 V (1) T_{amb} = -40 °C (2) T_{amb} = 25 °C (3) T_{amb} = 100 °C

Off-state input voltage as a function of collector current; typical values



 T_{amb} = 25 °C

Fig. 7. Collector capacitance as a function of collectorbase voltage; typical values



f = 100 MHz

 $T_{amb} = 25 \, ^{\circ}C$ $V_{CE} = 5 V$

Transition frequency as a function of collector Fig. 8. current; typical values of built-in transistor

50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - Stress test qualification for discrete semiconductors, and is suitable for use in automotive applications.

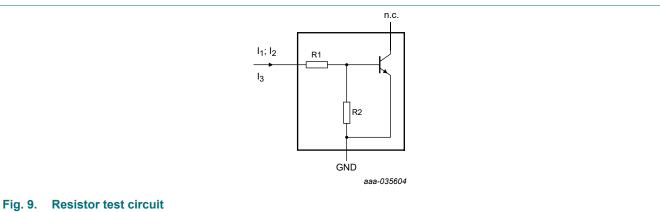
Resistor calculation

Calculation of bias resistor 1 (R1)

$$R_{I} = \frac{V(I_{2}) - V(I_{1})}{I_{2} - I_{1}}$$

· Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I3)}{R1 \cdot I3} - 1$$



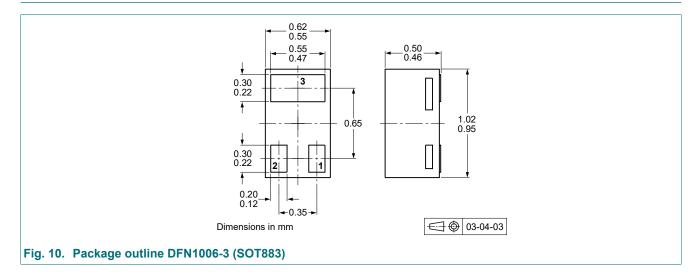
Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions		
			I ₁	l ₂	l ₃
PDTC124EM	22	22	160 μΑ	210 μΑ	-182 µA

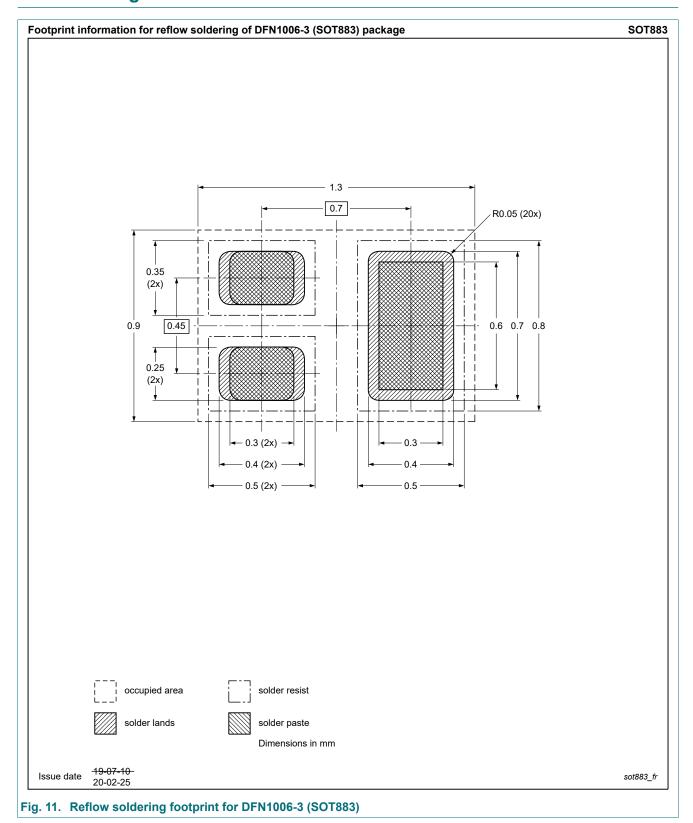
50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

12. Package outline



50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

13. Soldering



50 V, 100 mA NPN resistor-equipped transistor; R1 = 22 k Ω , R2 = 22 k Ω

14. Revision history

Table 9. Revision history

	1		1		
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes	
PDTC124EM v.9	20221027	Product data sheet	-	PDTC124E_SER v.8	
Modification:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Family data sheet reduced to single type data sheet. Packing information removed. 				
PDTC124E_SER v.8	20111128	Product data sheet	-	PDTC124E_SERIES v.7	
PDTC124E_SERIES v.7	20040817	Product data sheet	-	PDTC124E_SERIES v.6	
PDTC124E_SERIES v.6	20030414	Product specification	-	-	

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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PDTC124EM

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