74HC154; 74HCT154

4-to-16 line decoder/demultiplexer

Rev. 10 — 5 August 2024 Product data sheet

1. General description

The 74HC154; 74HCT154 is a 4-to-16 line decoder/demultiplexer. It decodes four binary weighted address inputs (A0 to A3) to sixteen mutually exclusive outputs ($\overline{Y0}$ to $\overline{Y15}$). The device features two input enable ($\overline{E0}$ and $\overline{E1}$) inputs. A HIGH on either of the input enables forces the outputs HIGH. The device can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input. When the other enable input is LOW the addressed output will follow the state of the applied data. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}.

2. Features and benefits

- Wide supply voltage range from 2.0 V to 6.0 V
- CMOS low power dissipation
- High noise immunity
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into 16 mutually-exclusive outputs
- Input levels:
  - For 74HC154: CMOS level
  - For 74HCT154: TTL level
- Complies with JEDEC standards:
  - JESD8C (2.7 V to 3.6 V)
  - JESD7A (2.0 V to 6.0 V)
- ESD protection:
  - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
  - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC154D 74HCT154D	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74HC154PW 74HCT154PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74HC154BQ 74HCT154BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram

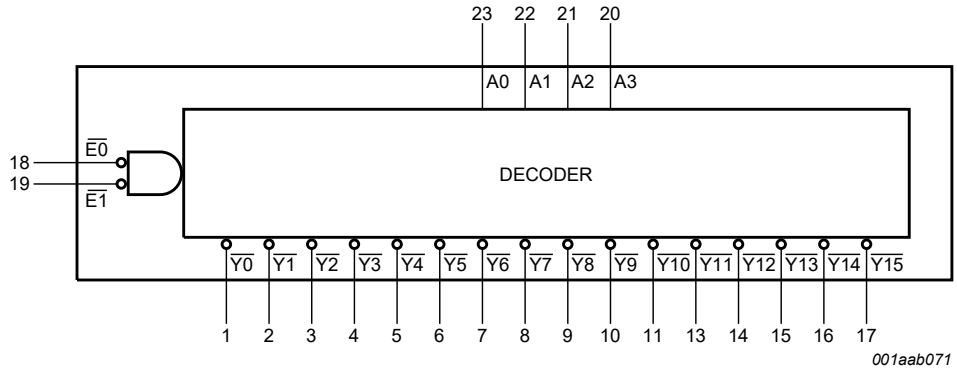


Fig. 1. Functional diagram

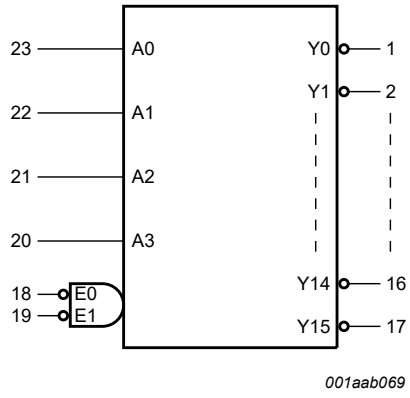


Fig. 2. Logic symbol

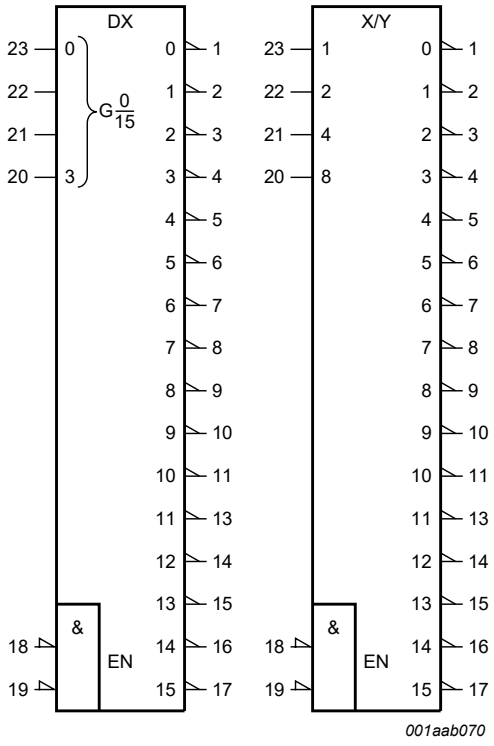


Fig. 3. IEC logic symbol

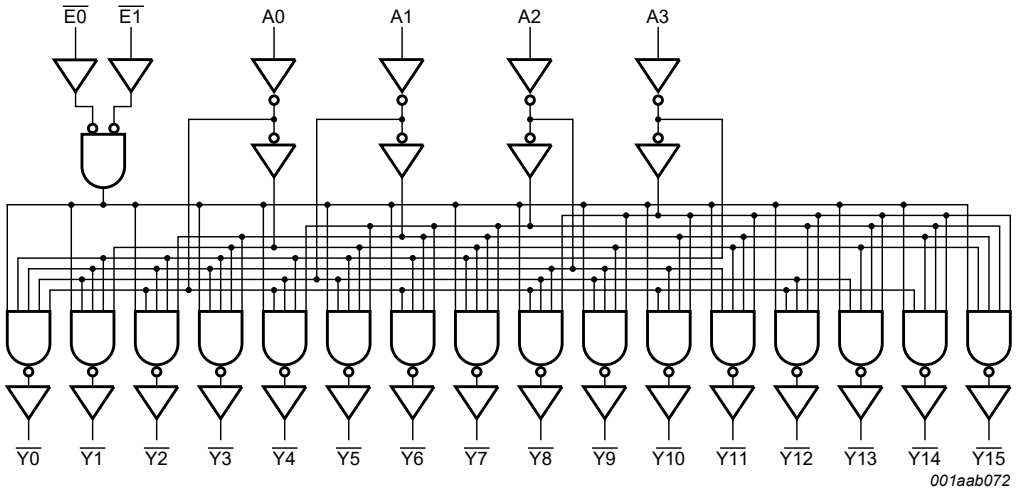
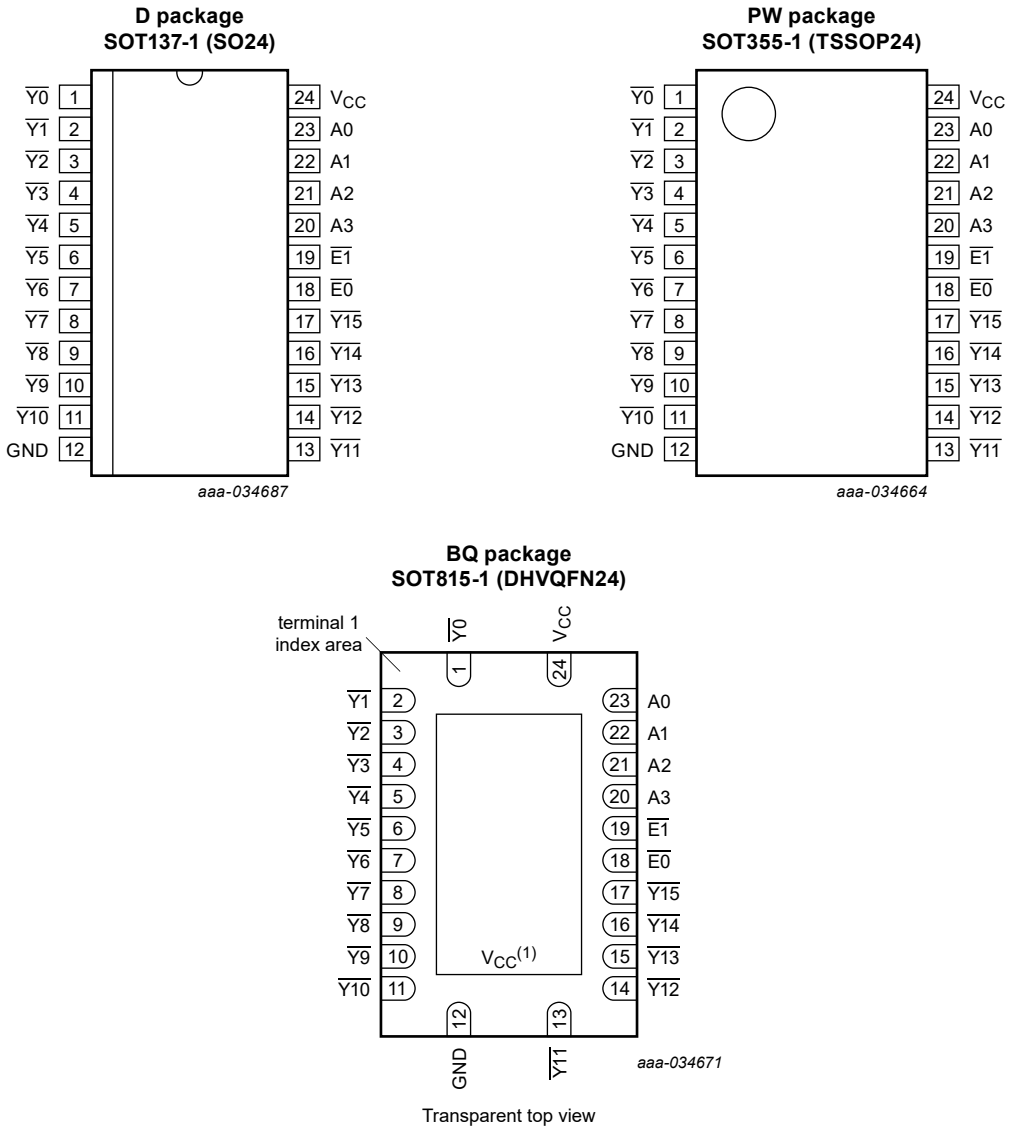


Fig. 4. Logic diagram

5. Pinning information

5.1. Pinning



(1) This is not a V_{CC} pin. There is no electrical or mechanical requirement to solder the pad. In case soldered, the solder land should remain floating or connected to V_{CC}.

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{Y0}$, $\overline{Y1}$, $\overline{Y2}$, $\overline{Y3}$, $\overline{Y4}$, $\overline{Y5}$, $\overline{Y6}$, $\overline{Y7}$, $\overline{Y8}$, $\overline{Y9}$, $\overline{Y10}$, $\overline{Y11}$, $\overline{Y12}$, $\overline{Y13}$, $\overline{Y14}$, $\overline{Y15}$	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	data output (active LOW)
GND	12	ground (0 V)
$\overline{E0}$, $\overline{E1}$	18, 19	enable input (active LOW)
A0, A1, A2, A3	23, 22, 21, 20	address input
V_{CC}	24	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care.

Input						Output															
$\overline{E0}$	$\overline{E1}$	A0	A1	A2	A3	$\overline{Y0}$	$\overline{Y1}$	$\overline{Y2}$	$\overline{Y3}$	$\overline{Y4}$	$\overline{Y5}$	$\overline{Y6}$	$\overline{Y7}$	$\overline{Y8}$	$\overline{Y9}$	$\overline{Y10}$	$\overline{Y11}$	$\overline{Y12}$	$\overline{Y13}$	$\overline{Y14}$	$\overline{Y15}$
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
		L	H	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
		H	H	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
		L	L	H	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
		H	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
		L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
		H	H	H	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
		L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
		H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
		L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
		H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
		L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
		H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
		L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
		H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			-0.5	+7.0	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V	[1]	-	±25	mA
I_{CC}	supply current		[1]	-	50	mA
I_{GND}	ground current		[1]	-	-50	mA
T_{stg}	storage temperature			-65	+150	°C
P_{tot}	total power dissipation	T_{amb} = -40 °C to +125 °C	[2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT137-1 (SO24) package: P_{tot} derates linearly with 16.2 mW/K above 119 °C.
For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC154			74HCT154			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V_{CC} = 2.0 V	-	-	625	-	-	-	ns/V
		V_{CC} = 4.5 V	-	1.67	139	-	1.67	139	ns/V
		V_{CC} = 6.0 V	-	-	83	-	-	-	ns/V

9. Static characteristics

Table 6. Static characteristics 74HC154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	1.2	-	V
		V_{CC} = 4.5 V	3.15	2.4	-	V
		V_{CC} = 6.0 V	4.2	3.2	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	0.8	0.5	V
		V_{CC} = 4.5 V	-	2.1	1.35	V
		V_{CC} = 6.0 V	-	2.8	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; I_O = -20 µA	1.9	2.0	-	V
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	4.5	-	V
		V_{CC} = 6.0 V; I_O = -20 µA	5.9	6.0	-	V
		V_{CC} = 4.5 V; I_O = -4.0 mA	3.98	4.32	-	V
		V_{CC} = 6.0 V; I_O = -5.2 mA	5.48	5.81	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; I_O = 20 µA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 20 µA	-	0	0.1	V
		V_{CC} = 6.0 V; I_O = 20 µA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 4.0 mA	-	0.15	0.26	V
		V_{CC} = 6.0 V; I_O = 5.2 mA	-	0.16	0.26	V
I_I	input leakage current	V_{CC} = 6.0 V; V_I = V_{CC} or GND	-	-	±0.1	µA
I_{CC}	supply current	V_{CC} = 6.0 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	8.0	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 2.0 V; I_O = -20 µA	1.9	-	-	V
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	-	-	V
		V_{CC} = 6.0 V; I_O = -20 µA	5.9	-	-	V
		V_{CC} = 4.5 V; I_O = -4.0 mA	3.84	-	-	V
		V_{CC} = 6.0 V; I_O = -5.2 mA	5.34	-	-	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 6.0 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 4.0 mA	-	-	0.33	V
		V_{CC} = 6.0 V; I_O = 5.2 mA	-	-	0.33	V
I_I	input leakage current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND	-	-	±1.0	µA
I_{CC}	supply current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	80	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 2.0 V	1.5	-	-	V
		V_{CC} = 4.5 V	3.15	-	-	V
		V_{CC} = 6.0 V	4.2	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 2.0 V	-	-	0.5	V
		V_{CC} = 4.5 V	-	-	1.35	V
		V_{CC} = 6.0 V	-	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = -20 µA	1.9	-	-	V
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	-	-	V
		V_{CC} = 6.0 V; I_O = -20 µA	5.9	-	-	V
		V_{CC} = 4.5 V; I_O = -4.0 mA	3.7	-	-	V
		V_{CC} = 6.0 V; I_O = -5.2 mA	5.2	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		V_{CC} = 2.0 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 6.0 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 4.0 mA	-	-	0.4	V
		V_{CC} = 6.0 V; I_O = 5.2 mA	-	-	0.4	V
I_I	input leakage current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND	-	-	±0.1	µA
I_{CC}	supply current	V_{CC} = 6.0 V; $V_I = V_{CC}$ or GND; I_O = 0 A	-	-	160	µA

Table 7. Static characteristics 74HCT154

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	1.6	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	1.2	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	4.5	-	V
		V_{CC} = 4.5 V; I_O = -4 mA	3.98	4.32	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 20 µA	-	0	0.1	V
		V_{CC} = 4.5 V; I_O = 4 mA	-	0.15	0.25	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±0.1	µA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	8.0	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	360	µA
C_I	input capacitance		-	3.5	-	pF
T_{amb} = -40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	-	-	V
		V_{CC} = 4.5 V; I_O = -4 mA	3.84	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 4 mA	-	-	0.33	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±1.0	µA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	80	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	450	µA
T_{amb} = -40 °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 4.5 V to 5.5 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 4.5 V to 5.5 V	-	-	0.8	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = -20 µA	4.4	-	-	V
		V_{CC} = 4.5 V; I_O = -4 mA	3.7	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		V_{CC} = 4.5 V; I_O = 20 µA	-	-	0.1	V
		V_{CC} = 4.5 V; I_O = 4 mA	-	-	0.4	V
I_I	input leakage current	V_{CC} = 5.5 V; V_I = V_{CC} or GND	-	-	±1.0	µA
I_{CC}	supply current	V_{CC} = 5.5 V; V_I = V_{CC} or GND; I_O = 0 A	-	-	160	µA
ΔI_{CC}	additional supply current	per input pin; V_{CC} = 4.5 V to 5.5 V; V_I = V_{CC} - 2.1 V; I_O = 0 A	-	-	490	µA

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit, see Fig. 7.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC154										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Fig. 5 [1]								
		V_{CC} = 2.0 V	-	36	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	13	30	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	10	26	-	33	-	38	ns
		$\overline{En}$ to $\overline{Yn}$; see Fig. 6								
		V_{CC} = 2.0 V	-	39	150	-	190	-	225	ns
		V_{CC} = 4.5 V	-	14	30	-	38	-	45	ns
		V_{CC} = 5 V; C_L = 15 pF	-	11	-	-	-	-	-	ns
		V_{CC} = 6.0 V	-	11	26	-	33	-	38	ns
t_t	transition time	see Fig. 5 and Fig. 6 [2]								
		V_{CC} = 2.0 V	-	19	75	-	95	-	110	ns
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
		V_{CC} = 6.0 V	-	6	13	-	16	-	19	ns
C_{PD}	power dissipation capacitance	per gate; V_I = GND to V_{CC} [3]	-	60	-	-	-	-	-	pF
74HCT154										
t_{pd}	propagation delay	An to $\overline{Yn}$; see Fig. 5 [1]								
		V_{CC} = 4.5 V	-	16	35	-	44	-	53	ns
		V_{CC} = 5 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
		$\overline{En}$ to $\overline{Yn}$; see Fig. 6								
		V_{CC} = 4.5 V	-	15	32	-	40	-	48	ns
		V_{CC} = 5 V; C_L = 15 pF	-	13	-	-	-	-	-	ns
t_t	transition time	see Fig. 5 and Fig. 6 [2]								
		V_{CC} = 4.5 V	-	7	15	-	19	-	22	ns
C_{PD}	power dissipation capacitance	per gate; V_I = GND to (V_{CC} - 1.5 V) [3]	-	60	-	-	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}

[2] t_t is the same as t_{TLH} and t_{THL}

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

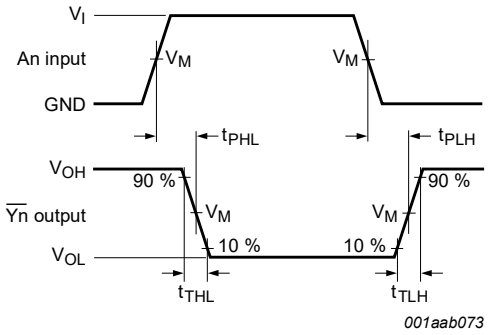
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of load switching outputs;

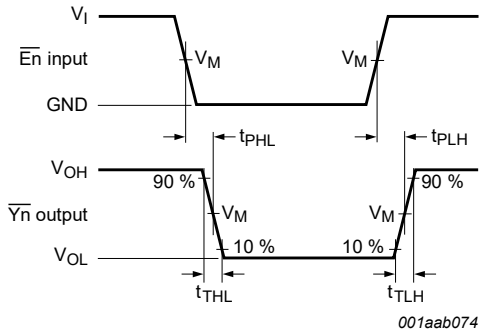
$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms and test circuit



Measurement points are given in Table 9.

Fig. 5. Propagation delay address input (An) to output (Yn) and transition time output (Yn)

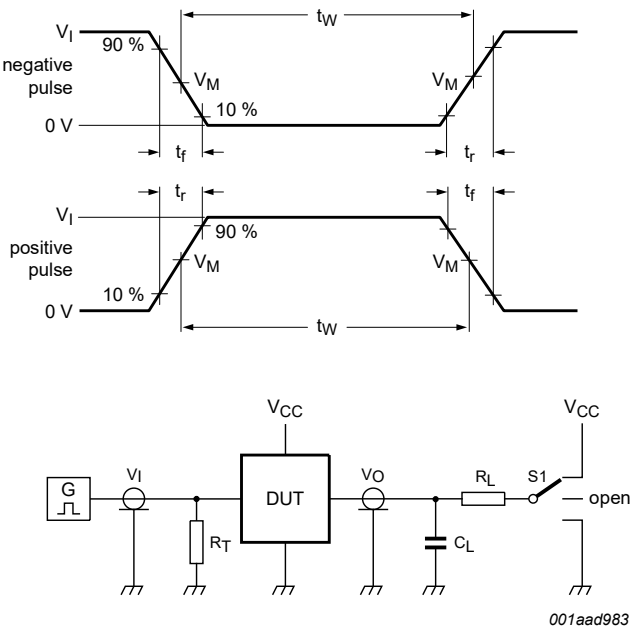


Measurement points are given in Table 9.

Fig. 6. Propagation delay enable input (En) to output (Yn) and transition time output (Yn)

Table 9. Measurement points

Type	Input	Output
	V_M	V_M
74HC154	$0.5V_{CC}$	$0.5V_{CC}$
74HCT154	1.3 V	1.3 V



Test data is given in Table 10.

Definitions test circuit:

R_T = Termination resistance; should be equal to output impedance Z_o of the pulse generator;

C_L = Load capacitance including jig and probe capacitance;

R_L = Load resistor;

S1 = Test selection switch.

Fig. 7. Test circuit for measuring switching times

Table 10. Test data

Type	Input		Load		S1 position
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}
74HC154	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open
74HCT154	3 V	6 ns	15 pF, 50 pF	1 kΩ	open

11. Application information

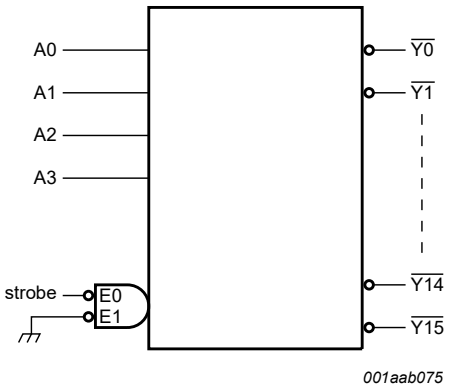


Fig. 8. 1-of-16 decoder; LOW level output selected

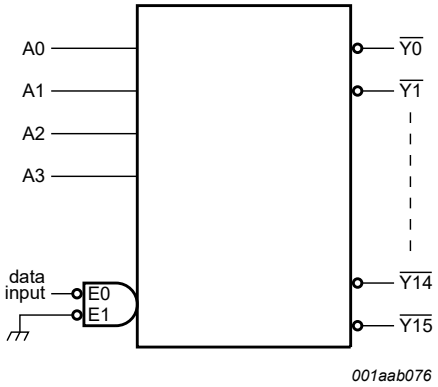
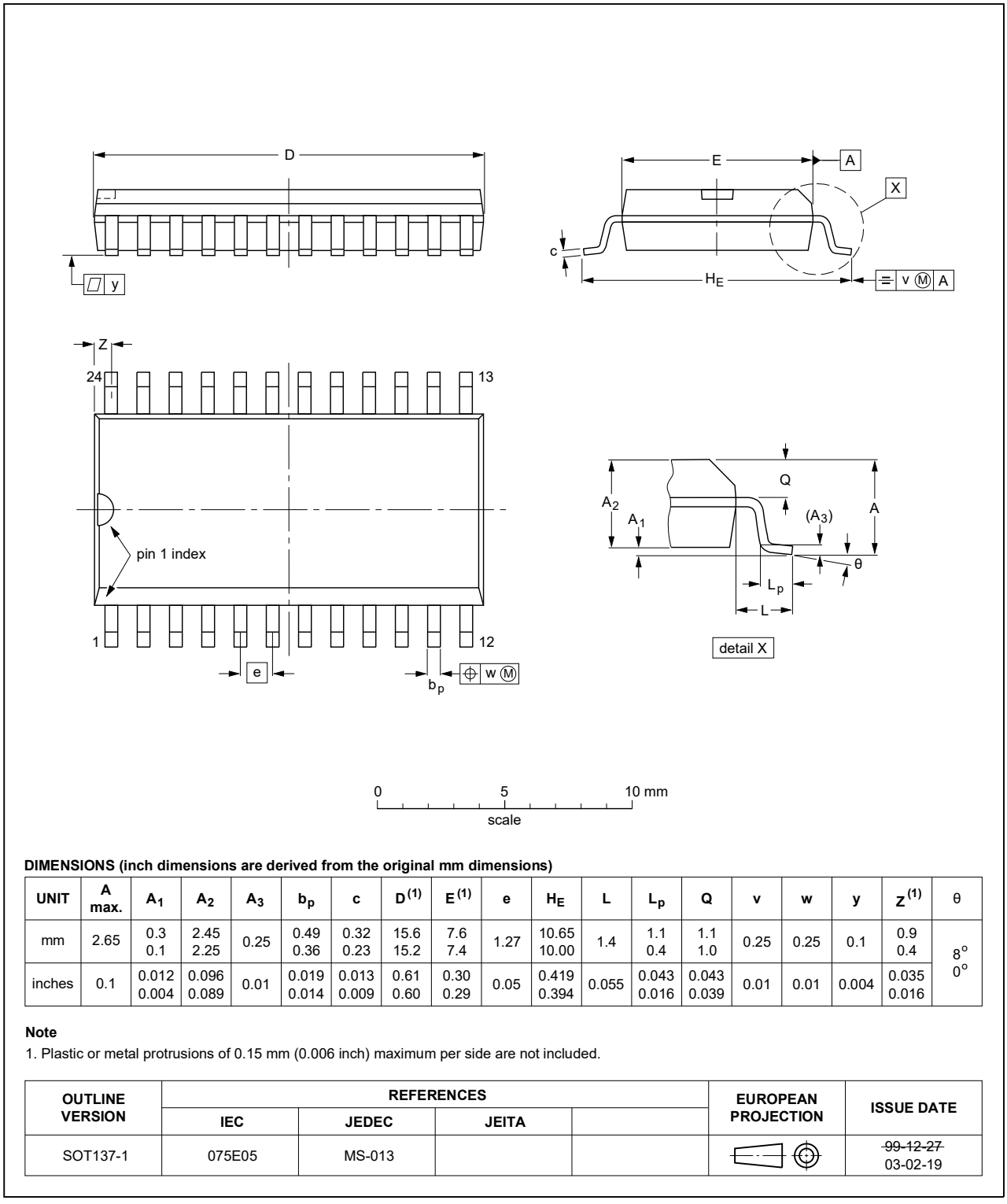


Fig. 9. 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

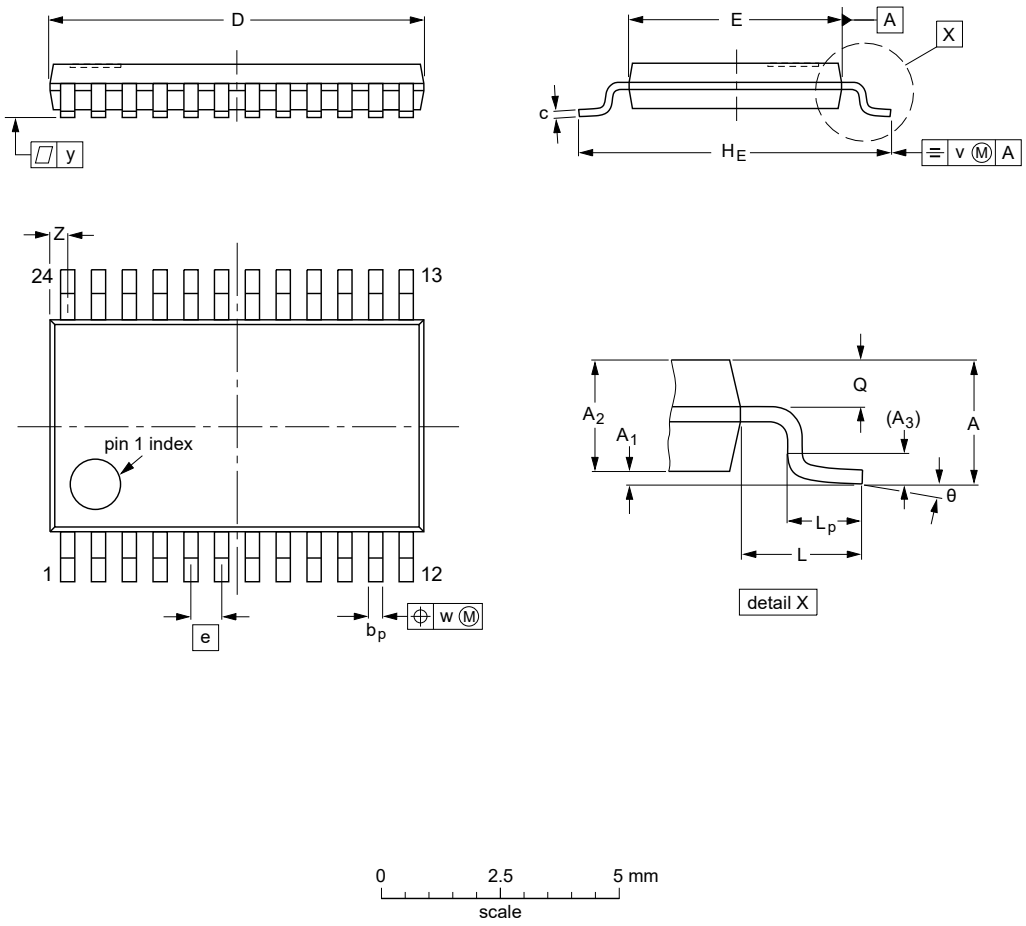
Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT137-1	075E05	MS-013				~~99-12-27~~ 03-02-19

Fig. 10. Package outline SOT137-1 (SO24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

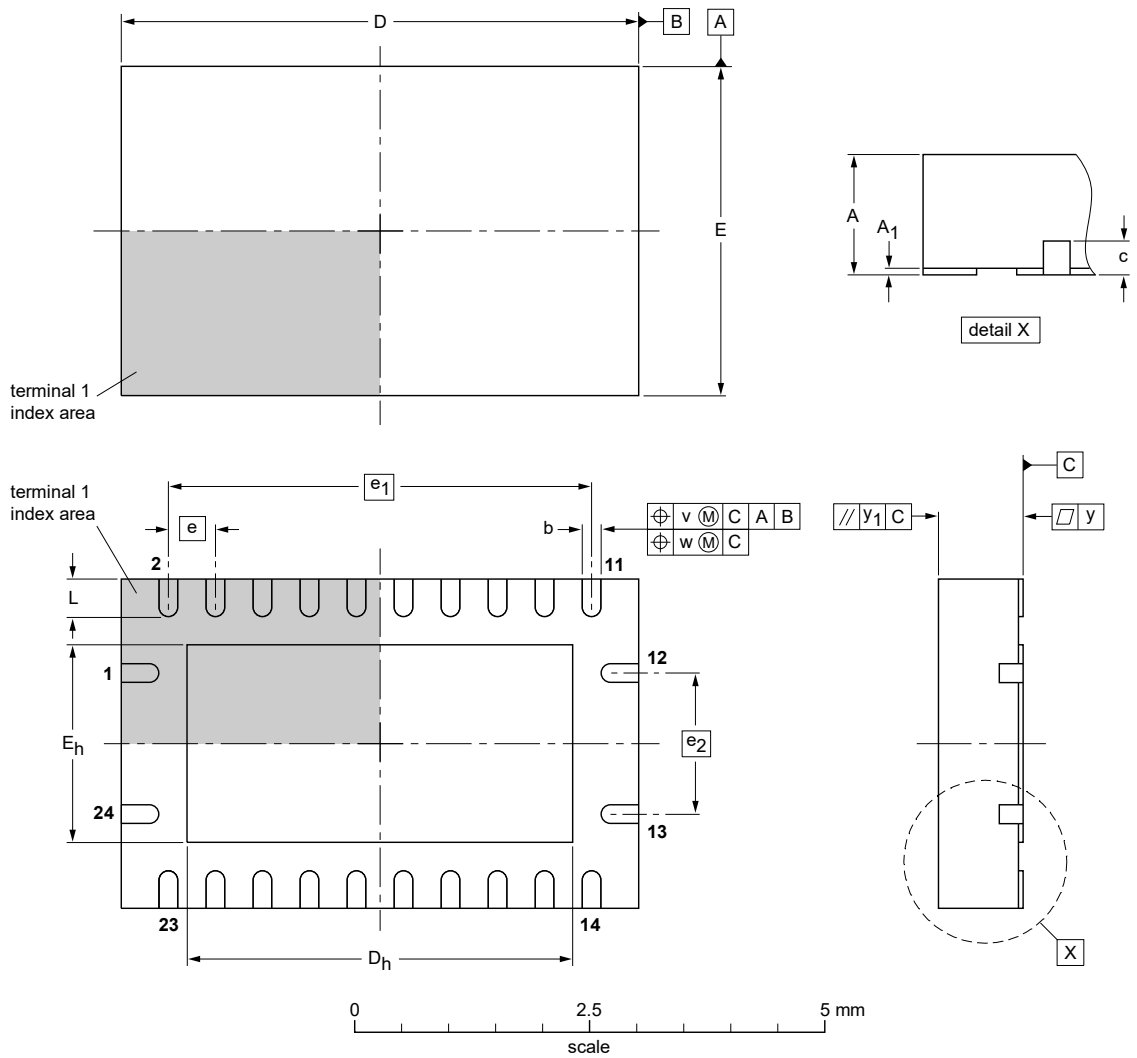
Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT355-1		MO-153				~~99-12-27~~ 03-02-19

Fig. 11. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm **SOT815-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.6 5.4	4.25 3.95	3.6 3.4	2.25 1.95	0.5	4.5	1.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT815-1	- - -	- - -	- - -			03-04-29

Fig. 12. Package outline SOT815-1 (DHVQFN24)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT154 v.10	20240805	Product data sheet	-	74HC_HCT154 v.9
Modifications:	• Section 2: ESD specification updated according to the latest JEDEC standard.			
74HC_HCT154 v.9	20210819	Product data sheet	-	74HC_HCT154 v.8
Modifications:	• Section 2 updated. • Type number 74HC154DB (SOT340-1/SSOP24) removed.			
74HC_HCT154 v.8	20210511	Product data sheet	-	74HC_HCT154 v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74HCT154DB (SOT340-1/SSOP24) removed. • Section 5.1: overline corrected (errata). • Section 7: Derating values for P_{tot} total power dissipation updated.			
74HC_HCT154 v.7	20160229	Product data sheet	-	74HC_HCT154 v.6
Modifications:	• Type numbers 74HC154N and 74HCT154N (SOT101-1) removed.			
74HC_HCT154 v.6	20070212	Product data sheet	-	74HC_HCT154 v.5
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 3: Corrected errors in output information.			
74HC_HCT154 v.5	20041012	Product specification	-	74HC_HCT154 v.4
74HC_HCT154 v.4	20041005	Product specification	-	74HC_HCT154 v.3
74HC_HCT154 v.3	20040601	Product specification	-	74HC_HCT154_CNV v.2

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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