



PSMN4R1-30YLC

N-channel 30 V 4.35mΩ logic level MOSFET in LPAK using NextPower technology

12 February 2013

Product data sheet

1. General description

Logic level enhancement mode N-channel MOSFET in LPAK package. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

2. Features and benefits

- High reliability Power SO8 package, qualified to 175°C
- Low parasitic inductance and resistance
- Optimised for 4.5V Gate drive utilising NextPower Superjunction technology
- Ultra low QG, QGD, & QOSS for high system efficiencies at low and high loads

3. Applications

- DC-to-DC converters
- Load switching
- Power OR-ing
- Server power supplies
- Sync rectifier

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	-	30	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; Fig. 1		-	-	92	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	-	67	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 20 A; T _j = 25 °C; Fig. 12		-	4.75	5.7	mΩ
		V _{GS} = 10 V; I _D = 20 A; T _j = 25 °C; Fig. 12		-	3.65	4.35	mΩ
Dynamic characteristics							
Q _{GD}	gate-drain charge	V _{GS} = 4.5 V; I _D = 20 A; V _{DS} = 15 V; Fig. 14 ; Fig. 15		-	3.5	-	nC

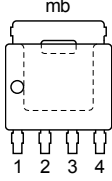
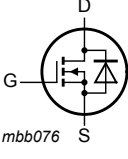
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$Q_{G(tot)}$	total gate charge	$V_{GS} = 4.5\text{ V}$; $I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 14 ; Fig. 15	-	11	-	nC

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN4R1-30YLC	LPAK; Power-SO8	plastic single-ended surface-mounted package; 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN4R1-30YLC	4C130L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-20	20	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 1	-	92	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 1	-	65	A

Symbol	Parameter	Conditions		Min	Max	Unit
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 4		-	367	A
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 2		-	67	W
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
T _{sld(M)}	peak soldering temperature			-	260	°C
V _{ESD}	electrostatic discharge voltage	MM (JEDEC JESD22-A115)		270	-	V
Source-drain diode						
I _S	source current	T _{mb} = 25 °C		-	61	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	367	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	V _{GS} = 10 V; T _{j(init)} = 25 °C; I _D = 92 A; V _{sup} ≤ 30 V; R _{GS} = 50 Ω; unclamped; Fig. 3		-	21	mJ

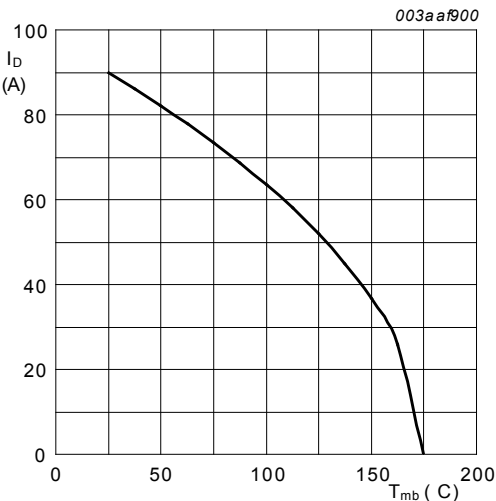


Fig. 1. Continuous drain current as a function of mounting base temperature

$V_{GS} \geq 10V$

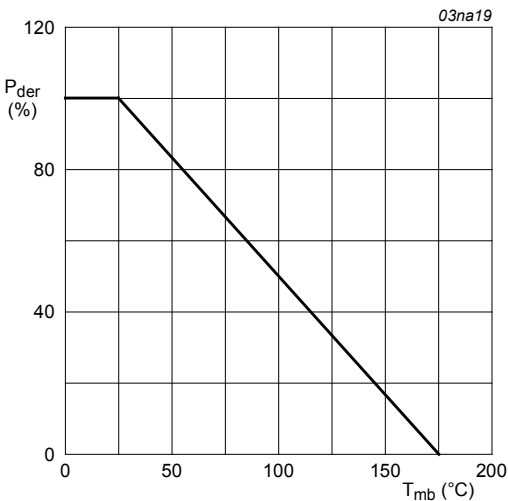


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

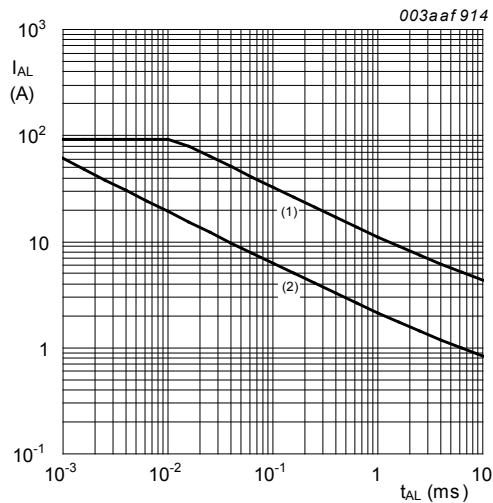


Fig. 3. Single pulse avalanche rating; avalanche current as a function of avalanche time

(1) $T_{j\ (init)} = 25^{\circ}C$; (2) $T_{j\ (init)} = 100^{\circ}C$

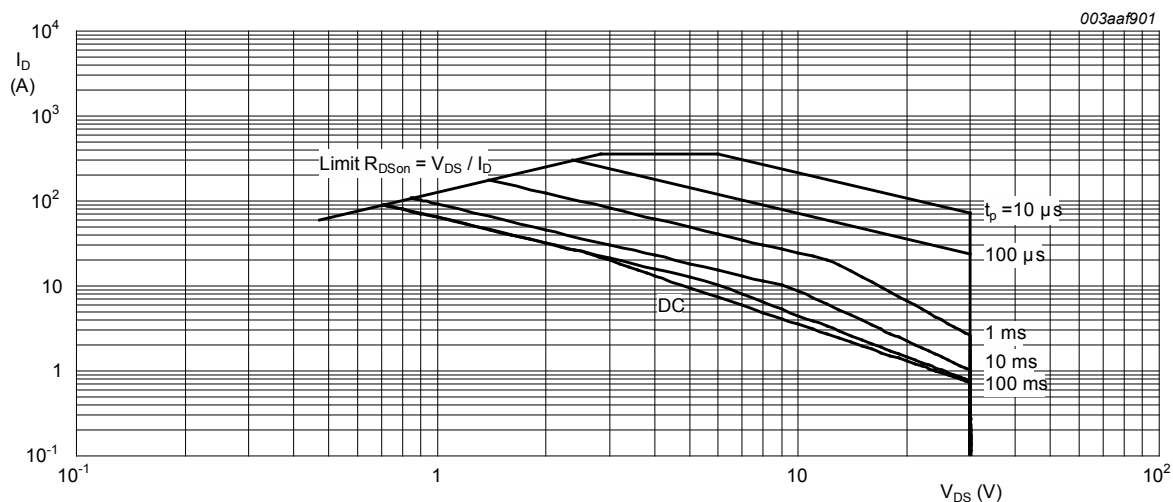


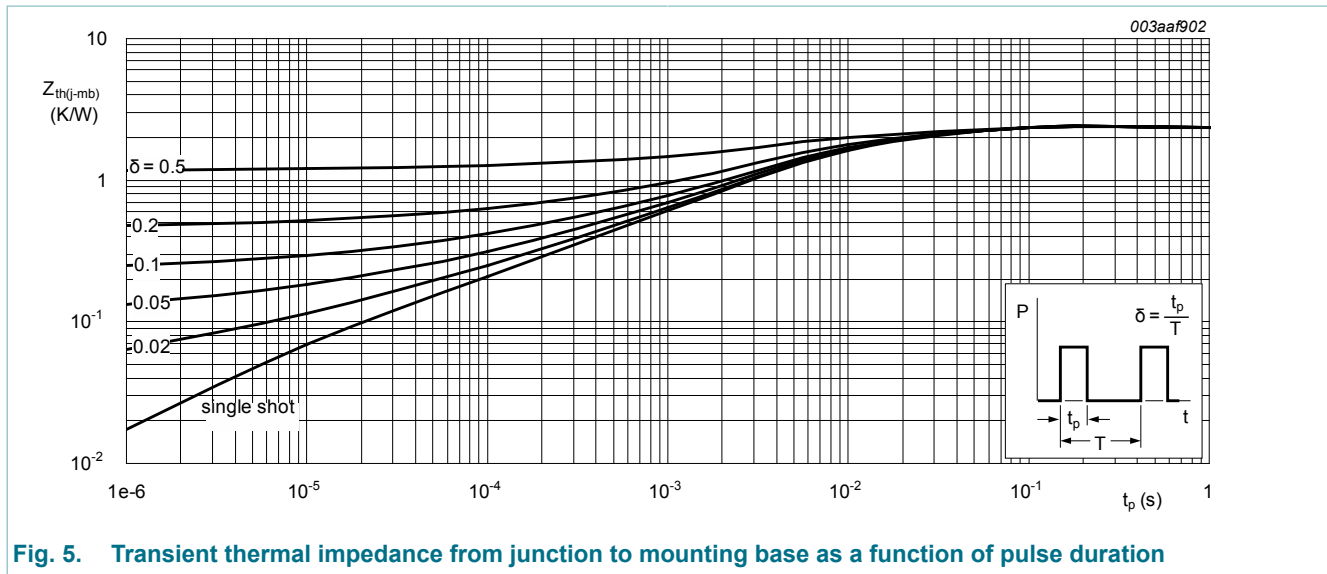
Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

$T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	2.05	2.24	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	30	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_J = -55\ ^\circ C$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_J = 25\ ^\circ C$; Fig. 10 ; Fig. 11	1.05	1.58	1.95	V
		$I_D = 10\ mA$; $V_{DS} = V_{GS}$; $T_J = 150\ ^\circ C$	0.5	-	-	V
		$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_J = -55\ ^\circ C$	-	-	2.25	V
I_{DSS}	drain leakage current	$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	1	μA
		$V_{DS} = 30\ V$; $V_{GS} = 0\ V$; $T_J = 150\ ^\circ C$	-	-	100	μA
I_{GSS}	gate leakage current	$V_{GS} = 16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -16\ V$; $V_{DS} = 0\ V$; $T_J = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\ V$; $I_D = 20\ A$; $T_J = 25\ ^\circ C$; Fig. 12	-	4.75	5.7	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 20\ A$; $T_J = 150\ ^\circ C$; Fig. 12 ; Fig. 13	-	-	9.4	mΩ
		$V_{GS} = 10\ V$; $I_D = 20\ A$; $T_J = 25\ ^\circ C$; Fig. 12	-	3.65	4.35	mΩ
		$V_{GS} = 10\ V$; $I_D = 20\ A$; $T_J = 150\ ^\circ C$; Fig. 12 ; Fig. 13	-	-	7.25	mΩ
R_G	gate resistance	$f = 1\ MHz$	-	1.9	3.8	Ω

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	$I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 10\text{ V}$; Fig. 14 ; Fig. 15		-	23	-	nC
		$I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 14 ; Fig. 15		-	11	-	nC
		$I_D = 0\text{ A}$; $V_{DS} = 0\text{ V}$; $V_{GS} = 10\text{ V}$		-	20	-	nC
Q_{GS}	gate-source charge	$I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; $V_{GS} = 4.5\text{ V}$; Fig. 14 ; Fig. 15		-	3.5	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge			-	2.3	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge			-	1.2	-	nC
Q_{GD}	gate-drain charge			-	3.5	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 20\text{ A}$; $V_{DS} = 15\text{ V}$; Fig. 14 ; Fig. 15		-	2.66	-	V
C_{iss}	input capacitance	$V_{DS} = 15\text{ V}$; $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ °C}$; Fig. 16		-	1502	-	pF
C_{oss}	output capacitance			-	316	-	pF
C_{rss}	reverse transfer capacitance			-	106	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}$; $R_L = 0.6\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_{G(ext)} = 4.7\text{ }\Omega$		-	16	-	ns
t_r	rise time			-	19	-	ns
$t_{d(off)}$	turn-off delay time			-	24	-	ns
t_f	fall time			-	10	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$; $f = 1\text{ MHz}$; $T_J = 25\text{ °C}$		-	8	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 20\text{ A}$; $V_{GS} = 0\text{ V}$; $T_J = 25\text{ °C}$; Fig. 17		-	0.8	1.1	V
t_{rr}	reverse recovery time	$I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$		-	23	-	ns
Q_r	recovered charge			-	15	-	nC
t_a	reverse recovery rise time	$V_{GS} = 0\text{ V}$; $I_S = 20\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; $V_{DS} = 15\text{ V}$; Fig. 18		-	13.5	-	ns
t_b	reverse recovery fall time			-	9.5	-	ns

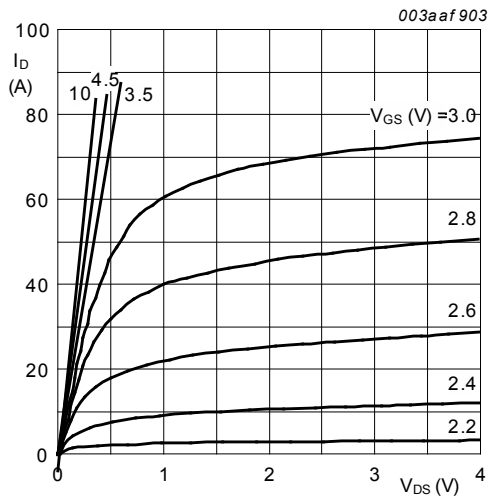


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

$T_j = 25^{\circ}\text{C}$

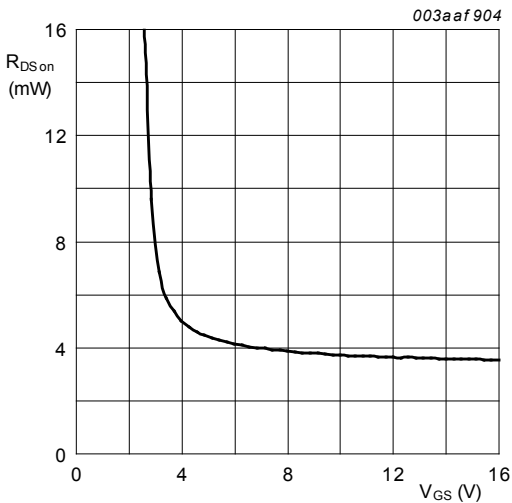


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

$T_j = 25^{\circ}\text{C}; I_D = 20\text{A}$

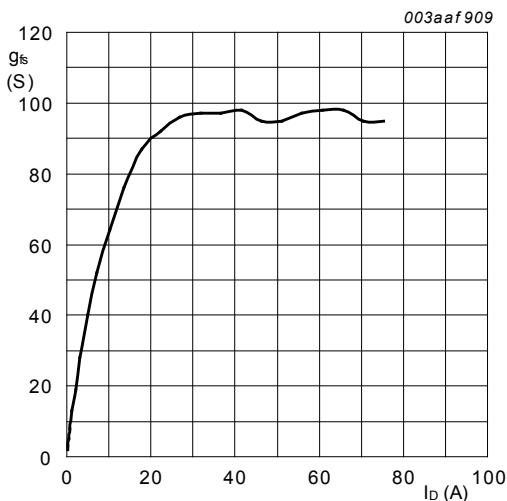


Fig. 8. Forward transconductance as a function of drain current; typical values

$T_j = 25^{\circ}\text{C}; V_{DS} = 10\text{V}$

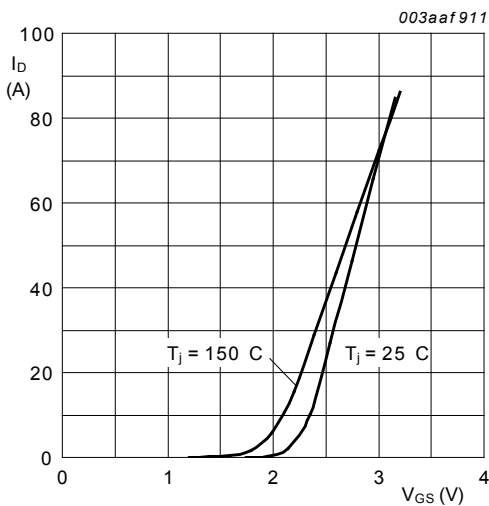


Fig. 9. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$V_{DS} = 10\text{V}$

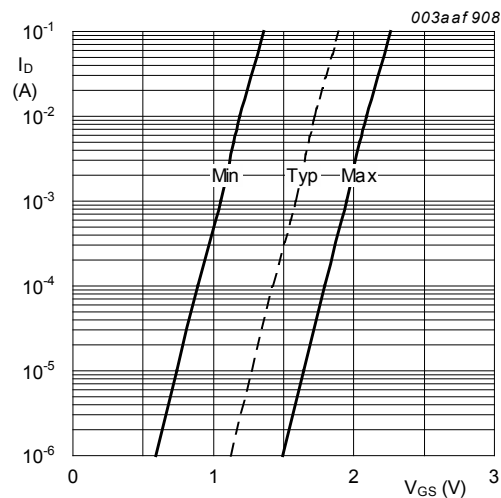


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25^{\circ}\text{C}; V_{DS} = 5\text{V}$

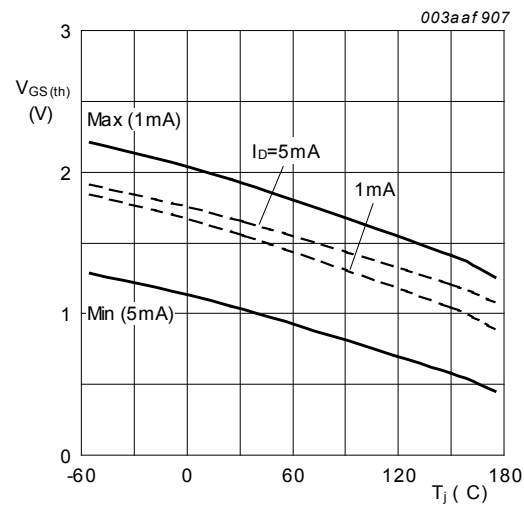


Fig. 11. Gate-source threshold voltage as a function of junction temperature

$V_{DS} = V_{GS}$

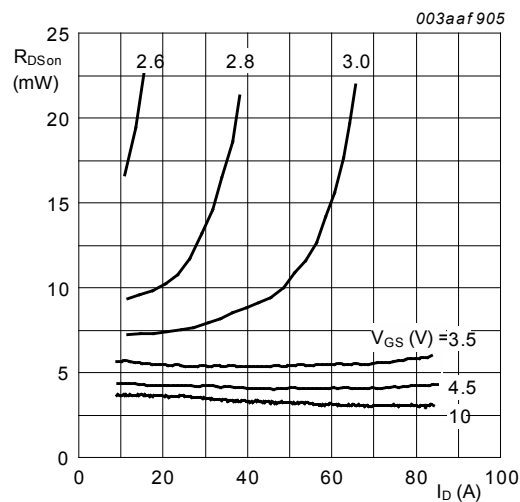


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

$T_j = 25^{\circ}\text{C}$

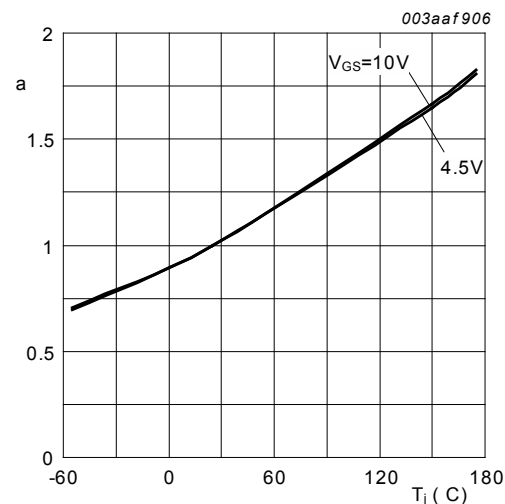


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$

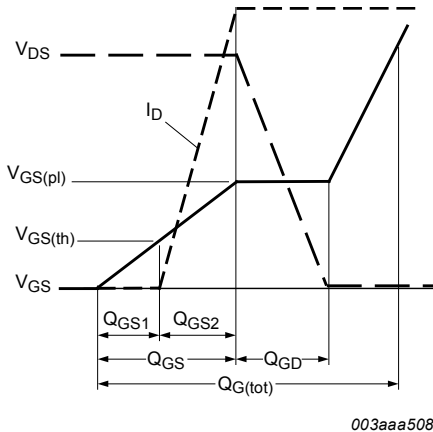


Fig. 14. Gate charge waveform definitions

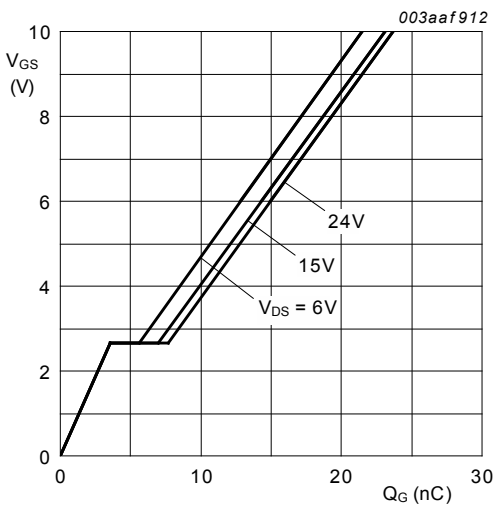


Fig. 15. Gate-source voltage as a function of gate charge; typical values

$T_j = 25^\circ C; I_D = 20A$

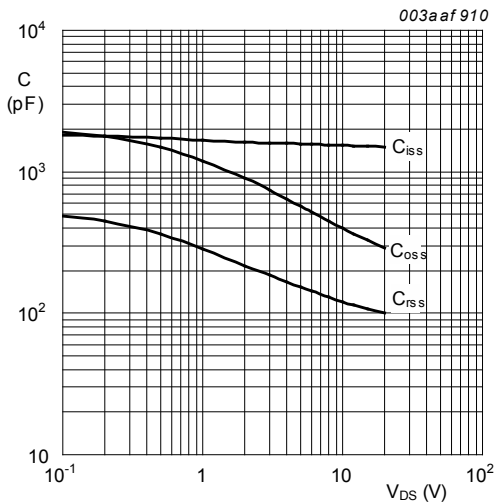


Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0V; f = 1MHz$

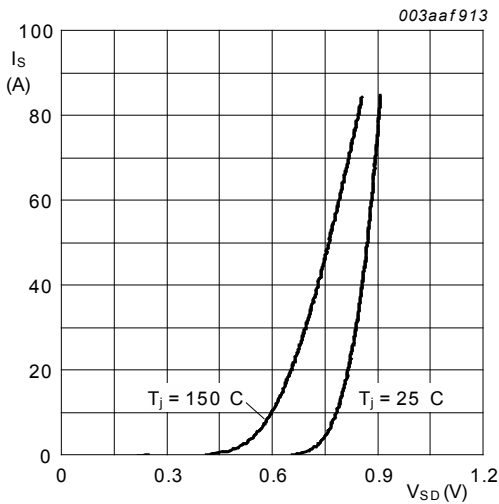


Fig. 17. Source current as a function of source-drain voltage; typical values

$V_{GS} = 0V$

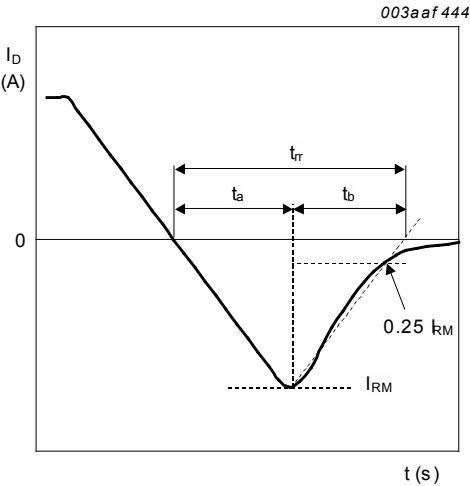


Fig. 18. Reverse recovery timing definition

11. Package outline

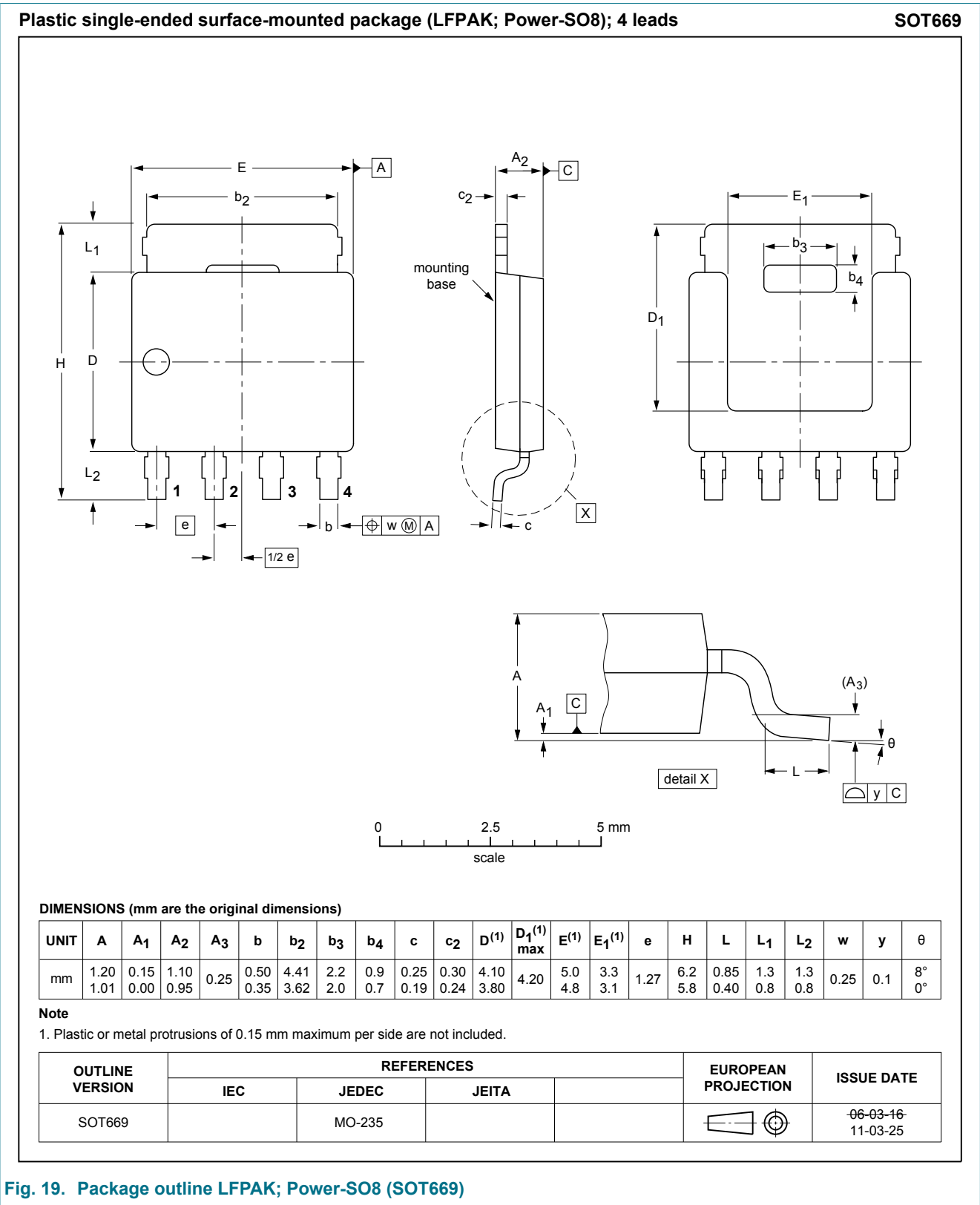


Fig. 19. Package outline LPAK; Power-SO8 (SOT669)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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