

# PXP1500-100QS

100 V, P-channel Trench MOSFET

31 July 2023

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in an MLPAK33 (SOT8002-2) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Trench MOSFET technology
- MLPAK33 package (3.3 x 3.3 mm footprint)
- Low thermal resistance
- Low 0.8 mm profile

## 3. Applications

- Active clamp circuits

## 4. Quick reference data

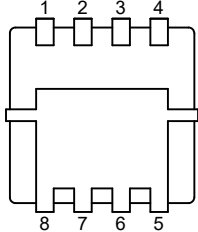
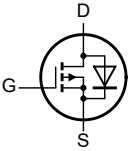
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-100	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = -10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	-0.7	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -0.7\text{ A}; T_j = 25\text{ °C}$	-	930	1500	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>MLPAK33 (SOT8002-2)</p>	 <p>017aaa094</p>
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PXP1500-100QS	MLPAK33	plastic thermal enhanced surface mounted package; mini leads; 8 terminals; pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body	SOT8002-2

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PXP1500-100QS	9AM

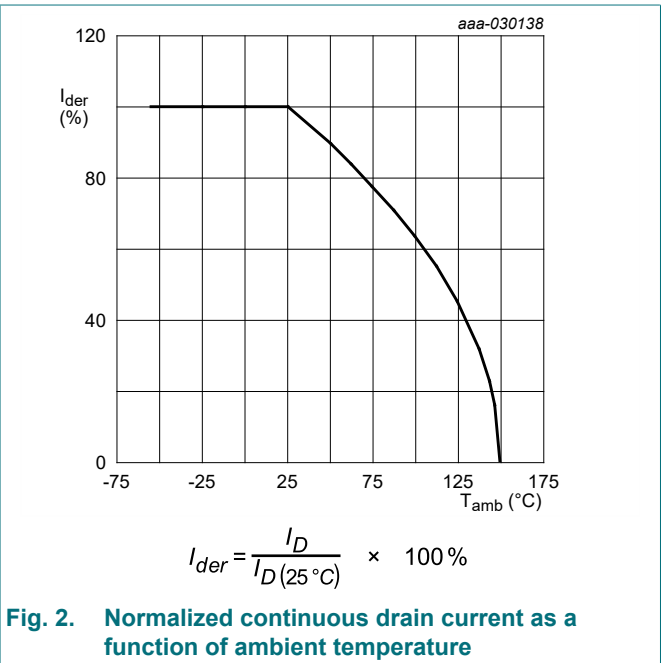
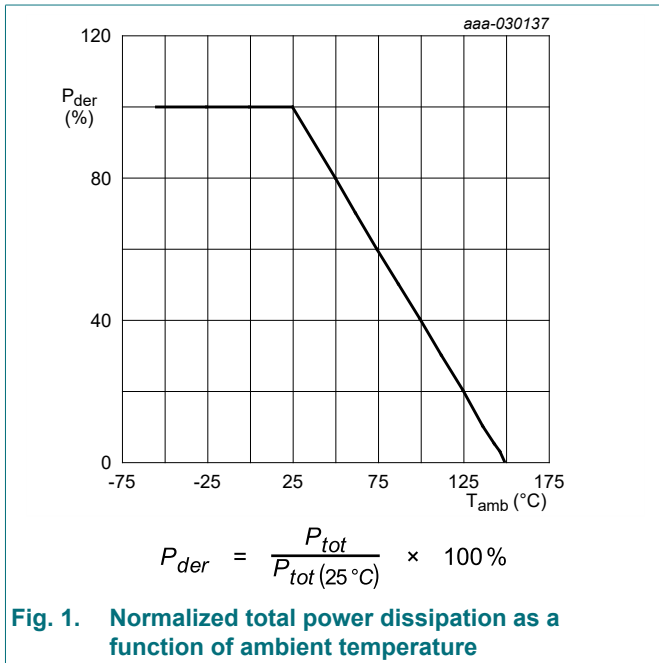
## 8. Limiting values

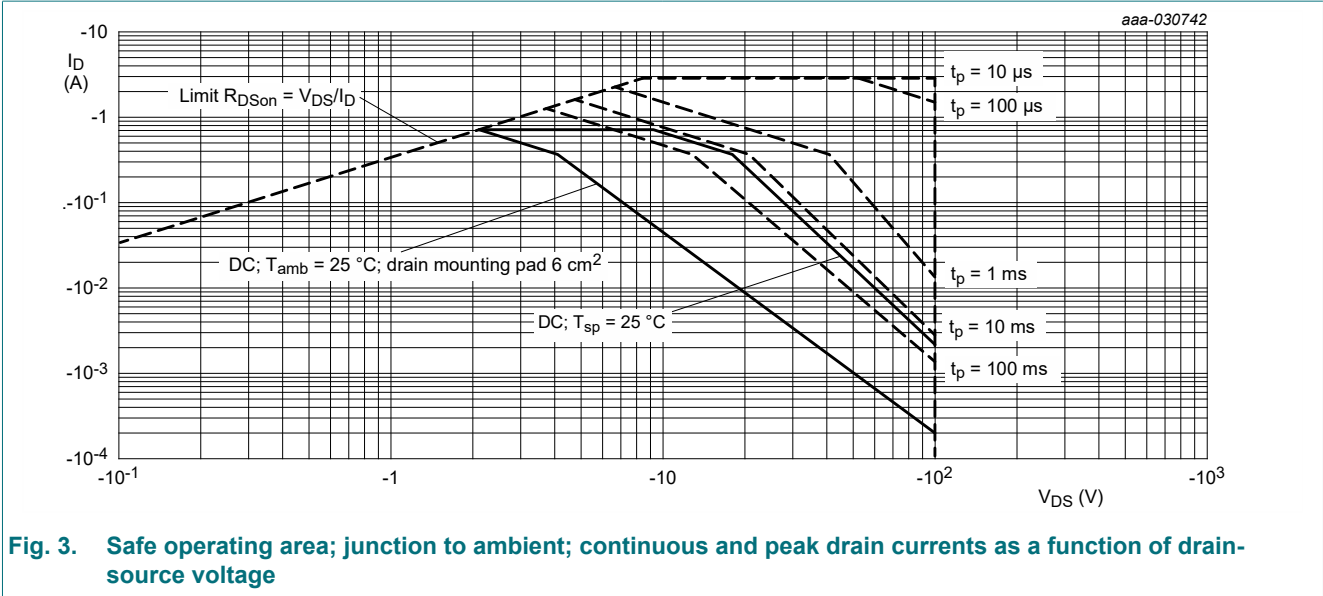
**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C		-	-100	V
V <sub>GS</sub>	gate-source voltage			-20	20	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 25 °C	[1]	-	-0.7	A
		V <sub>GS</sub> = -10 V; T <sub>amb</sub> = 100 °C	[1]	-	-0.4	A
		V <sub>GS</sub> = -10 V; T <sub>sp</sub> = 25 °C		-	-1.4	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs		-	-3	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[1]	-	1.4	W
		T <sub>sp</sub> = 25 °C		-	6.1	W
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-0.66	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = -0.6 A; DUT in avalanche (unclamped)		-	7	mJ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.





## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	170	205	K/W
			[2]	-	75	90	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	17.2	20.5	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

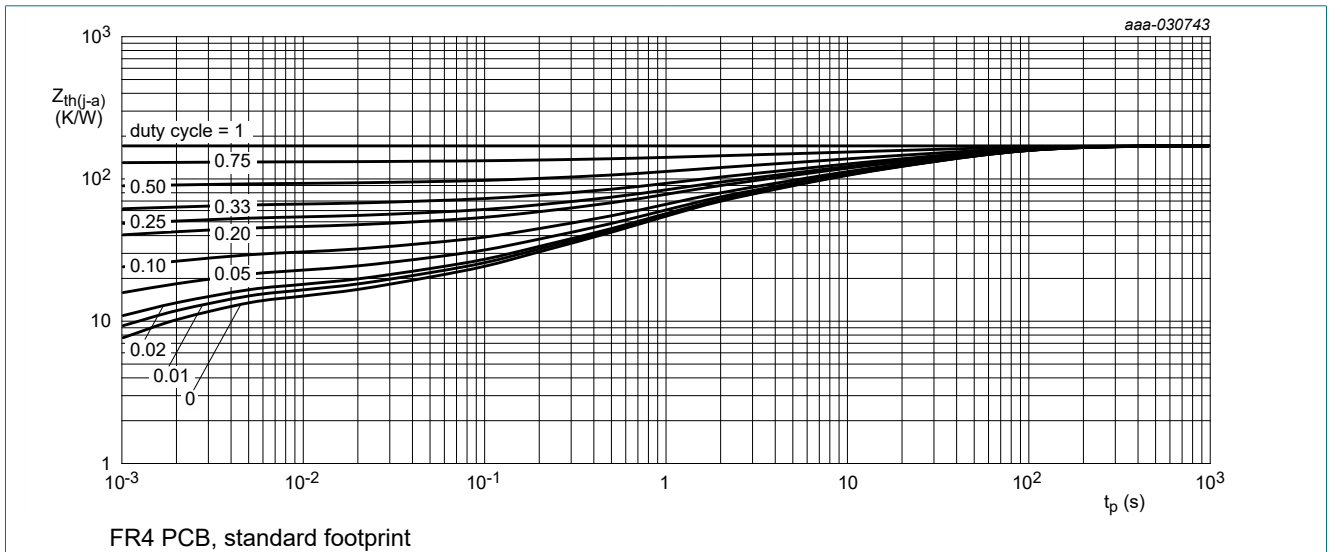


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

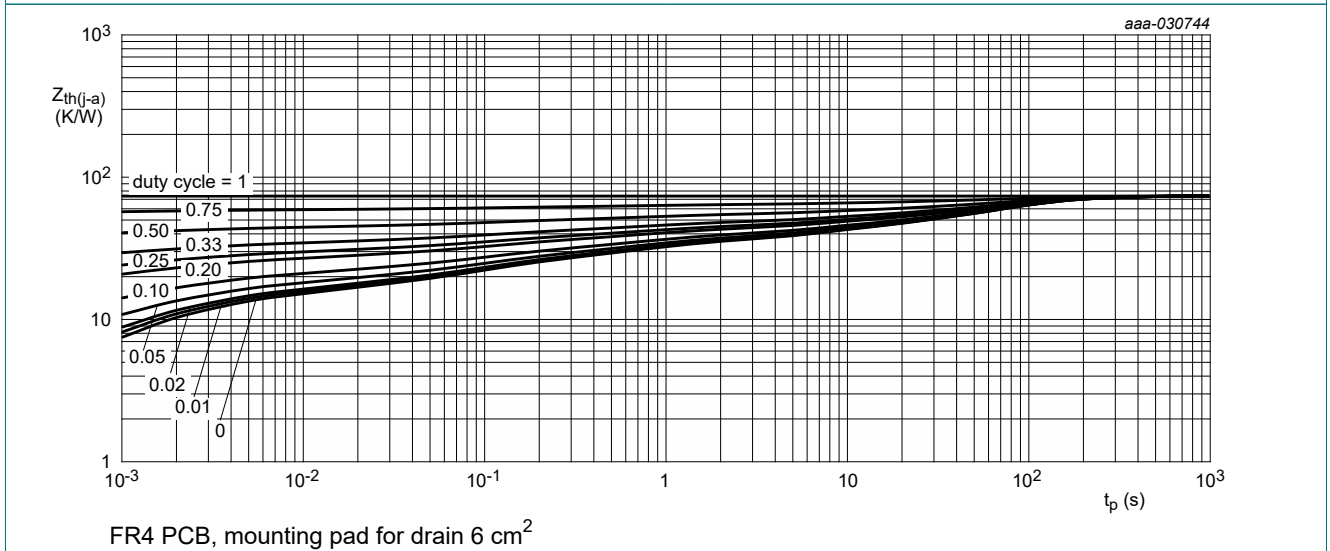


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-100	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C}$	-2	-3	-4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0 \text{ V}; V_{DS} = -100 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
		$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -10 \text{ V}; I_D = -0.7 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	930	1500	m $\Omega$
		$V_{GS} = -10 \text{ V}; I_D = -0.7 \text{ A}; T_j = 150 \text{ }^\circ\text{C}$	-	2000	3165	m $\Omega$
		$V_{GS} = -6 \text{ V}; I_D = -0.6 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	1000	1700	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -5 \text{ V}; I_D = -0.7 \text{ A}; T_j = 25 \text{ }^\circ\text{C}$	-	1.6	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$	-	26	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -50 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -10 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	3.1	4.5	nC
		$V_{DS} = -50 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -6 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2.1	3.1	nC
$Q_{GS}$	gate-source charge	$T_j = 25 \text{ }^\circ\text{C}$	-	0.6	-	nC
$Q_{GD}$	gate-drain charge		-	0.9	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -50 \text{ V}; f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	159	-	pF
$C_{oss}$	output capacitance		-	8	-	pF
$C_{rss}$	reverse transfer capacitance		-	4.5	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -50 \text{ V}; I_D = -0.6 \text{ A}; V_{GS} = -6 \text{ V}; R_{G(ext)} = 5 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	5	-	ns
$t_r$	rise time		-	17	-	ns
$t_{d(off)}$	turn-off delay time		-	5	-	ns
$t_f$	fall time		-	12	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -0.7 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	-0.8	-1.2	V
$t_{rr}$	reverse recovery time	$I_S = -0.6 \text{ A}; di_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = -6 \text{ V}; V_{DS} = -40 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	24	-	ns
$Q_r$	recovered charge		-	20	-	nC

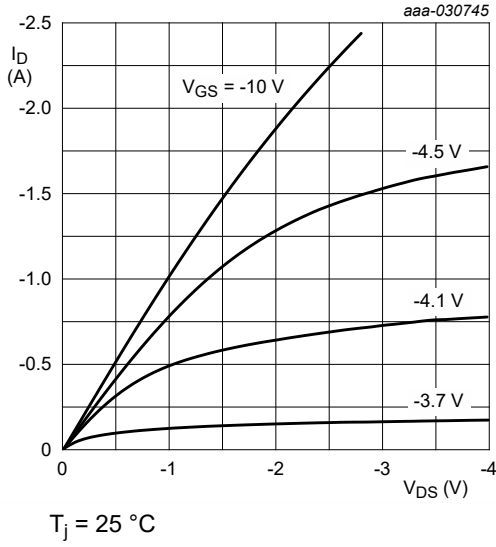


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

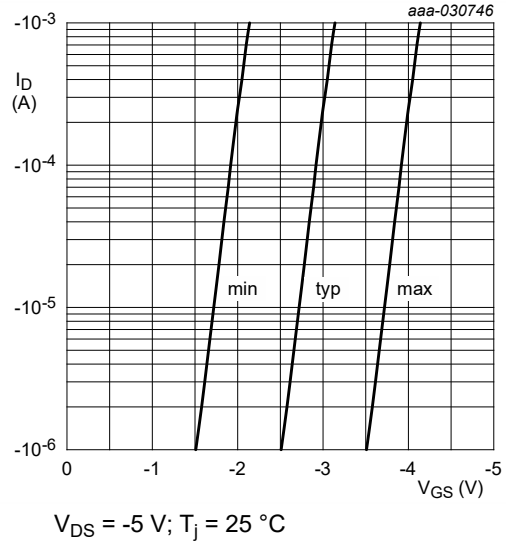


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

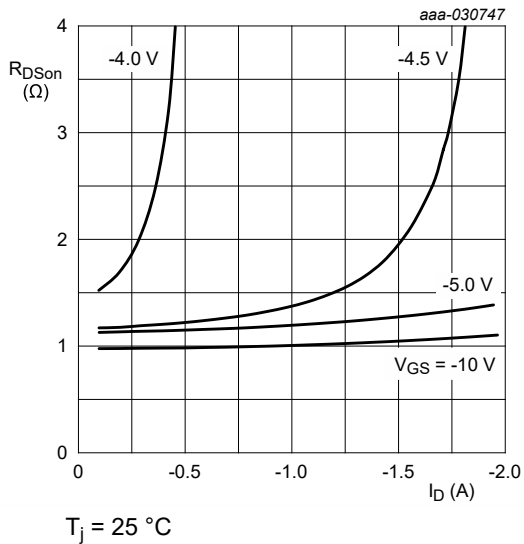


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

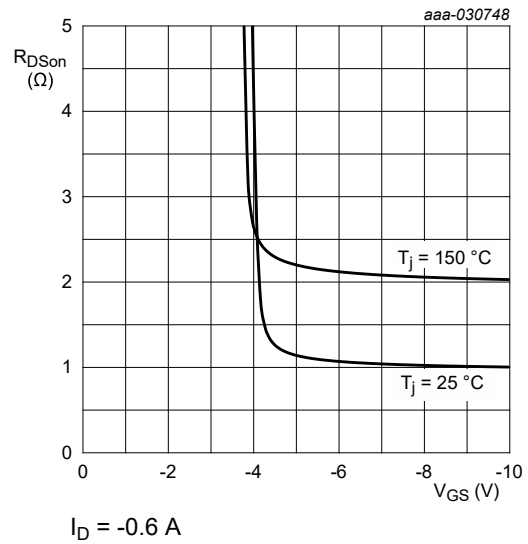


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

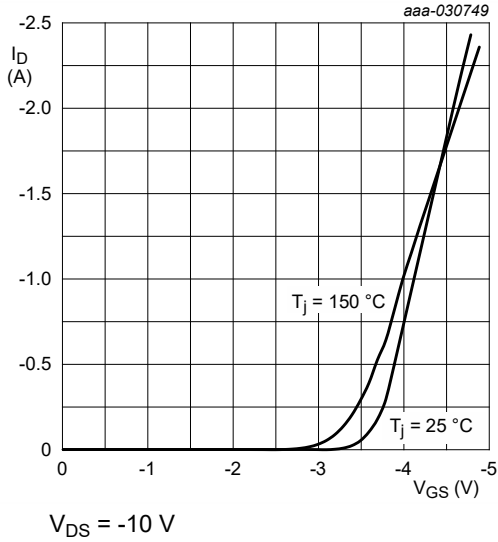


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

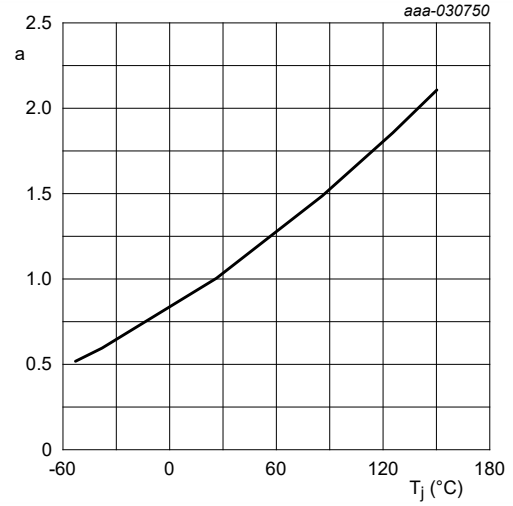


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

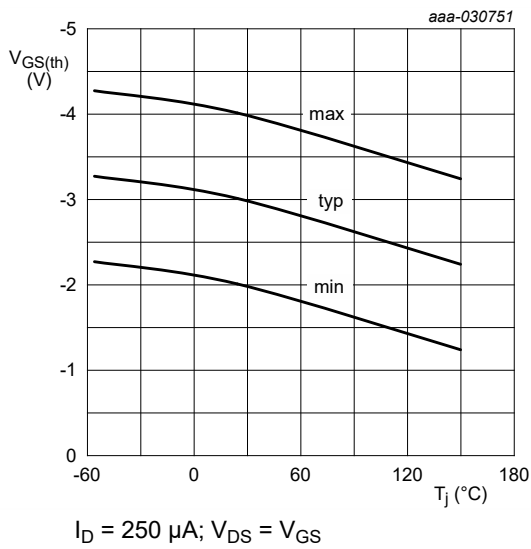


Fig. 12. Gate-source threshold voltage as a function of junction temperature

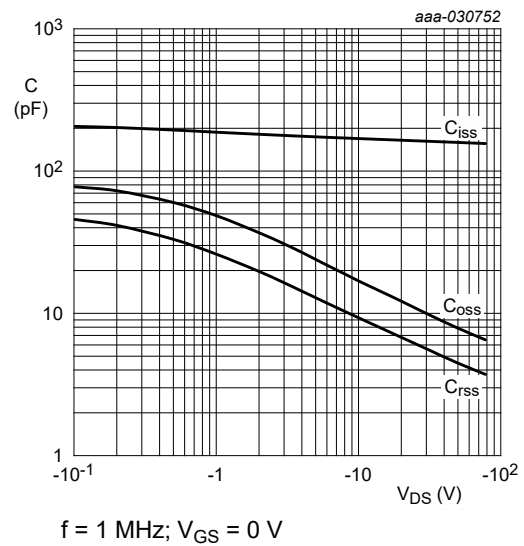
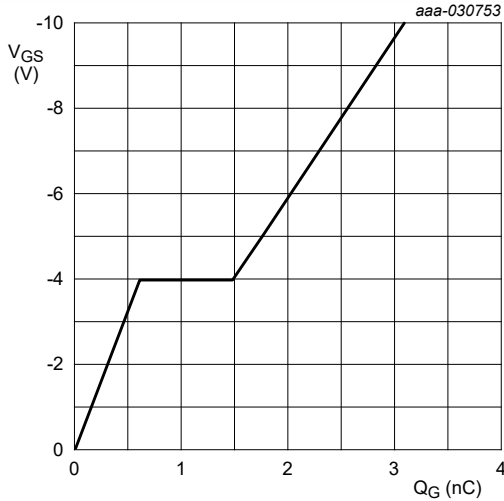


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values





$I_D = -0.6$  A;  $V_{DS} = -50$  V;  $T_j = 25$  °C

Fig. 14. Gate-source voltage as a function of gate charge; typical values

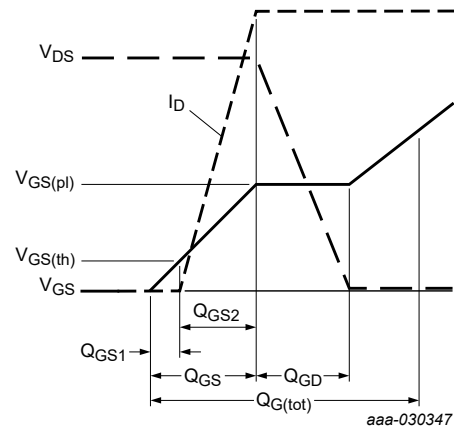
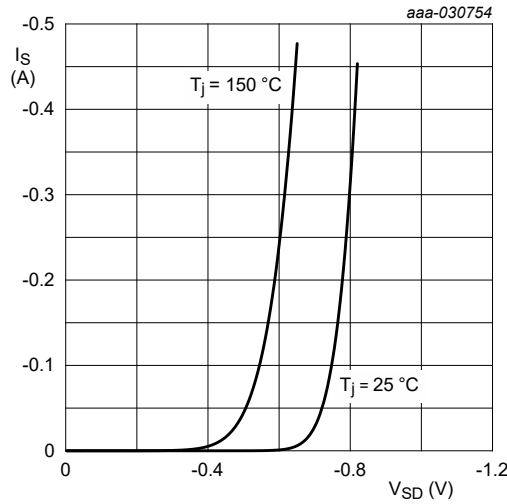


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0$  V

Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

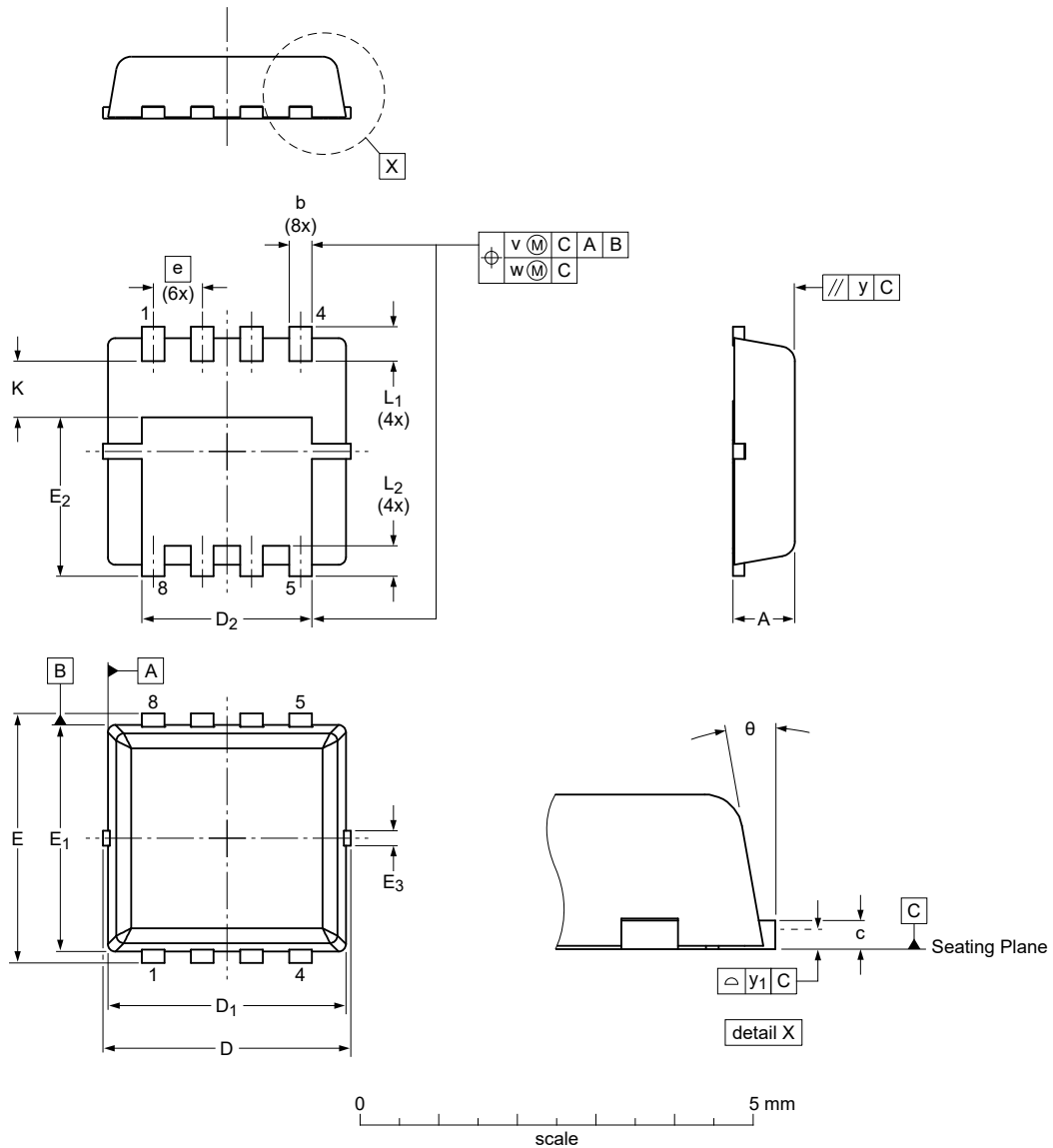


Fig. 17. Duty cycle definition

## 12. Package outline

MLPAK33: plastic thermal enhanced surface mounted package; mini leads; 8 terminals;  
pitch 0.65 mm; 3.3 x 3.3 x 0.8 mm body

SOT8002-2



Dimensions (mm are the original dimensions)

Unit	A	b	c	D	D <sub>1</sub>	D <sub>2</sub>	e	E	E <sub>1</sub>	E <sub>2</sub>	E <sub>3</sub>	K	L <sub>1</sub>	L <sub>2</sub>	θ	y	y <sub>1</sub>	v	w
max	0.90	0.35	0.18	3.40	3.20	2.35		3.35	3.10	2.20	0.25		0.55	0.50	12°				
mm	nom	0.80	0.30	3.30	3.15	2.25	0.65	3.30	3.00	2.10	0.20	0.6	0.45	0.40	10°	0.05	0.05	0.1	0.05
	min	0.70	0.25	3.20	3.10	2.15		3.25	2.90	2.00	0.15	(ref)	0.35	0.30	8°				

sot8002-2\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	EIAJ			
SOT8002-2						20-01-08 23-05-17

Fig. 18. Package outline MLPAK33 (SOT8002-2)

### 13. Soldering

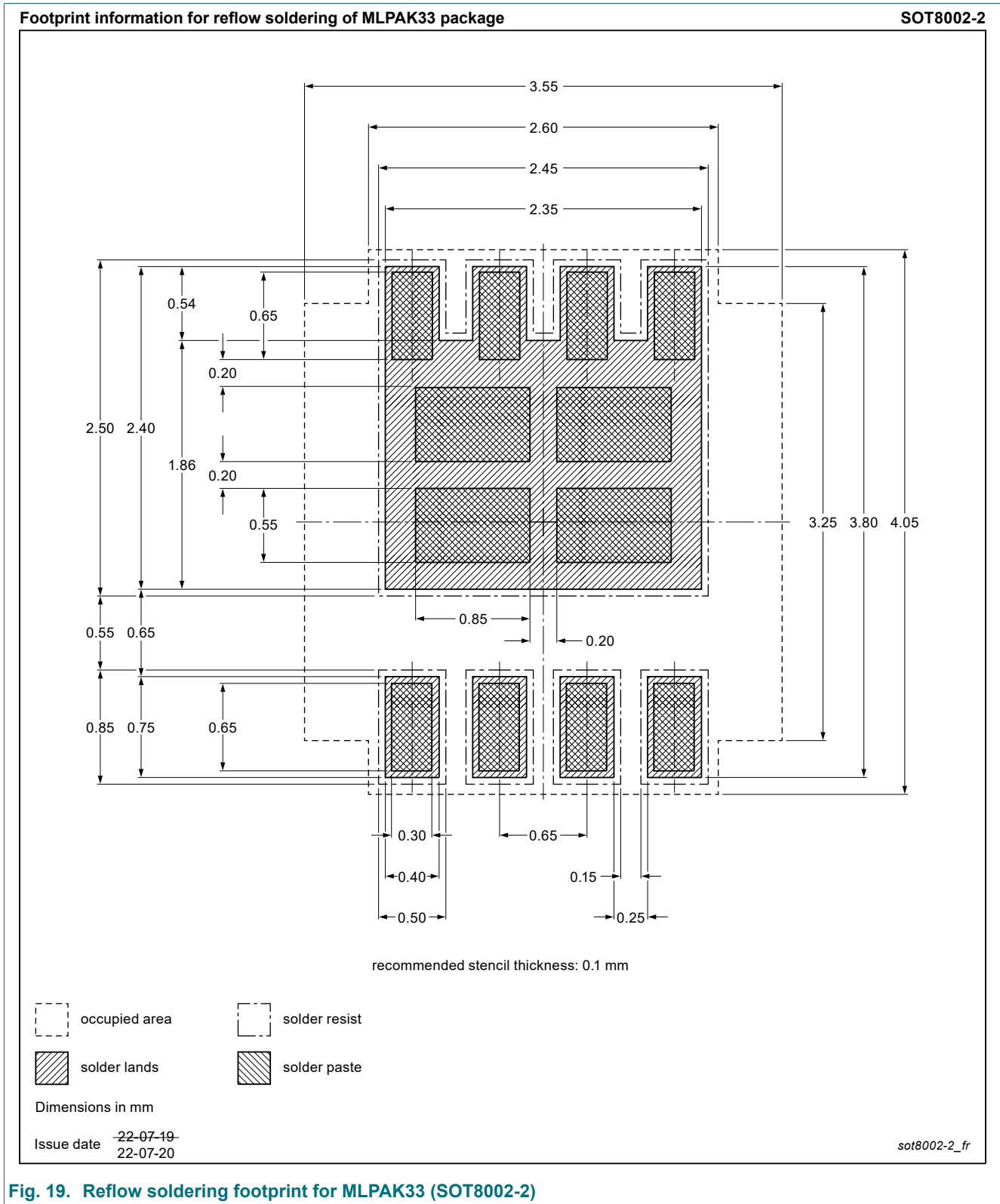


Fig. 19. Reflow soldering footprint for MLPAK33 (SOT8002-2)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PXP1500-100QS v.3	20230731	Product data sheet	-	PXP1500-100QS v.2
Modifications:	• Chapter "Package outline": drawing update			
PXP1500-100QS v.2	20211120	Product data sheet	-	PXP1500-100QS v.1
PXP1500-100QS v.1	20200507	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 31 July 2023

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