Product data sheet

1. General description

Low capacitance unidirectional ElectroStatic Discharge (ESD) protection diode in a SOD523 (SC-79) ultra small and flat lead Surface-Mounted Device (SMD) plastic package, designed to protect one signal line from the damage caused by ESD and other transients.

2. Features and benefits

- ESD protection of one line
- Low diode capacitance
- Max. peak pulse power: P_{PPM} = 180 W
- Low clamping voltage: V_{CL} = 14 V
- Low leakage current: I_{RM} < 1 nA
- ESD protection up to 30 kV (IEC 61000-4-2)
- IEC 61000-4-5 (surge); I_{PPM} = 10 A
- Qualified according to AEC-Q101 and recommended for use in automotive applications

3. Application information

- Computers and peripherals
- Audio and video equipment
- Cellular handsets and accessories
- 10/100/1000 Mbit/s Ethernet
- Communication systems
- Portable electronics
- SIM card protection
- High-speed data lines

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	7	V
I _{PPM}	rated peak pulse current	t _p = 8/20 μs	[1] [2]	-	-	10	Α
V_{CL}	clamping voltage	$I_{PPM} = 10 \text{ A}; t_p = 8/20 \mu\text{s}; T_{amb} = 25 ^{\circ}\text{C}$	[1] [2]	-	-	19	V

- [1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
- Measured from pin 1 to pin 2.



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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode		
2	A	anode	1 2 SC-79 (SOD523)	K A 006aaa152

6. Ordering information

Table 3. Ordering information

Type number	Package					
	Name	Description	Version			
PESD5Z7.0-Q	SC-79	plastic, surface-mounted package; 2 leads; 1.2 mm x 0.8 mm x 0.6 mm body	SOD523			

7. Marking

Table 4. Marking codes

Type number	Marking code
PESD5Z7.0-Q	NB

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1] [2]	-	180	W
I _{PPM}	rated peak pulse current		[1] [2]	-	10	Α
Tj	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximi	um ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[3] [2]	-	30	kV
	voltage	MIL-STD-883; human body model (HBM)		-	10	kV
		machine model		-	400	V

- [1] Non-repetitive current pulse 8/20 μs exponentially decaying waveform according to IEC 61000-4-5.
- [2] Measured from pin 1 to pin 2.
- [3] Device stressed with ten non-repetitive ESD pulses.

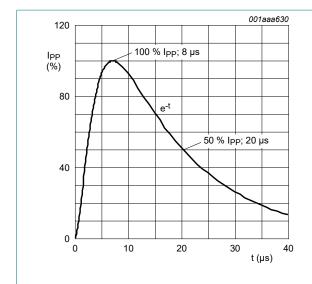


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

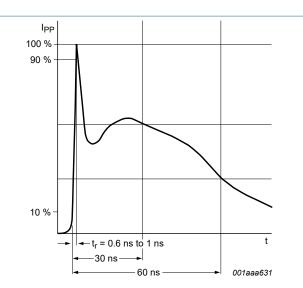


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

Low capacitance unidirectional ESD protection diodes

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _{amb} = 25 °C		-	-	7	V
V_{BR}	breakdown voltage	I _R = 1 mA; T _{amb} = 25 °C		7.5	-	-	V
I _{RM}	reverse leakage current	V _{RWM} = 7 V; T _{amb} = 25 °C		-	1	10	nA
C _d	diode capacitance	f = 1 MHz; V _R = 0 V; T _{amb} = 25 °C		-	69	150	pF
V _{CL}	clamping voltage	I _{PP} = 5 A; t _p = 8/20 μs; T _{amb} = 25 °C	[1] [2]	-	14	15	V
		I_{PPM} = 10 A; t_p = 8/20 µs; T_{amb} = 25 °C	[1] [2]	-	-	19	V
R _{diff}	differential resistance	I _R = 5 mA; T _{amb} = 25 °C		-	-	15	Ω

- [1] Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC 61000-4-5.
- [2] Measured from pin 1 to pin 2.

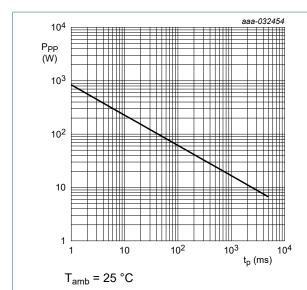


Fig. 3. Peak pulse power as a function of exponential pulse duration; typical values

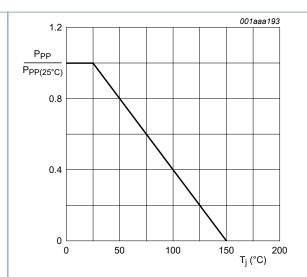


Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values

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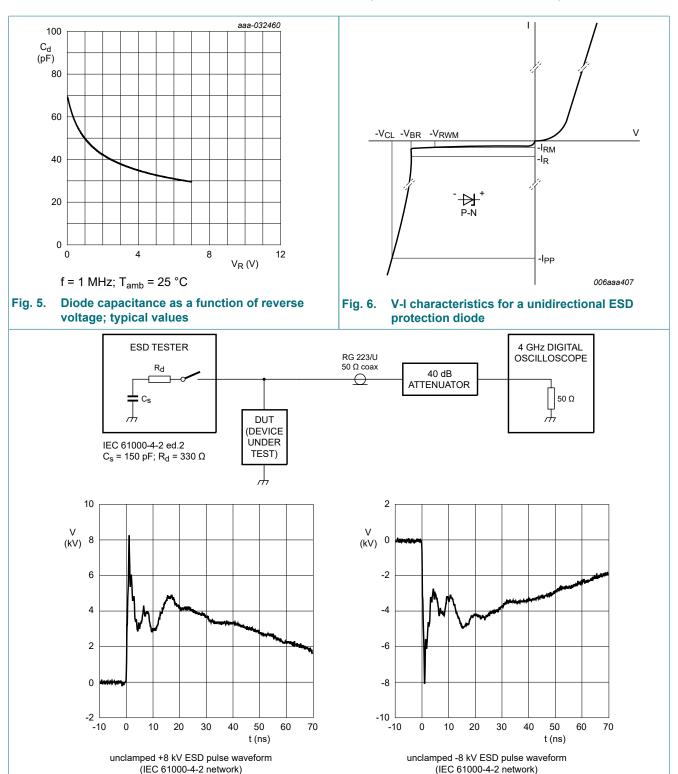


Fig. 7.

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ESD clamping test setup and waveforms

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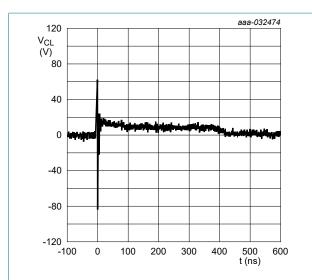


Fig. 8. Clamped +8 kV ESD pulse waveform (IEC 61000-4-2 network)

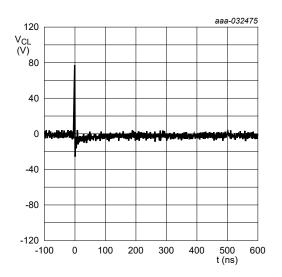
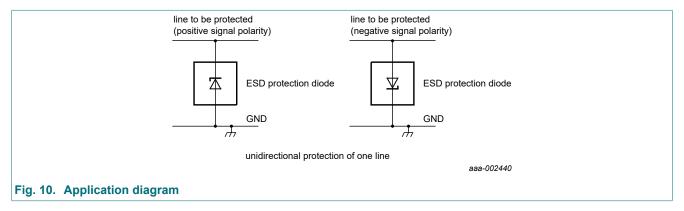


Fig. 9. Clamped -8 kV ESD pulse waveform (IEC 61000-4-2 network)

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10. Application information

The device is designed for protection of one unidirectional data or signal line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are either positive or negative with respect to ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- **6.** Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

11. Test information

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

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12. Package outline

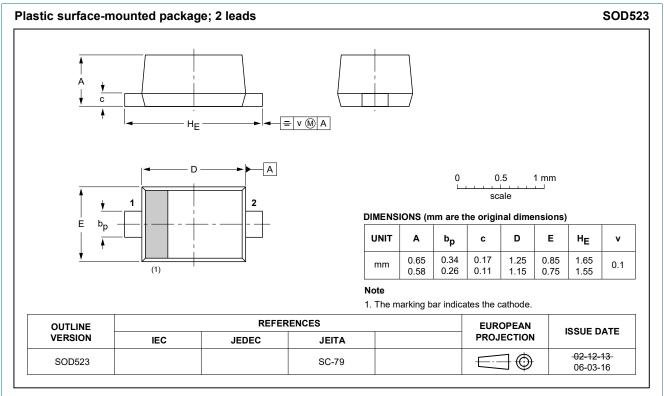
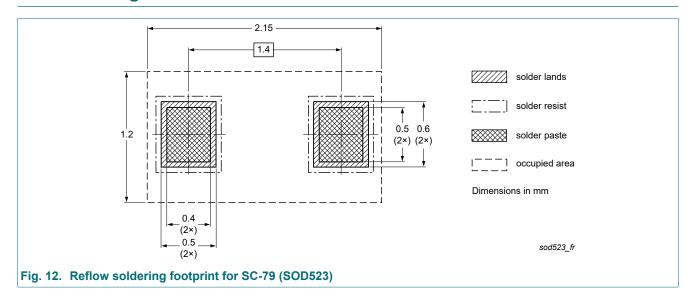


Fig. 11. Package outline SC-79 (SOD523)

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13. Soldering



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14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5Z7_0-Q v.1	20221125	Product data sheet	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
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