

# PSMN9R8-100YSF

# NextPower 100 V, 10.2 mOhm N-channel MOSFET in LFPAK56 package

20 June 2023

**Product data sheet** 

## 1. General description

NextPower 100 V, standard level gate drive MOSFET. Qualified to 175 °C and recommended for industrial and consumer applications.

#### 2. Features and benefits

- Low Q<sub>rr</sub> for higher efficiency and lower spiking
- Low Q<sub>G</sub> × R<sub>DSon</sub> FOM for high efficiency switching applications
- Strong avalanche energy rating (E<sub>AS</sub>)
- Avalanche rated and 100% tested
- Ha-free and RoHS compliant LFPAK56 package
- · Wave-solderable LFPAK56 package

## 3. Applications

- Synchronous rectifier in AC-DC and DC-DC
- Primary side switch in 48 V DC-DC
- · BLDC motor control
- USB-PD and mobile fast-charge adapters
- · Flyback and resonant topologies

### 4. Quick reference data

#### Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C		-	-	100	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>		-	-	80	Α
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>		-	-	147	W
Tj	junction temperature			-55	-	175	°C
Static chara	cteristics						'
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 25 °C; Fig. 12		-	8.3	10.2	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 20 \text{ A}; T_j = 100 ^{\circ}\text{C};$ Fig. 13		-	13	16.2	mΩ
Dynamic ch	aracteristics			'	'	'	'
Q <sub>GD</sub>	gate-drain charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;		1.8	6	13.8	nC
Q <sub>G(tot)</sub>	total gate charge	T <sub>j</sub> = 25 °C; <u>Fig. 14</u> ; <u>Fig. 15</u>		16.8	34	50.4	nC
Avalanche r	uggedness						'
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 30.4 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 56 μs; Fig. 4	[1]	-	-	111	mJ



Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain diode							
Q <sub>r</sub>		$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 18$		-	22	-	nC

[1] Protected by 100% test

## 5. Pinning information

**Table 2. Pinning information** 

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	
2	S	source	<u> </u>	D
3	S	source		
4	G	gate	0 0 0 0	G_(□□□□□)
mb	D	mounting base; connected to drain	LFPAK56; Power- SO8 (SOT669)	mbb076 S

## 6. Ordering information

**Table 3. Ordering information** 

Type number	Package		
	Name	Description	Version
PSMN9R8-100YSF	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

## 7. Marking

#### Table 4. Marking codes

Type number	Marking code
PSMN9R8-100YSF	9F8S10Y

# 8. Limiting values

#### **Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Tj = 25  $^{\circ}$ C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DS</sub>	drain-source voltage	25 °C ≤ T <sub>j</sub> ≤ 175 °C	-	100	V
$V_{DGR}$	drain-gate voltage	25 °C ≤ $T_j$ ≤ 175 °C; $R_{GS}$ = 20 kΩ	-	100	V
$V_{GS}$	gate-source voltage		-20	20	V
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <u>Fig. 1</u>	-	147	W
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 25 °C; <u>Fig. 2</u>	-	80	А
		V <sub>GS</sub> = 10 V; T <sub>mb</sub> = 100 °C; <u>Fig. 2</u>	-	57	А
I <sub>DM</sub>	peak drain current	pulsed; $t_p \le 10 \mu s$ ; $T_{mb} = 25 °C$ ; Fig. 3	-	320	А
T <sub>stg</sub>	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C

**Product data sheet** 

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>sld(M)</sub>	peak soldering temperature			-	260	°C
Source-drain	n diode		'	'		
Is	source current	T <sub>mb</sub> = 25 °C		-	80	Α
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 µs; T <sub>mb</sub> = 25 °C		-	320	Α
Avalanche r	uggedness		'			
E <sub>DS(AL)S</sub>	non-repetitive drain- source avalanche energy	$I_D$ = 30.4 A; $V_{sup} \le 100$ V; $R_{GS}$ = 50 Ω; $V_{GS}$ = 10 V; $T_{j(init)}$ = 25 °C; unclamped; $t_p$ = 56 μs; Fig. 4	[1]	-	111	mJ
I <sub>AS</sub>	non-repetitive avalanche current	$V_{sup} \le 100 \text{ V}; V_{GS} = 10 \text{ V}; T_{j(init)} = 25 \text{ °C}; R_{GS} = 50 \Omega; Fig. 4$	[1]	-	30.4	А

#### [1] Protected by 100% test

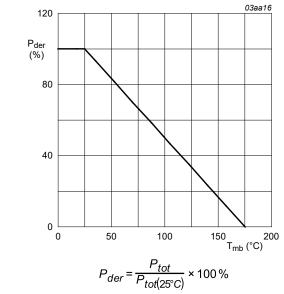
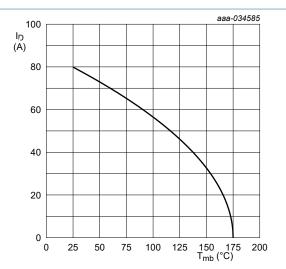


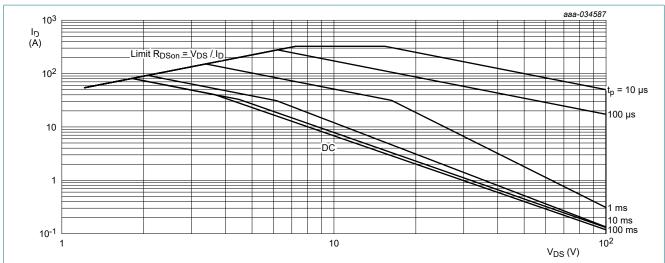
Fig. 1. Normalized total power dissipation as a function of mounting base temperature



 $V_{GS} \ge 10 \text{ V}$  80 A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature.

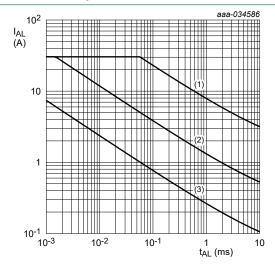
Fig. 2. Continuous drain current as a function of mounting base temperature

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T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1)  $T_{j \text{ (init)}}$  = 25 °C; (2)  $T_{j \text{ (init)}}$  = 150 °C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

### 9. Thermal characteristics

**Table 6. Thermal characteristics** 

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-mb)</sub>	thermal resistance from junction to mounting base	<u>Fig. 5</u>	-	0.92	1.02	K/W
R <sub>th(j-a)</sub>	thermal resistance from	Fig. 6	-	42	-	K/W
junction to ambient	<u>Fig. 7</u>	-	85	-	K/W	

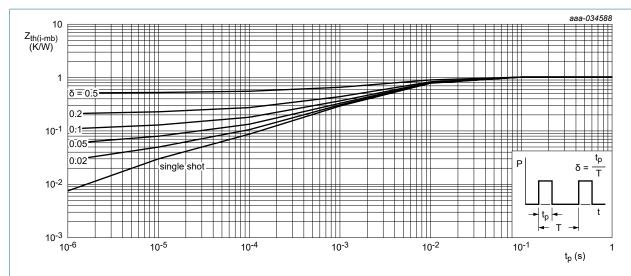
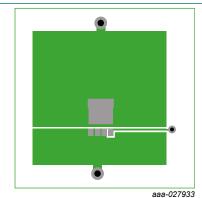
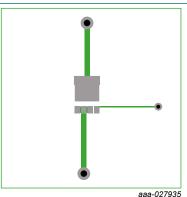


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration



Copper area 25.4 mm square; 70  $\mu$ m thick on FR4 board

Fig. 6. PCB layout for thermal resistance from junction to ambient



70 µm thick copper on FR4 board

Fig. 7. PCB layout with minimum footprint for thermal resistance from junction to ambient

## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static charac	cteristics		<u> </u>			
V <sub>(BR)DSS</sub>	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	100	-	-	V
	breakdown voltage	I <sub>D</sub> = 250 μA; V <sub>GS</sub> = 0 V; T <sub>j</sub> = -55 °C	90	-	-	V
V <sub>GS(th)</sub>	gate-source threshold	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ °C}; Fig. 11$	2	3	4	V
	voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> =V <sub>GS</sub> ; T <sub>j</sub> = 175 °C	-	1.8	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C}$	-	3.4	-	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	25 °C ≤ T <sub>j</sub> ≤ 150 °C	-	-7.4	-	mV/K
I <sub>DSS</sub>	drain leakage current	V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	0.01	1	μΑ
		V <sub>DS</sub> = 100 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 125 °C	-	5	100	μΑ
I <sub>GSS</sub>	gate leakage current	V <sub>GS</sub> = 20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA
		V <sub>GS</sub> = -20 V; V <sub>DS</sub> = 0 V; T <sub>j</sub> = 25 °C	-	2	100	nA

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Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$R_{DSon}$	drain-source on-state resistance	$V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 25 °C; Fig. 12	-	8.3	10.2	mΩ
		V <sub>GS</sub> = 7 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 25 °C; <u>Fig. 12</u>	-	9.7	15	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 20 A; $T_j$ = 100 °C; Fig. 13	-	13	16.2	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 20 A; T <sub>j</sub> = 175 °C; Fig. 13	-	18.4	23.2	mΩ
$R_G$	gate resistance	f = 1 MHz; T <sub>j</sub> = 25 °C	0.8	1.6	3.2	Ω
Dynamic ch	aracteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V; T <sub>j</sub> = 25 °C; <u>Fig. 14</u> ; <u>Fig. 15</u>	16.8	34	50.4	nC
		$I_D = 0 \text{ A}; V_{DS} = 0 \text{ V}; V_{GS} = 10 \text{ V};$ $T_j = 25 ^{\circ}\text{C}$	-	17.5	-	nC
Q <sub>GS</sub>	gate-source charge	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 10 V;	6.2	10.3	14.4	nC
Q <sub>GS(th)</sub>	pre-threshold gate- source charge	T <sub>j</sub> = 25 °C; <u>Fig. 14</u> ; <u>Fig. 15</u>	-	6.8	-	nC
Q <sub>GS(th-pl)</sub>	post-threshold gate- source charge		-	3.5	-	nC
Q <sub>GD</sub>	gate-drain charge		1.8	6	13.8	nC
V <sub>GS(pl)</sub>	gate-source plateau voltage	I <sub>D</sub> = 20 A; V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; Fig. 14; Fig. 15	-	4.6	-	V
C <sub>iss</sub>	input capacitance	V <sub>DS</sub> = 50 V; V <sub>GS</sub> = 0 V; f = 1 MHz;	1450	2417	3384	pF
C <sub>oss</sub>	output capacitance	T <sub>j</sub> = 25 °C; <u>Fig. 16</u>	347	579	926	pF
C <sub>rss</sub>	reverse transfer capacitance		2	20	52	pF
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 50 \text{ V}; R_L = 2.5 \Omega; V_{GS} = 10 \text{ V};$	-	10	-	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 5 \Omega; T_j = 25 °C$	-	9	-	ns
t <sub>d(off)</sub>	turn-off delay time	1	-	22	-	ns
t <sub>f</sub>	fall time	1	-	12	-	ns
Source-drai	n diode		ı	<u> </u>	<u> </u>	
V <sub>SD</sub>	source-drain voltage	$I_S = 20 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 17$	-	0.83	1	V
t <sub>rr</sub>	reverse recovery time	$I_S = 20 \text{ A}$ ; $dI_S/dt = -100 \text{ A/}\mu\text{s}$ ; $V_{GS} = 0 \text{ V}$ ;	-	31	-	ns
Q <sub>r</sub>	recovered charge	V <sub>DS</sub> = 50 V; T <sub>j</sub> = 25 °C; <u>Fig. 18</u>	-	22	-	nC
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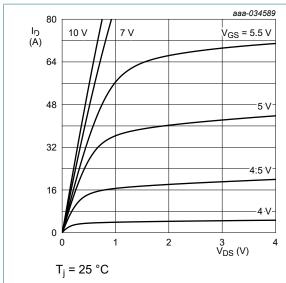


Fig. 8. Output characteristics; drain current as a function of drain-source voltage; typical values

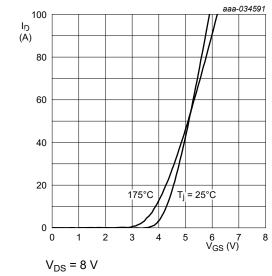


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values

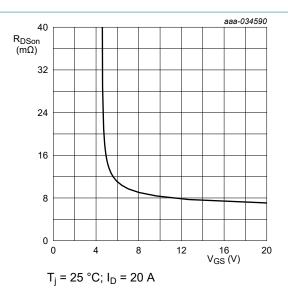


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

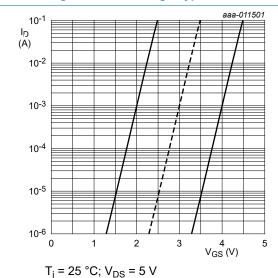


Fig. 11. Sub-threshold drain current as a function of gate-source voltage

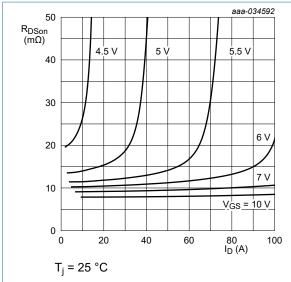


Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

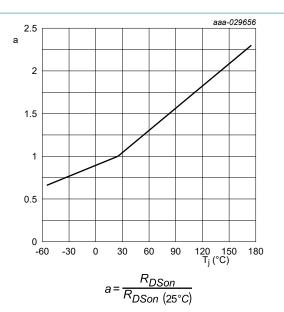


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

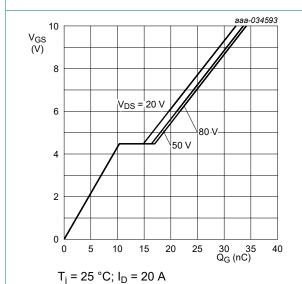


Fig. 14. Gate-source voltage as a function of gate charge; typical values

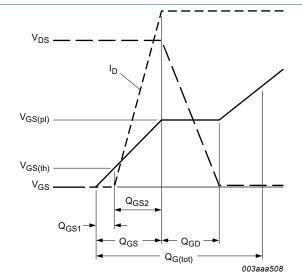


Fig. 15. Gate charge waveform definitions

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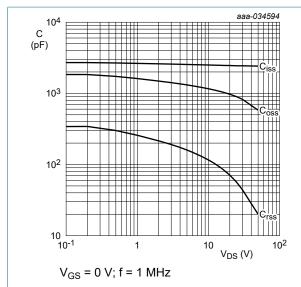
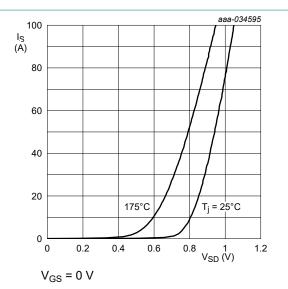


Fig. 16. Input, output and reverse transfer capacitances | Fig. 17. Source-drain (diode forward) current as a as a function of drain-source voltage; typical values



function of source-drain (diode forward) voltage; typical values

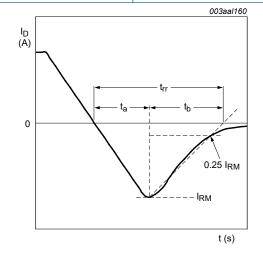
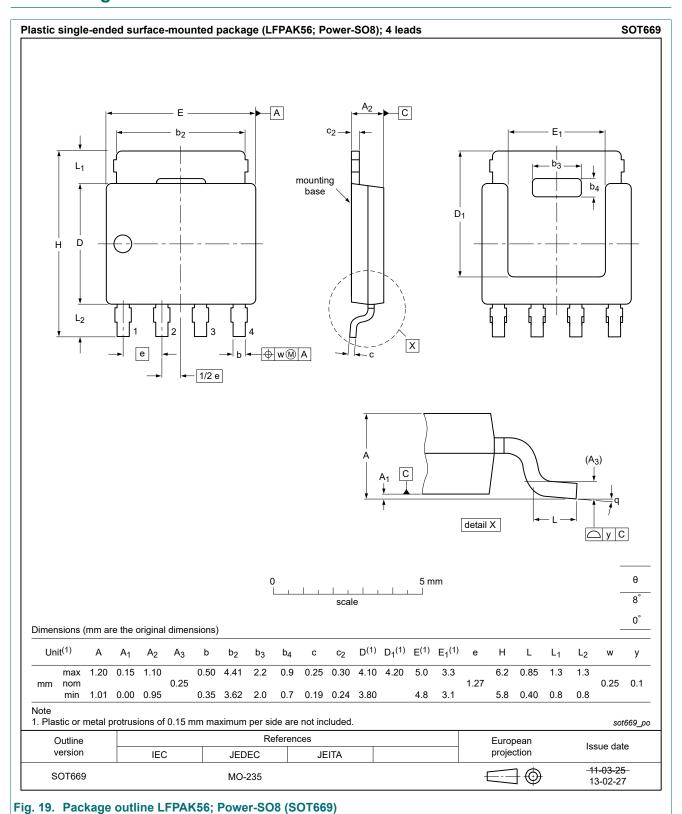
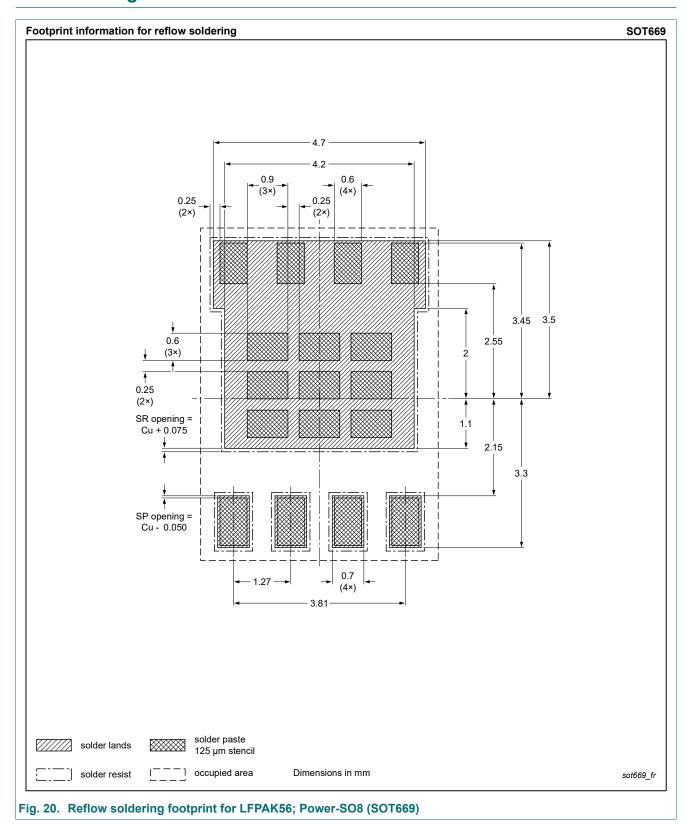


Fig. 18. Reverse recovery timing definition

# 11. Package outline



# 12. Soldering



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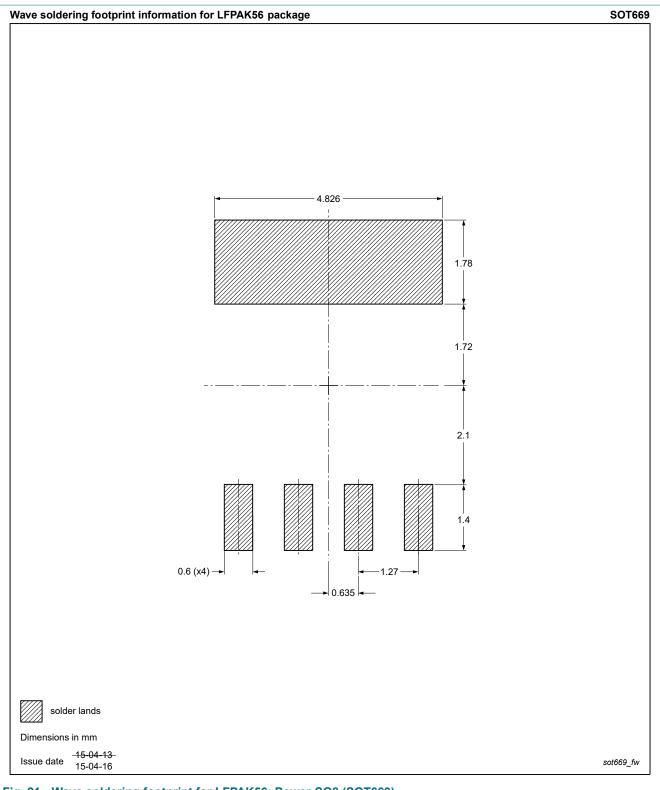


Fig. 21. Wave soldering footprint for LFPAK56; Power-SO8 (SOT669)

**Product data sheet** 

## 13. Legal information

#### **Data sheet status**

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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