

PESD5V0S2UAT

Double ESD protection diode in SOT23 package

pril 2023 Product data sheet

1. General description

Unidirectional double ESD protection diode in common cathode configuration in a small SOT23 Surface-Mounted Device (SMD) plastic package, designed to protect up to two data lines against damage from ElectroStatic Discharge (ESD) and other transients.

2. Features and benefits

- · Unidirectional ESD protection of up to two lines
- · Common-cathode configuration
- Max. peak pulse power: P_{PPM} = 260 W at t_p = 8/20 μs
- Ultra-low reverse leakage current: I_{RM} = 100 nA
- · ESD protection: 30 kV
- IEC 61000-4-2; level 4 (ESD)
- IEC 61000-4-5 (surge); I_{PPM} = 15 A at t_p = 8/20 μs

3. Applications

- · Computers and peripherals
- · Communication systems
- · Audio and video equipment
- Data lines
- CAN bus protection

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _j = 25 °C	[1]	-	-	5	V
C _d	diode capacitance	$f = 1 \text{ MHz}; V_R = 0 \text{ V}; T_j = 25 \text{ °C}$	[1]	-	152	200	pF

[1] Measured across either pins 1 and 3 or pins 2 and 3.



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A1	anode (diode 1)	3	
2	A2	anode (diode 2)		1——————————————————————————————————————
3	CC	common cathode	SOT23	3 sym002

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD5V0S2UAT	SOT23	plastic, surface-mounted package; 3 terminals; 1.9 mm pitch; 2.9 mm x 1.3 mm x 1 mm body	SOT23

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PESD5V0S2UAT	%7B

[1] % = placeholder for manufacturing site code

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
P _{PPM}	rated peak pulse power	t _p = 8/20 μs	[1] [2]	-	260	W
I _{PPM}	rated peak pulse current		[1] [2]	-	15	Α
T _j	junction temperature			-	150	°C
T _{amb}	ambient temperature			-65	150	°C
T _{stg}	storage temperature			-65	150	°C
ESD maximu	um ratings					
V _{ESD}	electrostatic discharge	IEC 61000-4-2; contact discharge	[3] [2]	-	30	kV
	voltage	IEC 61000-4-2; air discharge		-	15	kV
		MIL-STD-883; human body model (HBM)	[3] [2]	-	10	kV

- [1] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.
- [2] Measured across either pins 1 and 3 or pins 2 and 3.
- [3] Device stressed with ten non-repetitive ESD pulses.

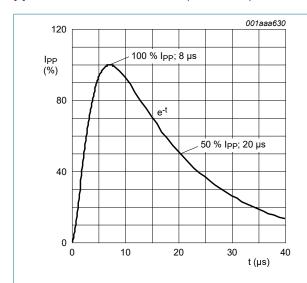


Fig. 1. 8/20 µs pulse waveform according to IEC 61000-4-5

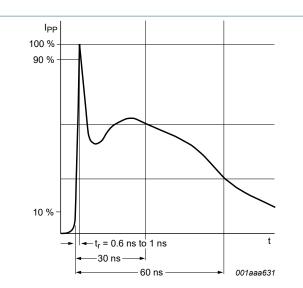


Fig. 2. ESD pulse waveform according to IEC 61000-4-2

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9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V_{RWM}	reverse standoff voltage	T _j = 25 °C	[1]	-	-	5	V
V_{BR}	breakdown voltage	$I_R = 5 \text{ mA}; T_j = 25 \text{ °C}$	[1]	6.4	6.8	7.2	V
I _{RM}	reverse leakage current	V _{RWM} = 5 V; T _j = 25 °C	[1]	-	0.1	1	μA
C _d	diode capacitance	$f = 1 \text{ MHz; } V_R = 0 \text{ V; } T_j = 25 ^{\circ}\text{C}$	[1]	-	152	200	pF
V _{CL}	clamping voltage	I _{PP} = 1 A; T _j = 25 °C	[2] [1]	-	-	9	V
		I _{PPM} = 15 A; T _j = 25 °C	[2] [1]	-	-	20	V
R _{diff}	differential resistance	I _R = 1 mA; T _j = 25 °C	[1]	-	-	80	Ω

- [1] Measured across either pins 1 and 3 or pins 2 and 3.
- [2] Non-repetitive current pulse 8/20 µs exponential decay waveform according to IEC 61000-4-5.

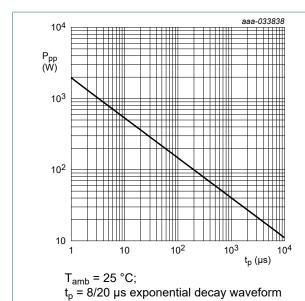


Fig. 3. Peak pulse power dissipation as a function of pulse time; typical values

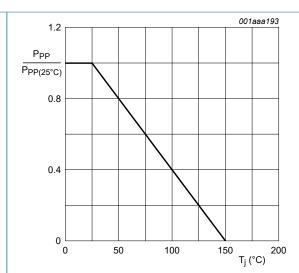


Fig. 4. Relative variation of peak pulse power as a function of junction temperature; typical values

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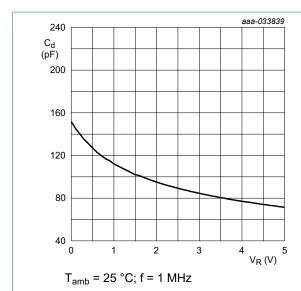


Fig. 5. Diode capacitance as a function of reverse voltage; typical values

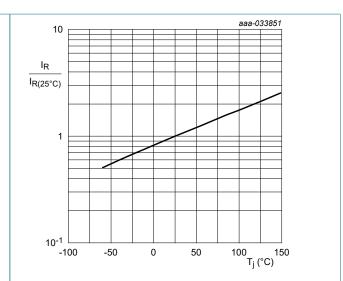
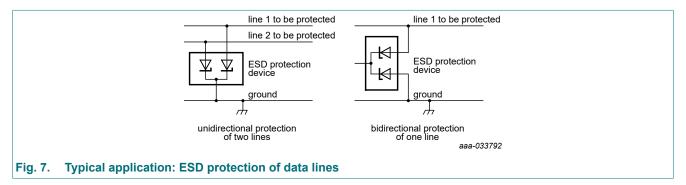


Fig. 6. Relative variation of reverse leakage current as a function of junction temperature; typical values

10. Application information

The device can protect up to two lines against damage caused by unidirectional ElectroStatic Discharge (ESD) and surge pulses. The device can protect lines whose signal polarities are below ground.



Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

- 1. Place the device as close to the input terminal or connector as possible.
- 2. Minimize the path length between the device and the protected line.
- 3. Keep parallel signal paths to a minimum.
- 4. Avoid running protected conductors in parallel with unprotected conductors.
- 5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
- 6. Minimize the length of the transient return path to ground.
- 7. Avoid using shared transient return paths to a common ground point.
- 8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

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11. Package outline

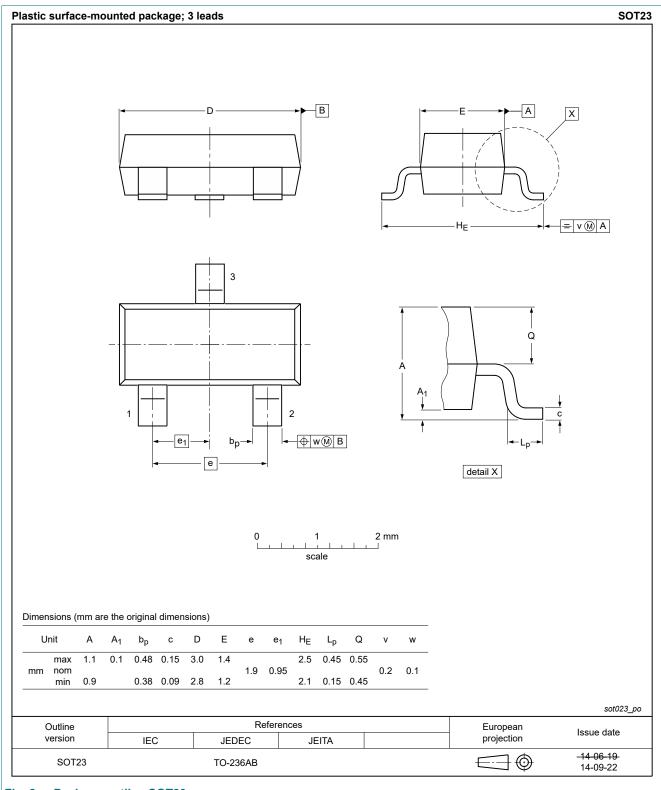
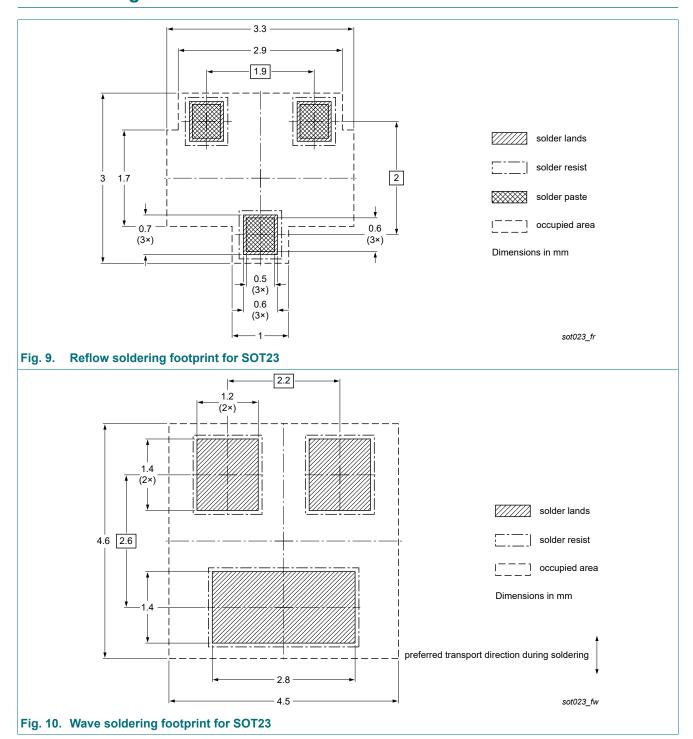


Fig. 8. Package outline SOT23

12. Soldering



13. Revision history

Table 7. Revision history

Table 1. Revision misto	'i y			
Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD5V0S2UAT v.2	20230401	Product data sheet	-	PESD5V0S2UAT v.1
Modifications:	Nexperia Legal texts have bee Family data sheet re	ta sheet has been redesion adapted to the new corduced to single type data standard qualification. Ple	mpany name where appro	opriate
PESDxS2UAT series v.1	20040218	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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