



# BAT54QC

Schottky barrier diode

27 November 2020

Product data sheet

## 1. General description

Planar Schottky barrier diode encapsulated in an ultra small DFN1412D-3 (SOT8009, JEDEC MO340-CA) leadless Surface-Mounted Device (SMD) plastic package with side-wettable flanks.

## 2. Features and benefits

- Low forward voltage
- Low capacitance
- Leadless ultra small SMD plastic package
- Low package height of 0.5 mm
- Suitable for Automatic Optical Inspection (AOI) of solder joint
- AEC-Q101 qualified

## 3. Applications

- Ultra high-speed switching
- Voltage clamping
- Protection circuits

## 4. Quick reference data

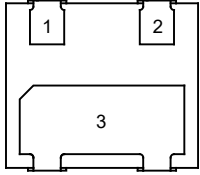
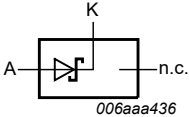
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$V_R$	reverse voltage			-	-	30	V
$V_F$	forward voltage	$I_F = 100 \text{ mA}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	800	mV
$I_R$	reverse current	$V_R = 25 \text{ V}$ ; $T_{\text{amb}} = 25 \text{ }^\circ\text{C}$	[1]	-	-	2	$\mu\text{A}$

[1] Pulse test:  $t_p \leq 300 \text{ } \mu\text{s}$ ;  $\delta \leq 0.02$

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	A	anode	 <p>Bottom view DFN1412D-3 (SOT8009)</p>	
2	n.c.	not connected		
3	K	cathode		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BAT54QC	DFN1412D-3	plastic, leadless extremely thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body	SOT8009

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BAT54QC	9B

## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_R$	reverse voltage			-	30	V
$I_F$	forward current	$T_{amb} \leq 25\text{ °C}$		-	200	mA
$I_{FRM}$	repetitive peak forward current	$t_p \leq 1\text{ s}$ ; $\delta \leq 0.5$ ; $T_{amb} = 25\text{ °C}$		-	300	mA
$I_{FSM}$	non-repetitive peak forward current	square-wave pulse; $t_p \leq 10\text{ ms}$ ; $T_{j(init)} = 25\text{ °C}$		-	600	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	[1]	-	415	mW
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C

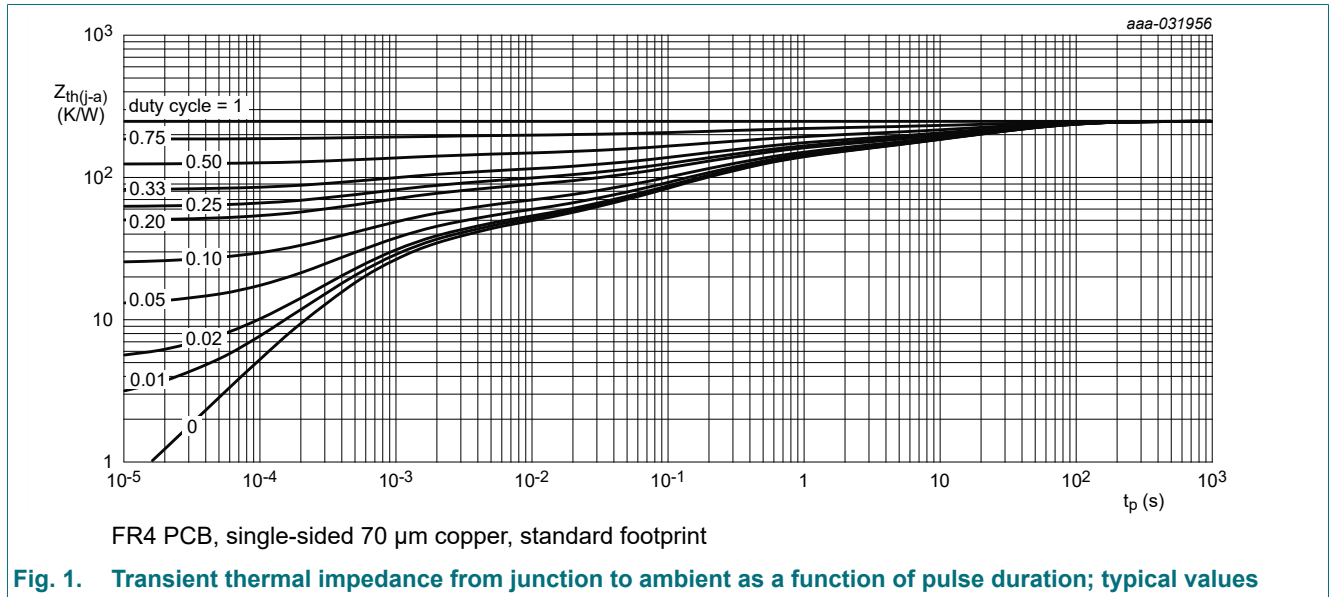
[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided 70 µm copper, tin-plated and standard footprint.

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1] [2]	-	-	290	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided 70  $\mu\text{m}$  copper, tin-plated and standard footprint.
- [2] For Schottky barrier diodes thermal runaway has to be considered, as in some applications the reverse power losses PR are a significant part of the total power losses.

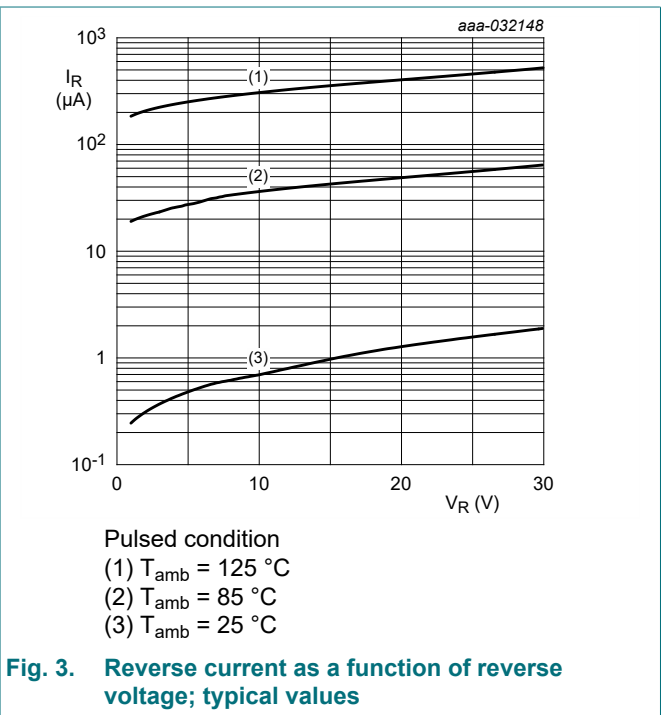
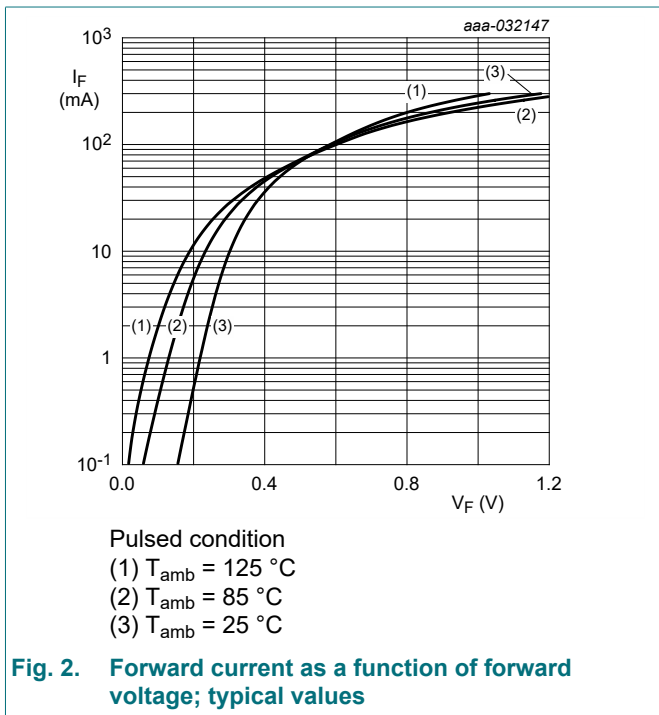


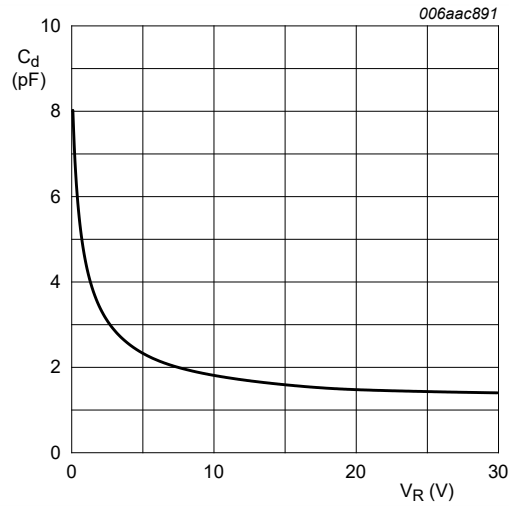
## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
V <sub>F</sub>	forward voltage	I <sub>F</sub> = 0.1 mA; T <sub>amb</sub> = 25 °C	[1]	-	-	240	mV
		I <sub>F</sub> = 1 mA; T <sub>amb</sub> = 25 °C	[1]	-	-	320	mV
		I <sub>F</sub> = 10 mA; T <sub>amb</sub> = 25 °C	[1]	-	-	400	mV
		I <sub>F</sub> = 30 mA; T <sub>amb</sub> = 25 °C	[1]	-	-	500	mV
		I <sub>F</sub> = 100 mA; T <sub>amb</sub> = 25 °C	[1]	-	-	800	mV
I <sub>R</sub>	reverse current	V <sub>R</sub> = 25 V; T <sub>amb</sub> = 25 °C	[1]	-	-	2	μA
C <sub>d</sub>	diode capacitance	V <sub>R</sub> = 1 V; f = 1 MHz; T <sub>amb</sub> = 25 °C	-	-	-	10	pF
t <sub>rr</sub>	reverse recovery time	I <sub>F</sub> = 10 mA; I <sub>R</sub> = 10 mA; R <sub>L</sub> = 100 Ω; I <sub>R(meas)</sub> = 1 mA; T <sub>amb</sub> = 25 °C	-	-	-	5	ns

[1] Pulse test: t<sub>p</sub> ≤ 300 μs; δ ≤ 0.02

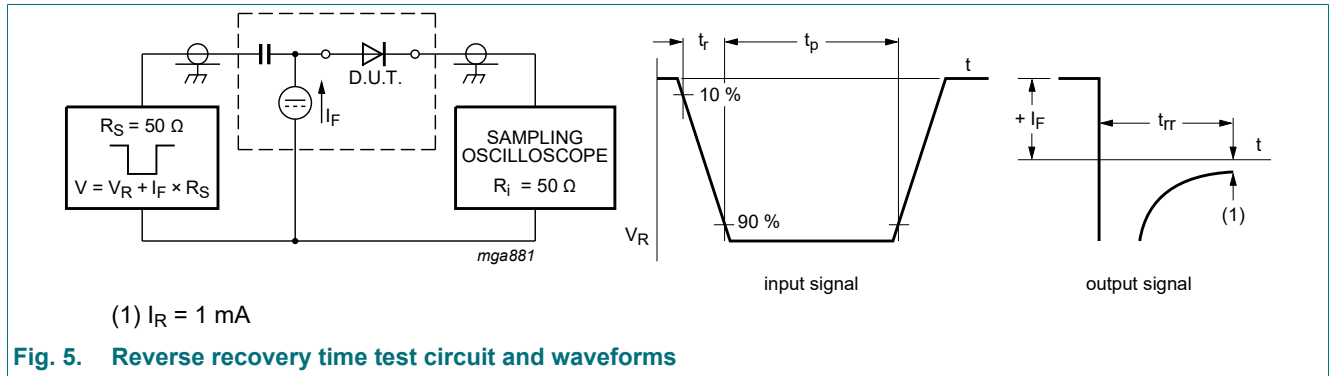




$T_{amb} = 25\text{ °C}; f = 1\text{ MHz}$

**Fig. 4. Diode capacitance as a function of reverse voltage; typical values**

### 11. Test information



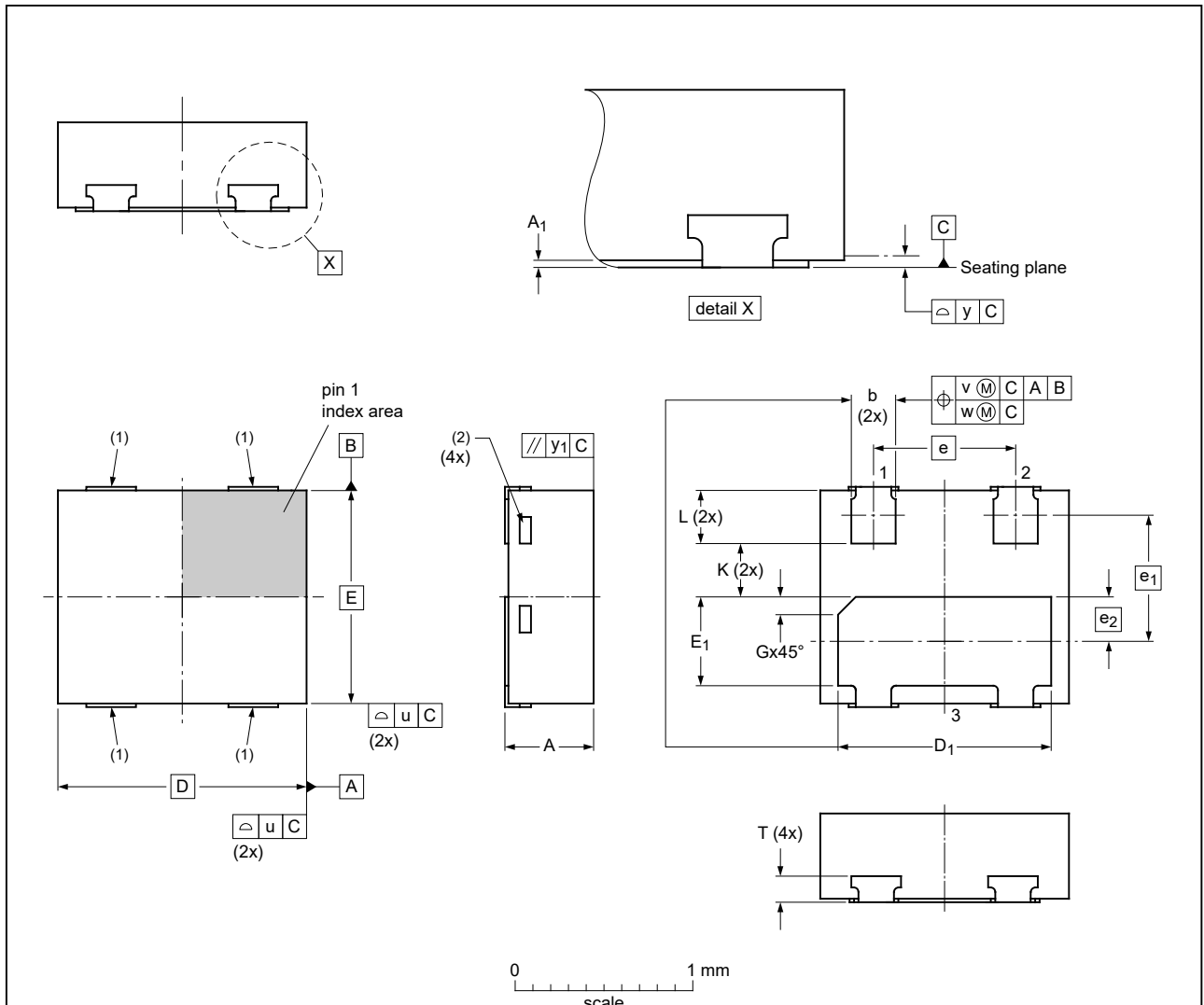
#### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

DFN1412D-3: plastic, leadless extremely thin small outline package with side-wettable flanks (SWF); 3 terminals; 0.8 mm pitch; 1.4 mm x 1.2 mm x 0.48 mm body

SOT8009



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	D	D <sub>1</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	e <sub>2</sub>	G	K	L	T	u	v	w	y	y <sub>1</sub>
max	0.50	0.04	0.30	1.25	0.55								0.35	0.22					
nom	0.47		0.25	1.4	1.20	1.2	0.50	0.8	0.71	0.26	0.09		0.30	0.16	0.05	0.1	0.05	0.05	0.05
min	0.44		0.22	1.17	0.47						(ref)	0.25	0.27	0.10					

Note

- Side Wettable Flank, protrusion max. 0.02 mm.
  - Visible depend upon used manufacturing technology.
- Dimension A and T are including plating thickness.

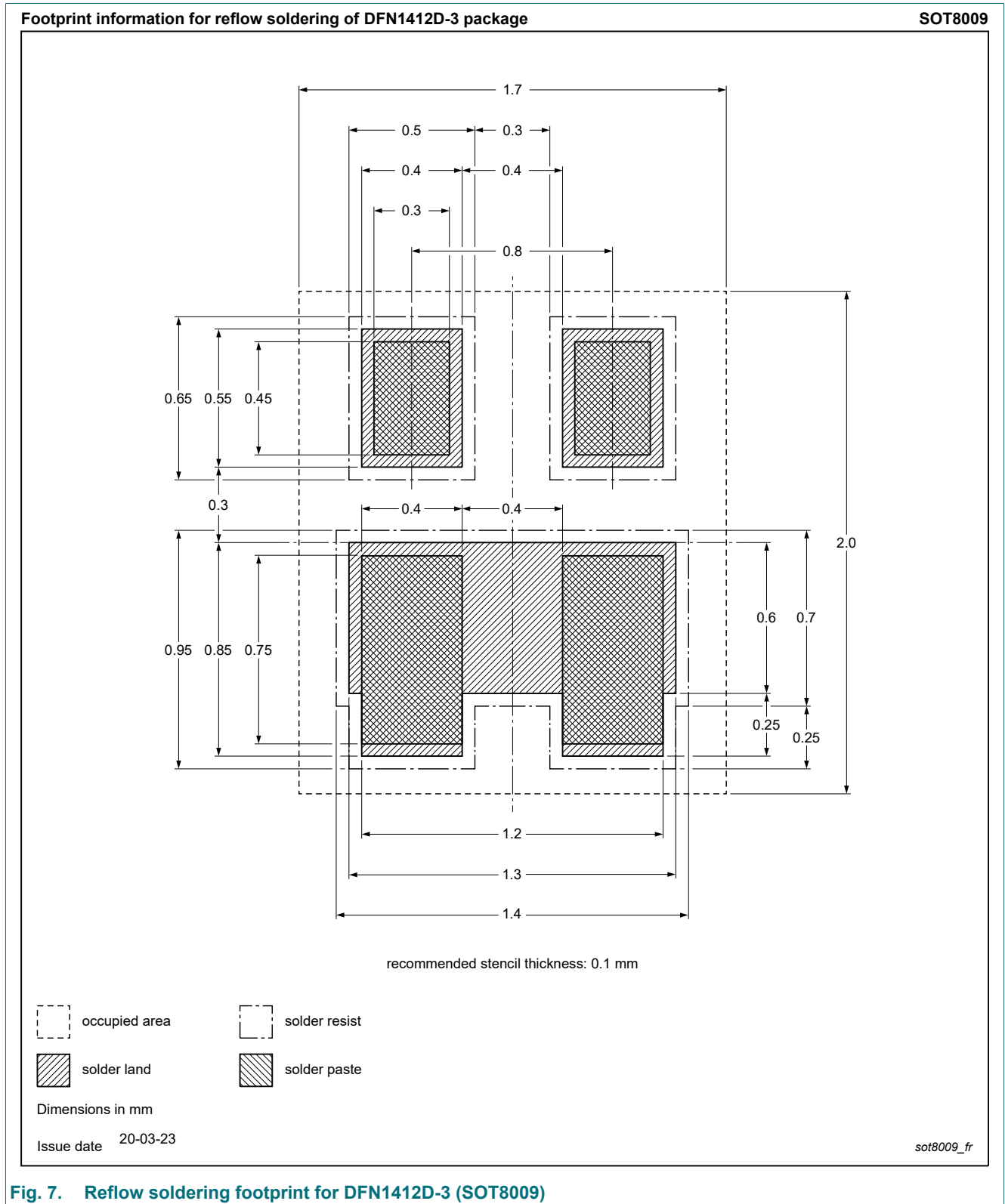
sot8009\_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT8009		MO-340CA				19-12-04 19-12-06

Fig. 6. Package outline DFN1412D-3 (SOT8009)



### 13. Soldering



**Fig. 7. Reflow soldering footprint for DFN1412D-3 (SOT8009)**

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BAT54QC v.1	20201127	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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