



BUK6Y61-60P

60 V, P-channel Trench MOSFET

16 March 2020

Product data sheet

1. General description

P-channel enhancement mode MOSFET in an LFPK56 (Power SO8) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

This product has been designed and qualified to AEC-Q101 standard for use in high-performance automotive applications such as reverse battery protection.

2. Features and benefits

- High thermal power dissipation capability
- Suitable for thermally demanding environments due to 175 °C rating
- Trench MOSFET technology
- AEC-Q101 qualified

3. Applications

- Reverse battery protection
- Power management
- High-side loadswitch
- Motor drive

4. Quick reference data

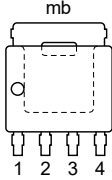
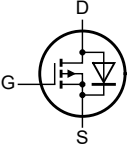
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$		-	-	-60	V
V_{GS}	gate-source voltage		[1]	-20	-	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$		-	-	-25	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$		-	-	66	W
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -10\text{ V}; I_D = -4.7\text{ A}; T_j = 25\text{ °C}$		-	48	61	mΩ

[1] $V_{GS} = -20\text{ V}/+5\text{ V}$ according AEC-Q101 at $T_j = 175\text{ °C}$; $V_{GS} = -20\text{ V}/+20\text{ V}$ according AEC-Q101 at $T_j = 150\text{ °C}$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LFPAK56; Power-SO8 (SOT669)	 017aaa094
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK6Y61-60P	LFPAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK6Y61-60P	6Y6160P

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	[1]	-	-60	V
V_{GS}	gate-source voltage			-20	20	V
I_D	drain current	$V_{GS} = -10\text{ V}; T_{mb} = 25\text{ °C}$		-	-25	A
		$V_{GS} = -10\text{ V}; T_{mb} = 100\text{ °C}$		-	-17.7	A
I_{DM}	peak drain current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$		-	-100	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$		-	66	W
T_j	junction temperature			-55	175	°C
T_{amb}	ambient temperature			-55	175	°C
T_{stg}	storage temperature			-65	175	°C
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$		-	-25	A
I_{SM}	peak source current	single pulse; $t_p \leq 10\text{ }\mu\text{s}; T_{mb} = 25\text{ °C}$		-	-100	A
ESD maximum rating						
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	800	V
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$T_{j(\text{init})} = 25\text{ °C}; I_D = -4.6\text{ A}; \text{DUT in avalanche (unclamped)}$		-	61	mJ

[1] $V_{GS} = -20\text{ V}/+5\text{ V}$ according AEC-Q101 at $T_j = 175\text{ °C}$; $V_{GS} = -20\text{ V}/+20\text{ V}$ according AEC-Q101 at $T_j = 150\text{ °C}$

[2] Measured between all pins.

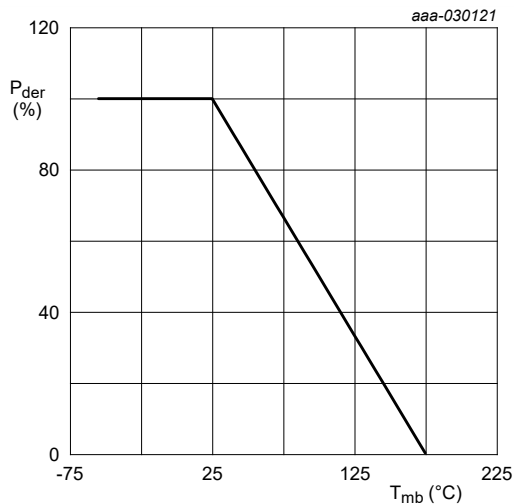


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

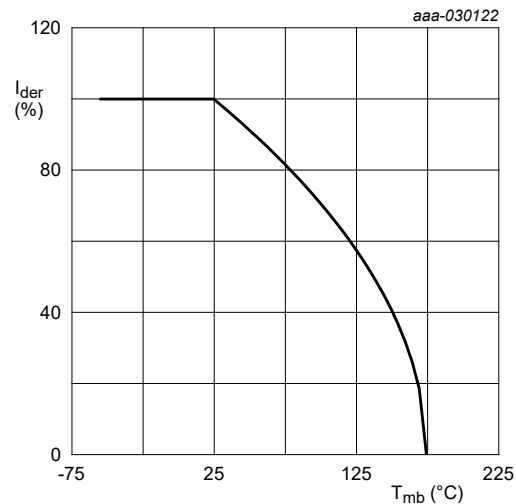
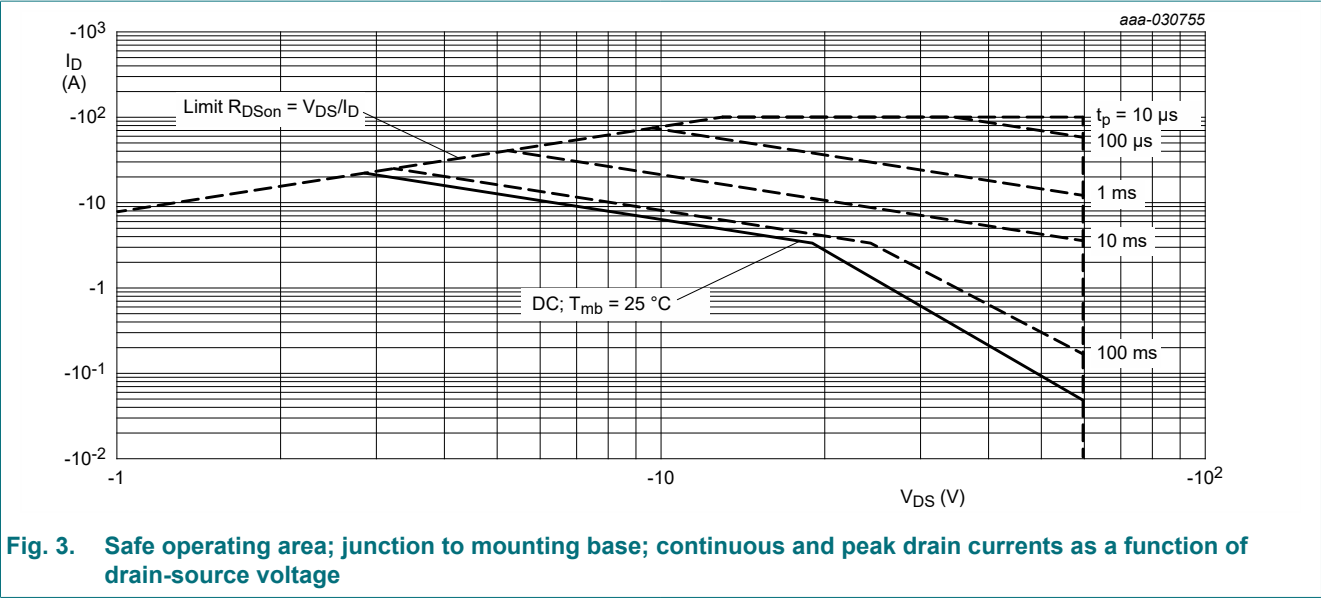


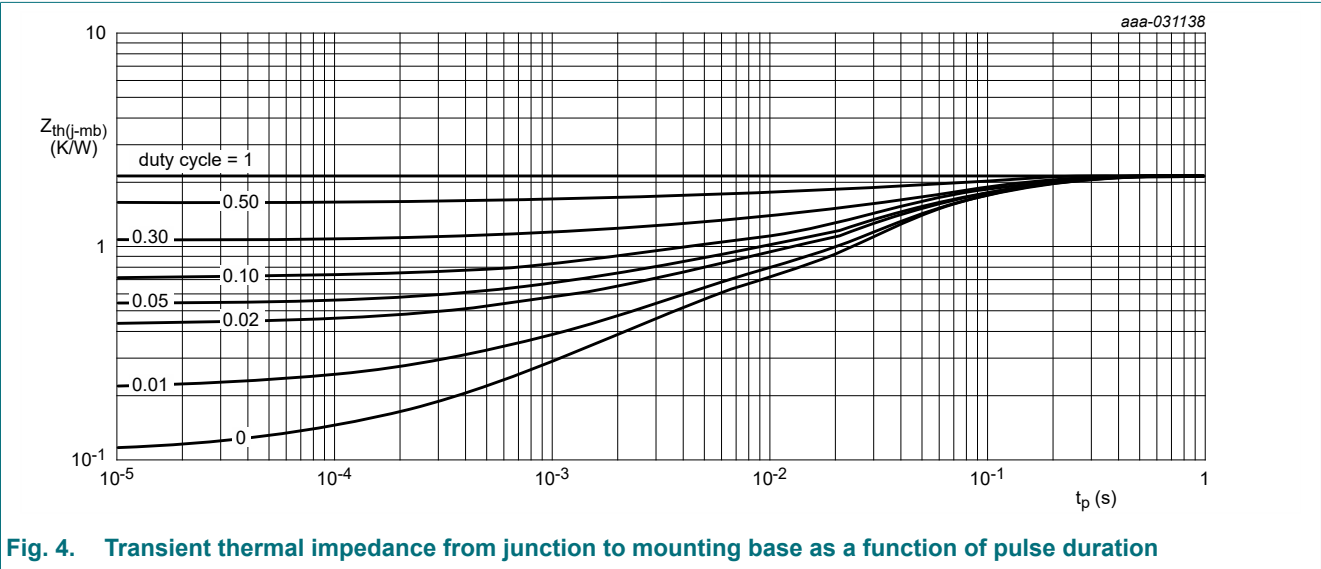
Fig. 2. Normalized continuous drain current as a function of mounting base temperature



9. Thermal characteristics

Table 6. Thermal characteristics

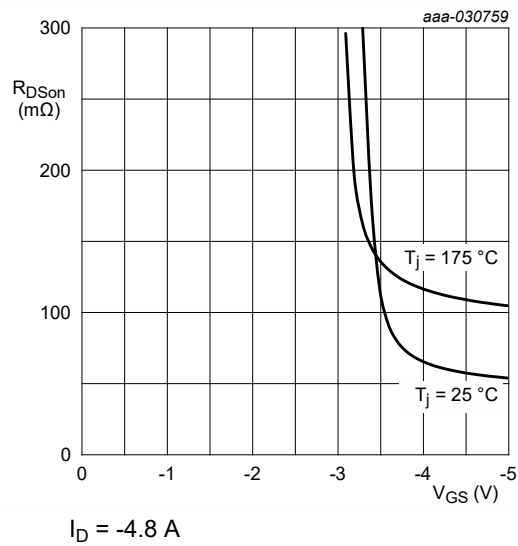
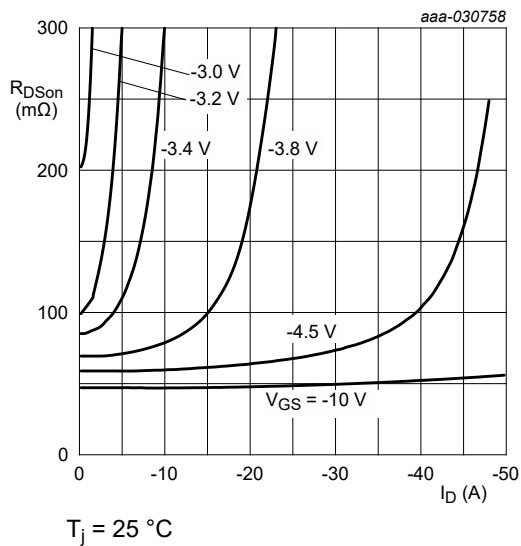
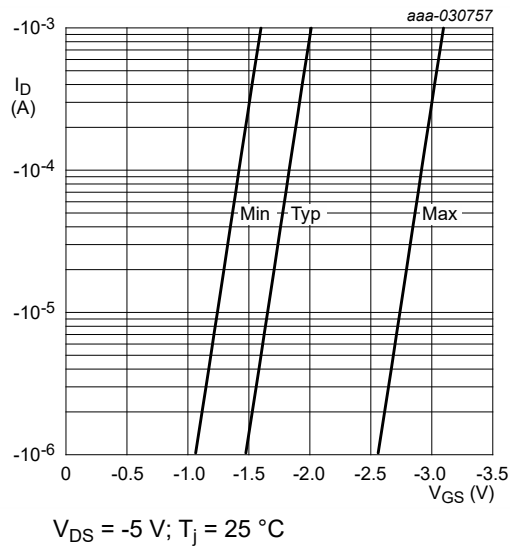
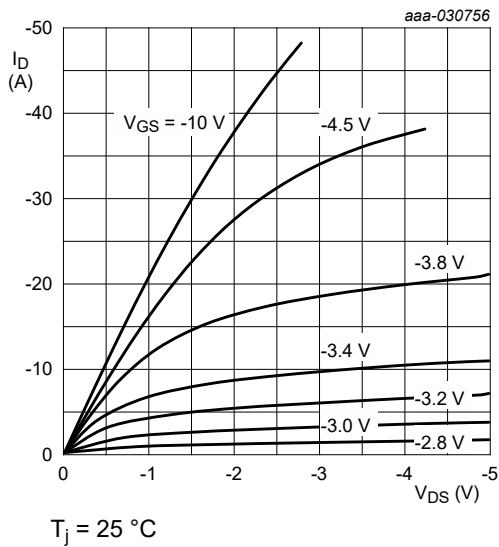
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base		-	1.8	2.3	K/W



10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
V _{(BR)DSS}	drain-source breakdown voltage	I _D = -250 μA; V _{GS} = 0 V; T _j = 25 °C		-60	-	-	V
V _{GSth}	gate-source threshold voltage	I _D = -250 μA; V _{DS} =V _{GS} ; T _j = 25 °C		-1.5	-2	-3	V
I _{DSS}	drain leakage current	V _{DS} = -60 V; V _{GS} = 0 V; T _j = 25 °C		-	-	-1	μA
		V _{DS} = -60 V; V _{GS} = 0 V; T _j = 125 °C		-	-	-10	μA
I _{GSS}	gate leakage current	V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	-100	nA
		V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C		-	-	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = -10 V; I _D = -4.7 A; T _j = 25 °C		-	48	61	mΩ
		V _{GS} = -10 V; I _D = -4.7 A; T _j = 175 °C		-	100	130	mΩ
		V _{GS} = -4.5 V; I _D = -3.8 A; T _j = 25 °C		-	62	93	mΩ
g _{fs}	forward transconductance	V _{DS} = -10 V; I _D = -4 A; T _j = 25 °C		-	65	-	S
R _G	gate resistance	f = 1 MHz; T _j = 25 °C		-	12	-	Ω
Dynamic characteristics							
Q _{G(tot)}	total gate charge	V _{DS} = -30 V; I _D = -4.7 A; V _{GS} = -10 V; T _j = 25 °C		-	20	30	nC
Q _{GS}	gate-source charge			-	3.3	-	nC
Q _{GD}	gate-drain charge			-	4.3	-	nC
C _{iss}	input capacitance	V _{DS} = -30 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C		-	1060	-	pF
C _{oss}	output capacitance			-	85	-	pF
C _{rss}	reverse transfer capacitance			-	49	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -30 V; I _D = -4.7 A; V _{GS} = -10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C		-	12	-	ns
t _r	rise time			-	58	-	ns
t _{d(off)}	turn-off delay time			-	21	-	ns
t _f	fall time			-	204	-	ns
Source-drain diode							
V _{SD}	source-drain voltage	I _S = -22.4 A; V _{GS} = 0 V; T _j = 25 °C		-	-0.7	-1.2	V
t _{rr}	reverse recovery time	I _S = -22.4 A; dI _S /dt = 100 A/μs;		-	30	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = -30 V; T _j = 25 °C		-	37	-	nC



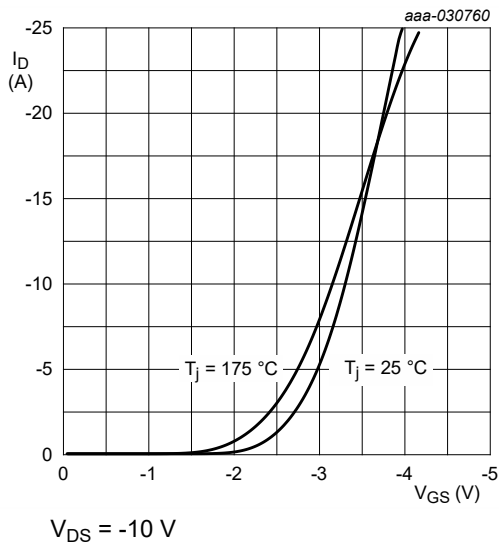


Fig. 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values

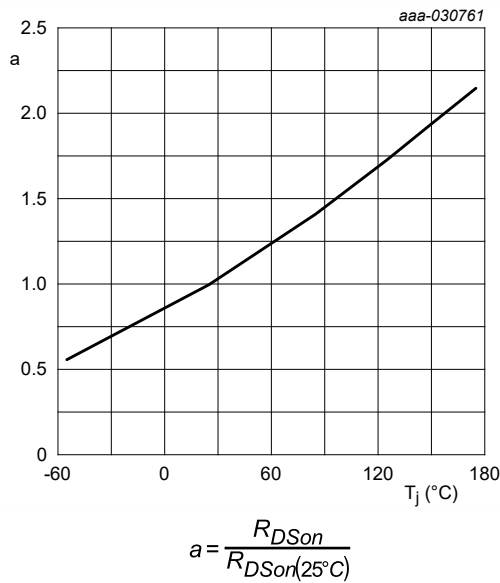


Fig. 10. Normalized drain-source on-state resistance as a function of junction temperature; typical values

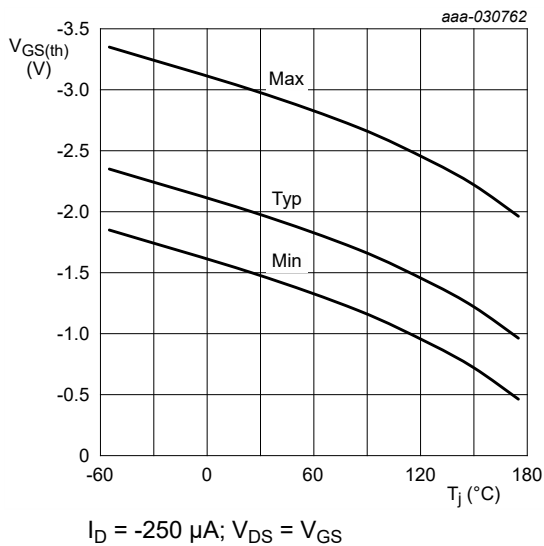


Fig. 11. Gate-source threshold voltage as a function of junction temperature

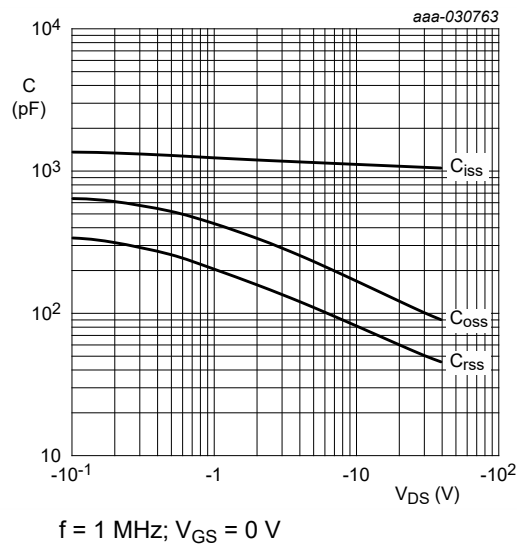
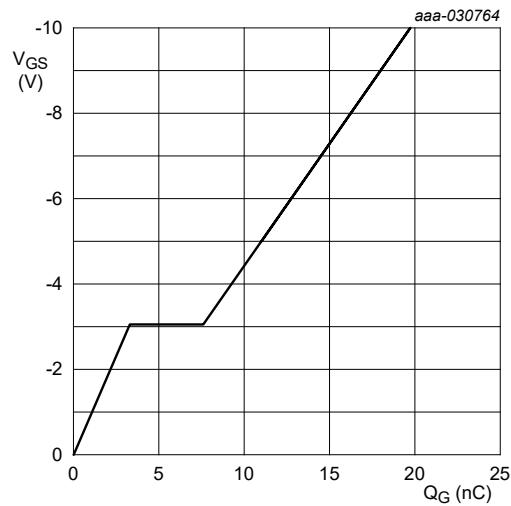


Fig. 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{DS} = -30\text{ V}$; $I_D = -4.8\text{ A}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values

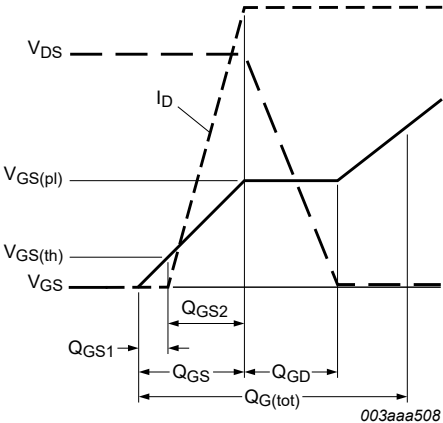
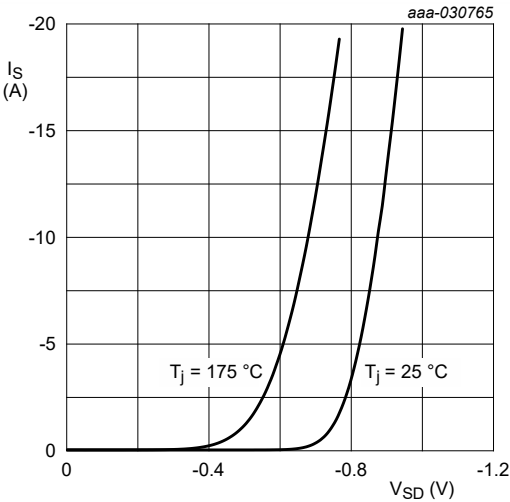


Fig. 14. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 15. Source current as a function of source-drain voltage; typical values

11. Test information

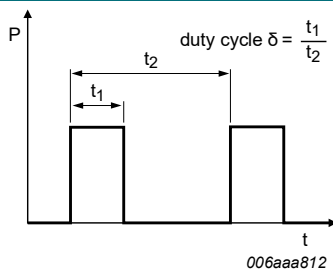


Fig. 16. Duty cycle definition

Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

12. Package outline

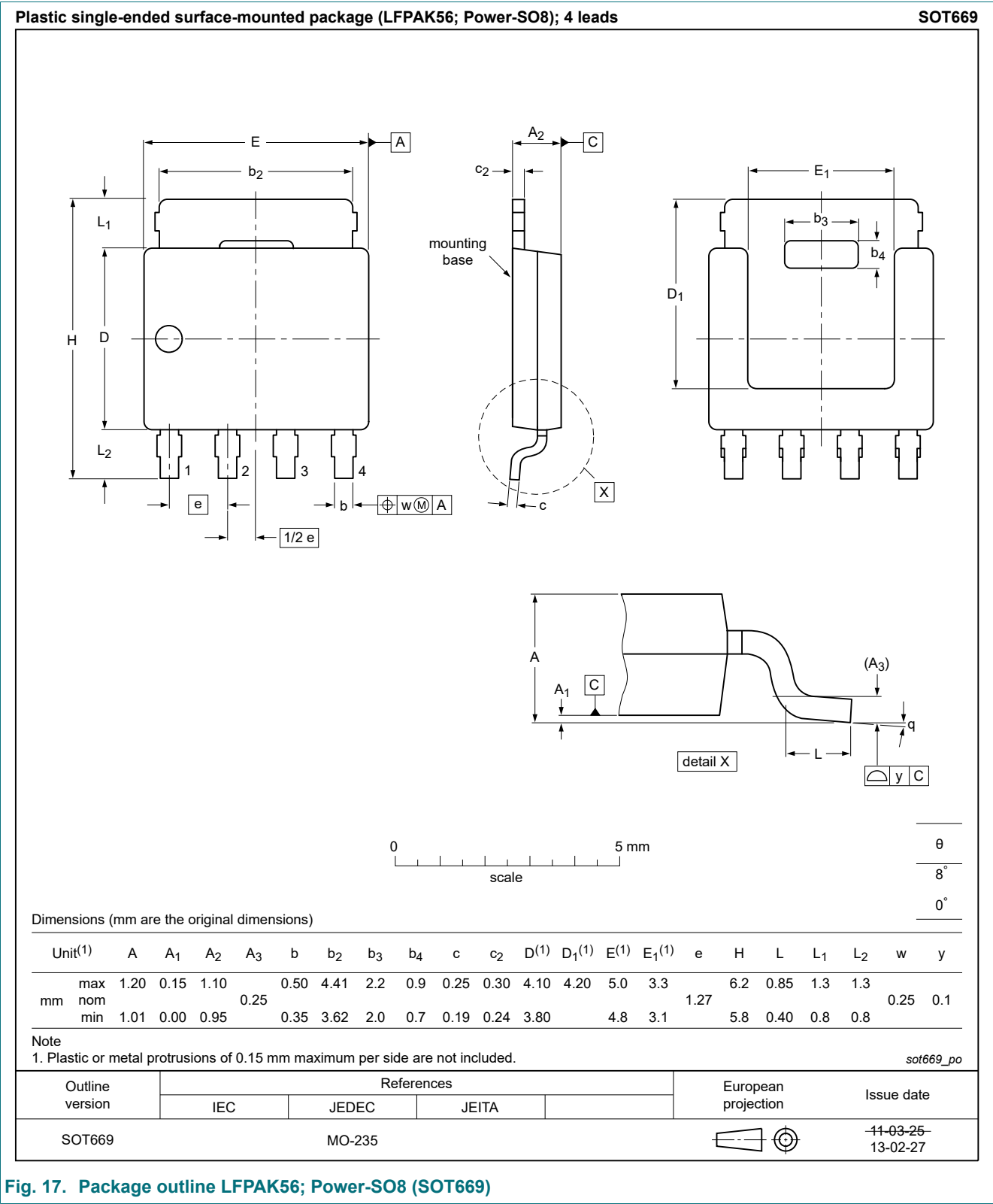


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

13. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
BUK6Y61-60P v.1	20200316	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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