PUMD9

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

1 July 2022 **Product data sheet**

1. General description

NPN/PNP Resistor-Equipped double Transistor (RET) in a very small SOT363 (SC-88) Surface-Mounted Device (SMD) plastic package.

NPN/NPN complement: PUMH9

PNP/PNP complement: PUMB9

2. Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs

3. Applications

- Digital application in automotive and industrial segments
- Cost-saving alternative for BC847/BC857 series in digital applications
- Controlling IC inputs
- Switching loads

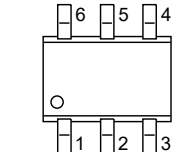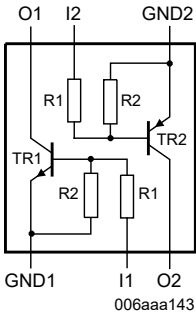## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
V_{CEO}	collector-emitter voltage	open base		-	-	50	V
I_O	output current			-	-	100	mA
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	

[1] See "Section 11: Test information" for resistor calculation and test conditions.

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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	GND1	GND (emitter) TR1		
2	I1	input (base) TR1		
3	O2	output (collector) TR2		
4	GND2	GND (emitter) TR2	**TSSOP6 (SOT363)**	
5	I2	input (base) TR2		
6	O1	output (collector) TR1		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	**Description**	**Version**
PUMD9	TSSOP6	plastic, surface-mounted package; 6 leads; 0.65 mm pitch; 2.1 mm x 1.25 mm x 0.95 mm body	SOT363

7. Marking

Table 4. Marking codes

Type number	Marking code[1]
PUMD9	D%9

[1] % = placeholder for manufacturing site code

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8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
Per transistor, for the PNP transistor with negative polarity						
V_{CBO}	collector-base voltage	open emitter		-	50	V
V_{CEO}	collector-emitter voltage	open base		-	50	V
V_{EBO}	emitter-base voltage	open collector		-	6	V
V_I	input voltage	input voltage TR1		-	40	V
				-	-6	V
		input voltage TR2		-	6	V
				-	-40	V
I_O	output current			-	100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	200	mW
Per device						
P_{tot}	total power dissipation	$T_{amb} \leq 25$ °C	[1]	-	300	mW
T_j	junction temperature			-	150	°C
T_{amb}	ambient temperature			-65	150	°C
T_{stg}	storage temperature			-65	150	°C

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided, 35 μm copper, tin-plated and standard footprint.
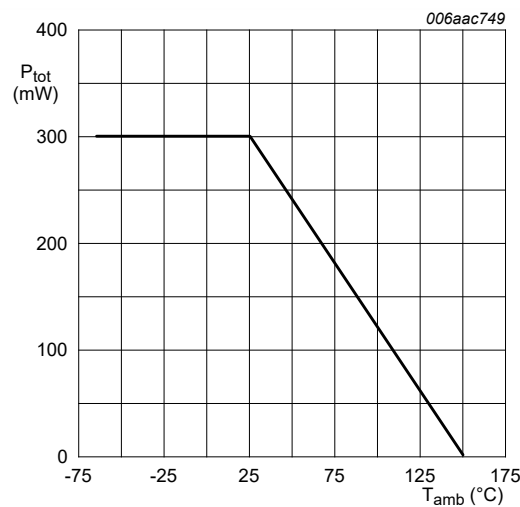
FR4 PCB, single-sided, 35 μm copper, tin-plated and standard footprint
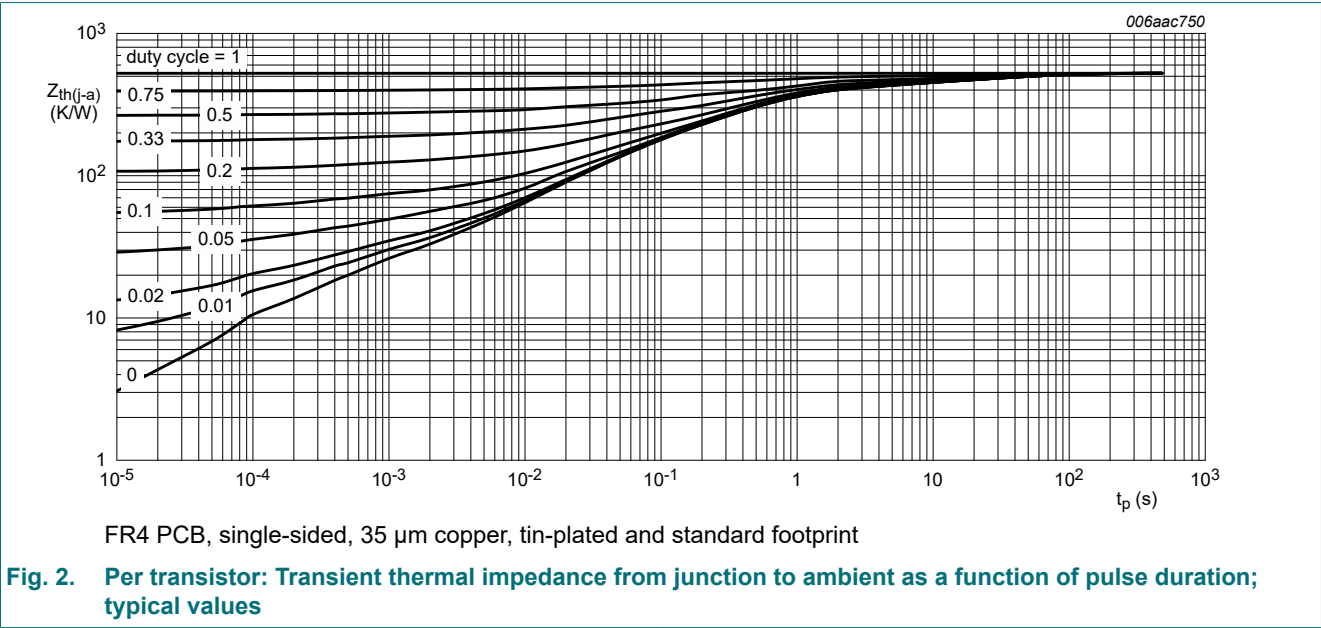
Fig. 1.   Per device: Power derating curve

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50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	625	K/W
Per device							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint.

FR4 PCB, single-sided, 35 µm copper, tin-plated and standard footprint

Fig. 2.   Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Per transistor, for the PNP transistor with negative polarity							
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 100 µA; I_E = 0 A; T_{amb} = 25 °C		50	-	-	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 2 mA; I_B = 0 A; T_{amb} = 25 °C		50	-	-	V
I_{CBO}	collector-base cut-off current	V_{CB} = 50 V; I_E = 0 A; T_{amb} = 25 °C		-	-	100	nA
I_{CEO}	collector-emitter cut-off current	V_{CE} = 30 V; I_B = 0 A; T_{amb} = 25 °C		-	-	100	nA
		V_{CE} = 30 V; I_B = 0 A; T_j = 150 °C		-	-	5	µA
I_{EBO}	emitter-base cut-off current	V_{EB} = 5 V; I_C = 0 mA; T_{amb} = 25 °C		-	-	150	µA
h_{FE}	DC current gain	V_{CE} = 5 V; I_C = 5 mA; T_{amb} = 25 °C		100	-	-	
V_{CEsat}	collector-emitter saturation voltage	I_C = 5 mA; I_B = 0.25 mA; T_{amb} = 25 °C		-	-	100	mV
$V_{I(off)}$	off-state input voltage	V_{CE} = 5 V; I_C = 100 µA; T_{amb} = 25 °C		-	0.7	0.5	V
$V_{I(on)}$	on-state input voltage	V_{CE} = 0.3 V; I_C = 1 mA; T_{amb} = 25 °C		1.4	0.8	-	V
R1	bias resistor 1 (input)		[1]	7	10	13	kΩ
R2/R1	bias resistor ratio		[1]	3.7	4.7	5.7	
TR1 (NPN)							
C_c	collector capacitance	V_{CB} = 10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	2.5	pF
f_T	transition frequency	V_{CE} = 5 V; I_C = 10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	230	-	MHz
TR2 (PNP)							
C_c	collector capacitance	V_{CB} = -10 V; I_E = 0 A; i_e = 0 A; f = 1 MHz; T_{amb} = 25 °C		-	-	3	pF
f_T	transition frequency	V_{CE} = -5 V; I_C = -10 mA; f = 100 MHz; T_{amb} = 25 °C	[2]	-	180	-	MHz

[1]   See "Section 11: Test information" for resistor calculation and test conditions.
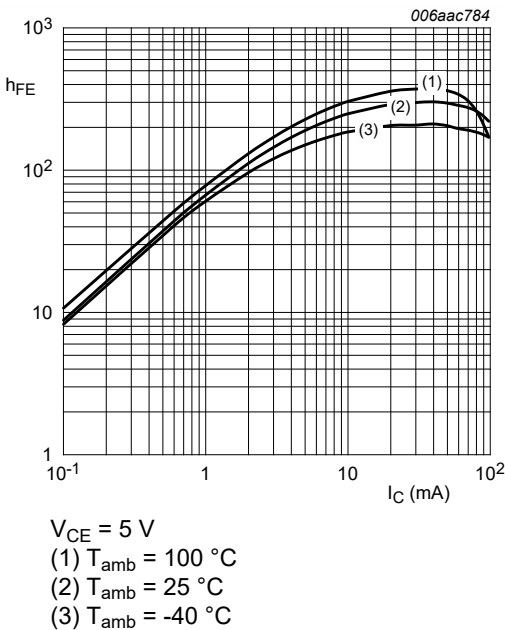[2]   Characteristics of built-in transistor

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50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

V_{CE} = 5 V
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 3. TR1 (NPN): DC current gain as a function of collector current; typical values

T_{amb} = 25 °C
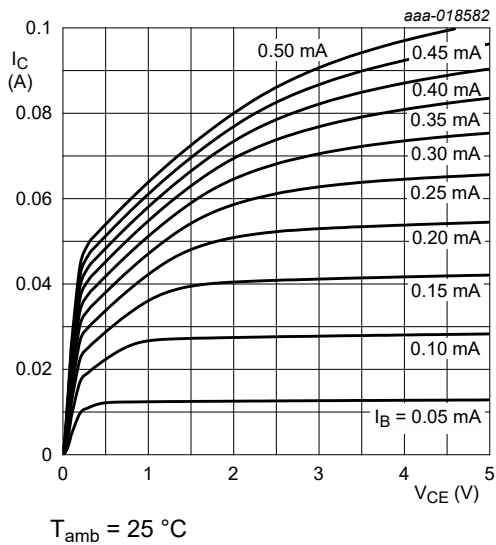
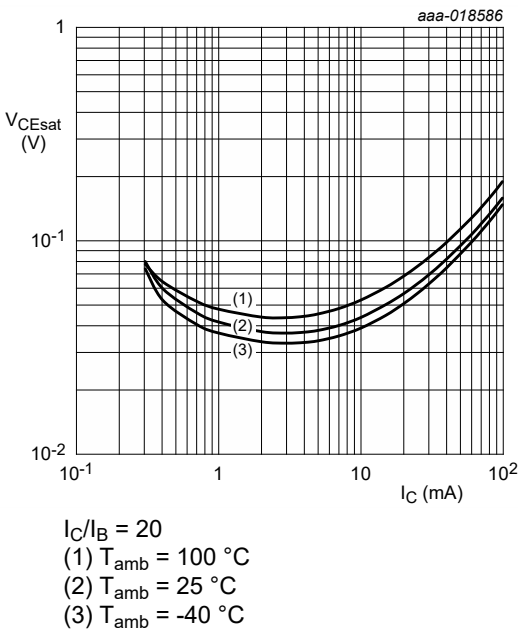**Fig. 4.** TR1 (NPN): Collector current as a function of collector-emitter voltage; typical values

I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values

V_{CE} = 0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
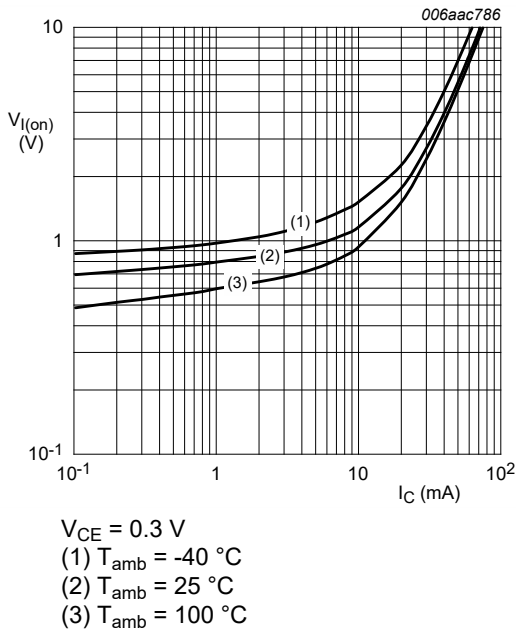
Fig. 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

V_{CE} = 5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
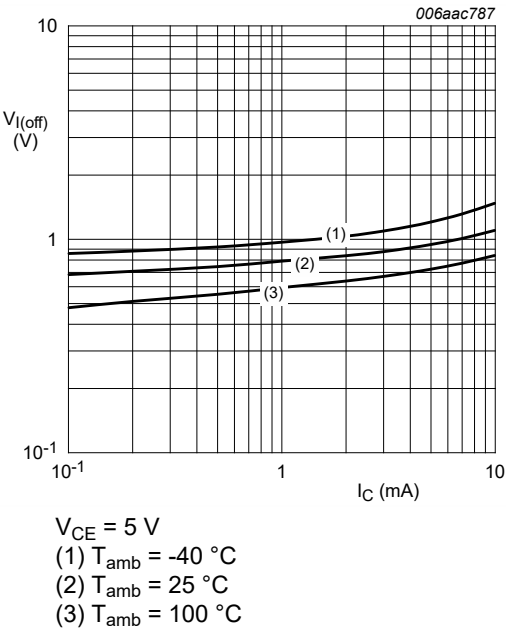
Fig. 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values

f = 1 MHz
T_{amb} = 25 °C
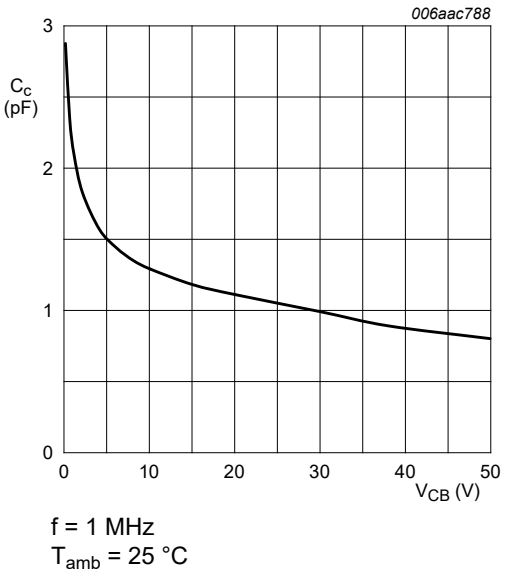
Fig. 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values
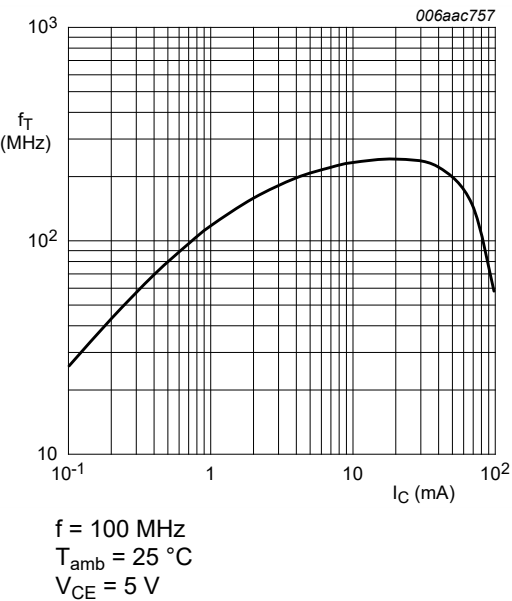

f = 100 MHz
T_{amb} = 25 °C
V_{CE} = 5 V

Fig. 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor

V_{CE} = -5 V
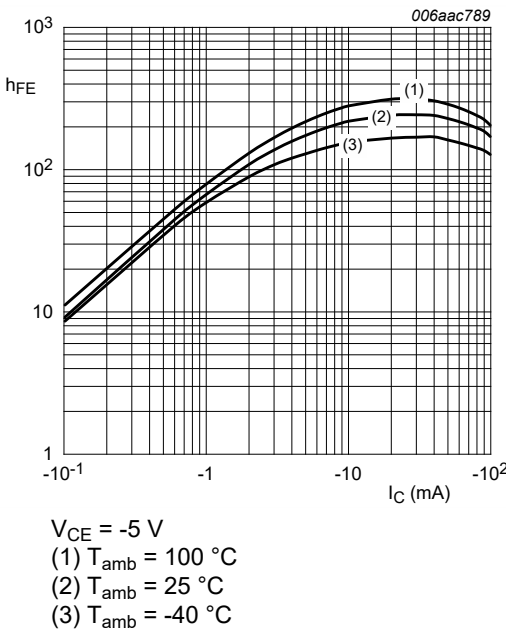(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C

Fig. 10. TR2 (PNP): DC current gain as a function of collector current; typical values

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50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ
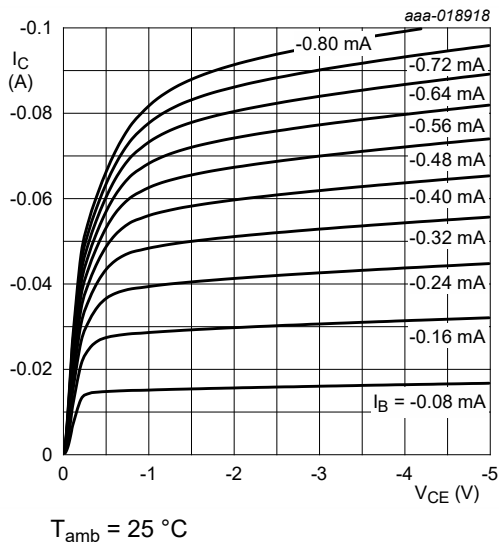
Fig. 11. TR2 (PNP): Collector current as a function of collector-emitter voltage; typical values

T_{amb} = 25 °C

I_C/I_B = 20
(1) T_{amb} = 100 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = -40 °C
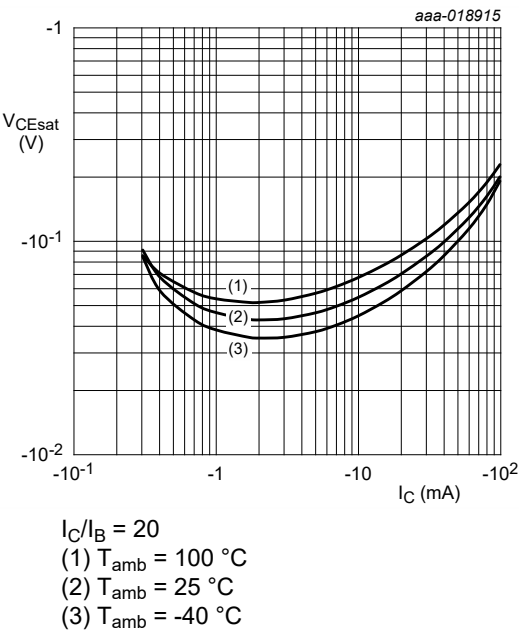
Fig. 12. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values

V_{CE} = -0.3 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
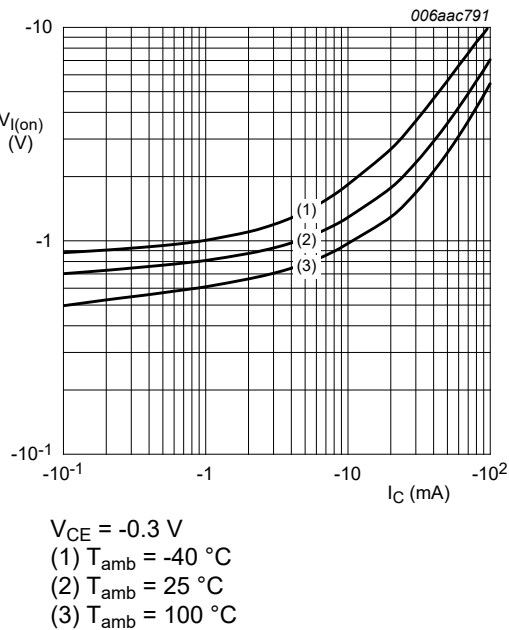
Fig. 13. TR2 (PNP): On-state input voltage as a function of collector current; typical values

V_{CE} = -5 V
(1) T_{amb} = -40 °C
(2) T_{amb} = 25 °C
(3) T_{amb} = 100 °C
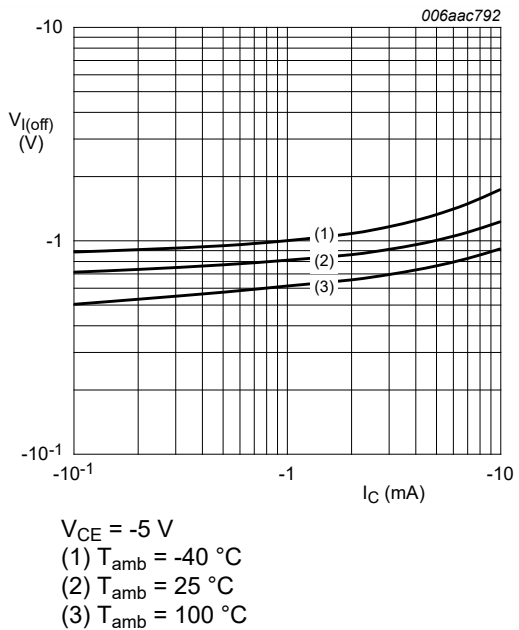
Fig. 14. TR2 (PNP): Off-state input voltage as a function of collector current; typical values

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

f = 1 MHz
T_{amb} = 25 °C
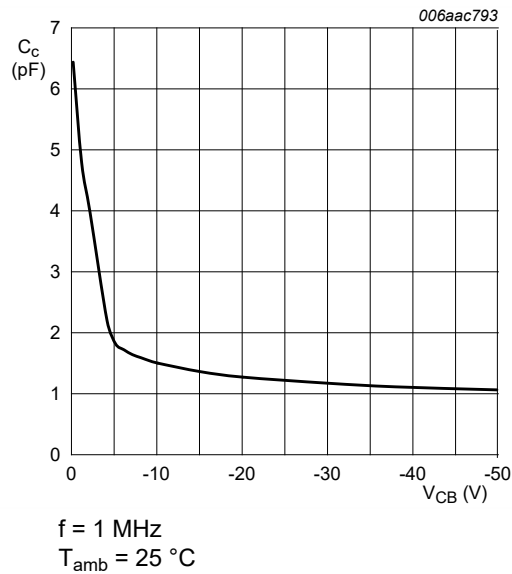
Fig. 15. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values
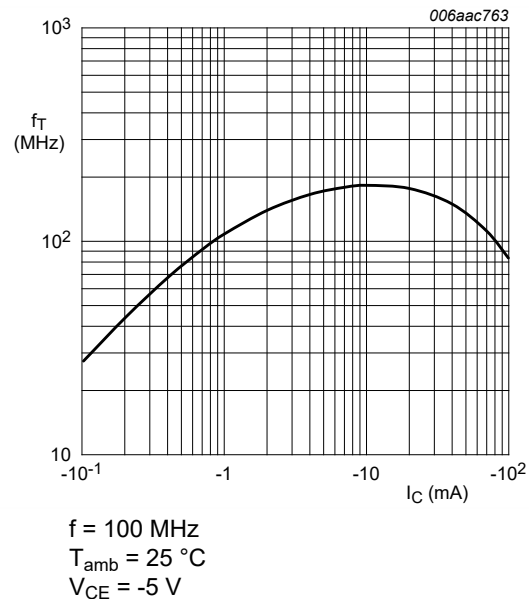

f = 100 MHz
T_{amb} = 25 °C
V_{CE} = -5 V

Fig. 16. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

11. Test information

Resistor calculation

- Calculation of bias resistor 1 (R1)

$$R1 = \frac{V(I_{I2}) - V(I_{I1})}{I_{I2} - I_{I1}}$$

- Calculation of bias resistor ratio (R2/R1)

$$\frac{R2}{R1} = \frac{V(I_{I4}) - V(I_{I3})}{R1 \cdot (I_{I4} - I_{I3})} - 1$$

aaa-020082
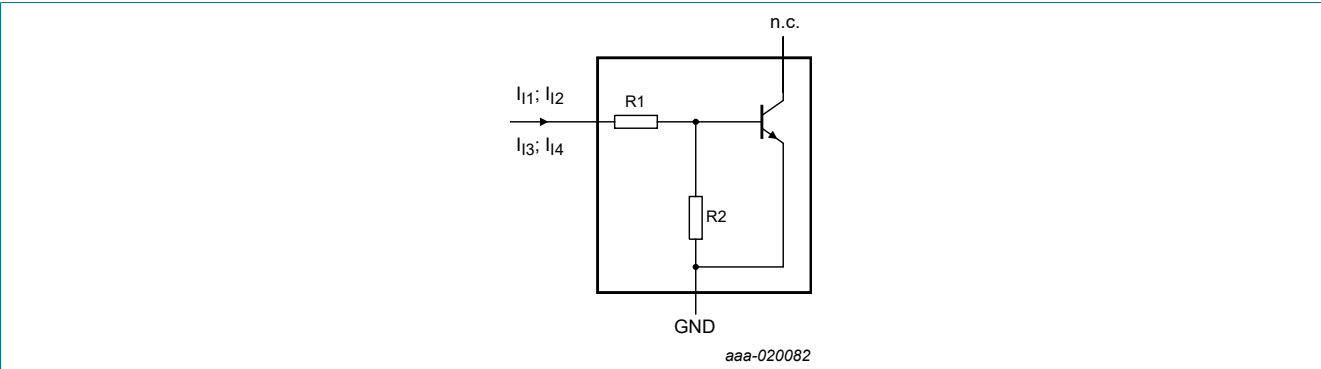
Fig. 17. TR1 (NPN): Resistor test circuit
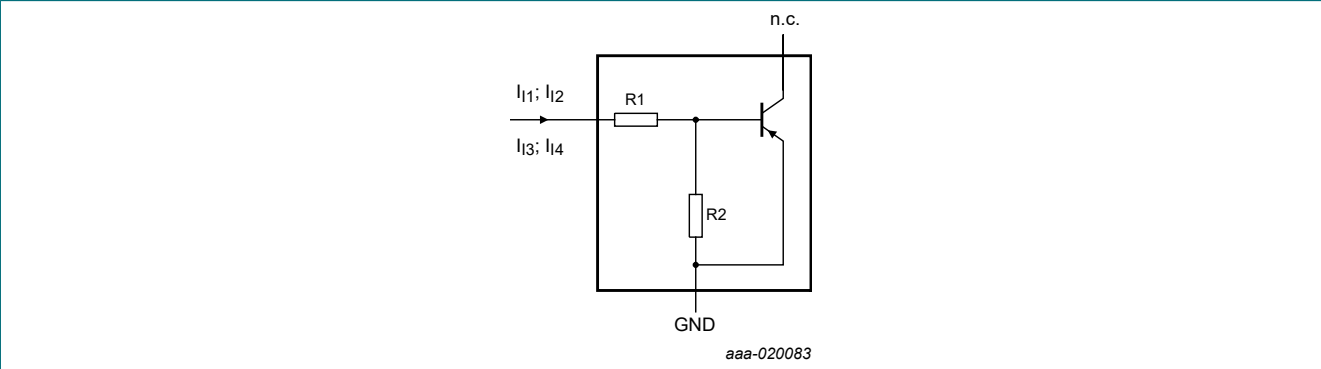

aaa-020083

Fig. 18. TR2 (PNP): Resistor test circuit

Resistor test conditions

Table 8. Resistor test conditions

Type number	R1 (kΩ)	R2 (kΩ)	Test conditions			
			I_{I1}	I_{I2}	I_{I3}	I_{I4}
Per transistor, for the PNP with negative polarity						
PUMD9	10	47	90 µA	140 µA	-55 µA	-105 µA

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50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

12. Package outline

Fig. 19. Package outline TSSOP6 (SOT363)

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

13. Soldering

solder lands

solder resist

solder paste

occupied area

Dimensions in mm

sot363_fr

Fig. 20. Reflow soldering footprint for TSSOP6 (SOT363)

solder lands

solder resist

occupied area

Dimensions in mm

preferred transport
direction during soldering
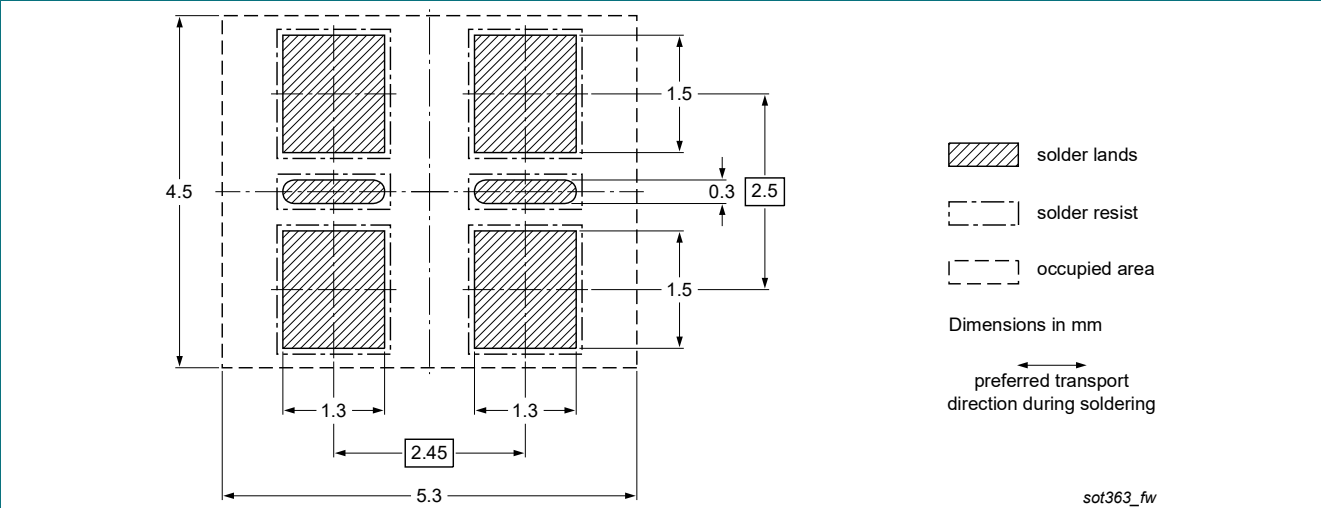
sot363_fw

Fig. 21. Wave soldering footprint for TSSOP6 (SOT363)

50 V, 100 mA NPN/PNP resistor-equipped double transistor; R1 = 10 kΩ, R2 = 47 kΩ

14. Revision history

Table 9. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PUMD9 v.7	20220701	Product data sheet	-	PEMD9_PUMD9 v.6
Modification:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Family data sheet reduced to single type data sheet. • Product changed to non-automotive qualification. Please refer to nexperia.com for automotive (-Q) product alternative(s). • Packing information removed.			
PEMD9_PUMD9 v.6	20111122	Product data sheet	-	PEMD9_PUMD9 v.5
PEMD9_PUMD9 v.5	20040415	Product data sheet	-	PEMD9_PUMD9 v.4
PEMD9_PUMD9 v.4	20031104	Product specification	-	PEMD9 v.2 PUMD9 v.3
PEMD9 v.2	20020905	Product specification	-	PEMD9 v.1
PEMD9 v.1	20011022	Preliminary specification	-	-
PUMD9 v.3	20010216	Product specification	-	PUMD9 v.2
PUMD9 v.2	19990520	Product specification	-	PUMD9 v.1
PUMD9 v.1	19990107	Product specification	-	-

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15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 1 July 2022

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