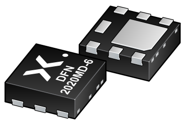


# BUK6D81-80E

**80 V, N-channel Trench MOSFET**

**4 April 2019** **Product data sheet**

## 1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Extended temperature range $T_j$ = 175 °C
- Side wettable flanks for optical solder inspection
- ElectroStatic Discharge (ESD) protection > 2 kV HBM (class H2)
- Trench MOSFET technology
- AEC-Q101 qualified

## 3. Applications

- Relay driver
- High-speed line driver
- Low-side load switch
- Switching circuits

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j$ = 25 °C | | - | - | 80 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | - | 20 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{sp}$ = 25 °C | | - | - | 9.8 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C | | - | - | 18.8 | W |
| **Static characteristics** | | | | | | | |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 3.2 A; $T_j$ = 25 °C | | - | 62 | 81 | mΩ |

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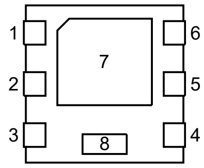
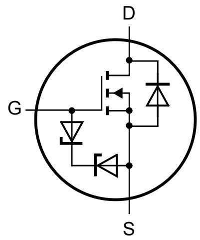
## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | D | drain | <br>Transparent top view<br>DFN2020MD-6 **(SOT1220)** | <br>017aaa255 |
| 2 | D | drain | | |
| 3 | G | gate | | |
| 4 | S | source | | |
| 5 | D | drain | | |
| 6 | D | drain | | |
| 7 | D | drain | | |
| 8 | S | source | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BUK6D81-80E | DFN2020MD-6 | plastic, leadless thermal enhanced ultra thin small outline package; 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body | SOT1220 |

## 7. Marking

**Table 4. Marking codes**

| Type number | Marking code |
|---|---|
| BUK6D81-80E | 4W |

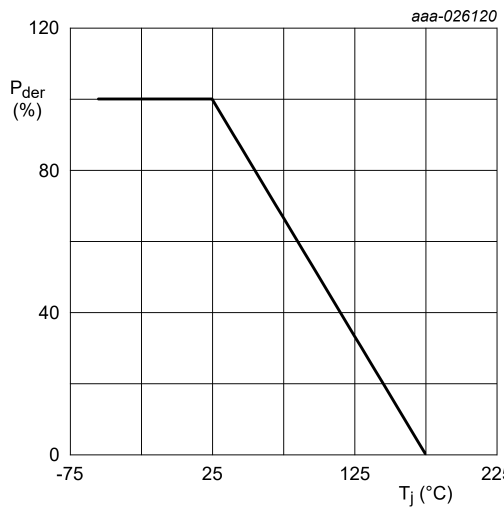
## 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

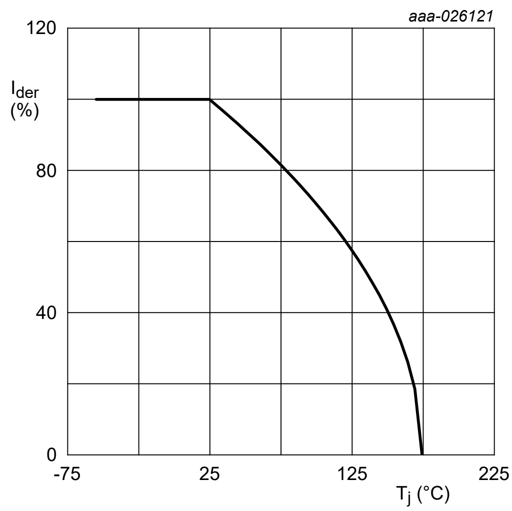
| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DS}$ | drain-source voltage | $T_j$ = 25 °C | | - | 80 | V |
| $V_{GS}$ | gate-source voltage | | | -20 | 20 | V |
| $I_D$ | drain current | $V_{GS}$ = 10 V; $T_{sp}$ = 25 °C | | - | 9.8 | A |
| | | $V_{GS}$ = 10 V; $T_{sp}$ = 100 °C | | - | 6.9 | A |
| | | $V_{GS}$ = 10 V; $T_{amb}$ = 25 °C | [1] | - | 3.2 | A |
| $I_{DM}$ | peak drain current | $T_{sp}$ = 25 °C; single pulse; $t_p \leq$ 10 µs | | - | 39 | A |
| $P_{tot}$ | total power dissipation | $T_{sp}$ = 25 °C | | - | 18.8 | W |
| | | $T_{amb}$ = 25 °C | [1] | - | 2 | W |
| $T_j$ | junction temperature | | | -55 | 175 | °C |
| $T_{amb}$ | ambient temperature | | | -55 | 175 | °C |
| $T_{stg}$ | storage temperature | | | -65 | 175 | °C |
| **Source-drain diode** | | | | | | |
| $I_S$ | source current | $T_{sp}$ = 25 °C | | - | 6.9 | A |
| | | $T_{amb}$ = 25 °C | [1] | - | 2 | A |
| $I_{SM}$ | peak source current | single pulse; $t_p \leq$ 10 µs; $T_{sp}$ = 25 °C | | - | 28 | A |
| **ESD maximum rating** | | | | | | |
| $V_{ESD}$ | electrostatic discharge voltage | HBM | [2] | - | 2000 | V |
| **Avalanche ruggedness** | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $T_{j(init)}$ = 25 °C; $I_D$ = 0.46 A; DUT in avalanche (unclamped) | | - | 19.3 | mJ |

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 $cm^2$.
[2] Measured between all pins.




$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\ \%$$

**Fig. 1. Normalized total power dissipation as a function of junction temperature**




$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\ \%$$

**Fig. 2. Normalized continuous drain current as a function of junction temperature**

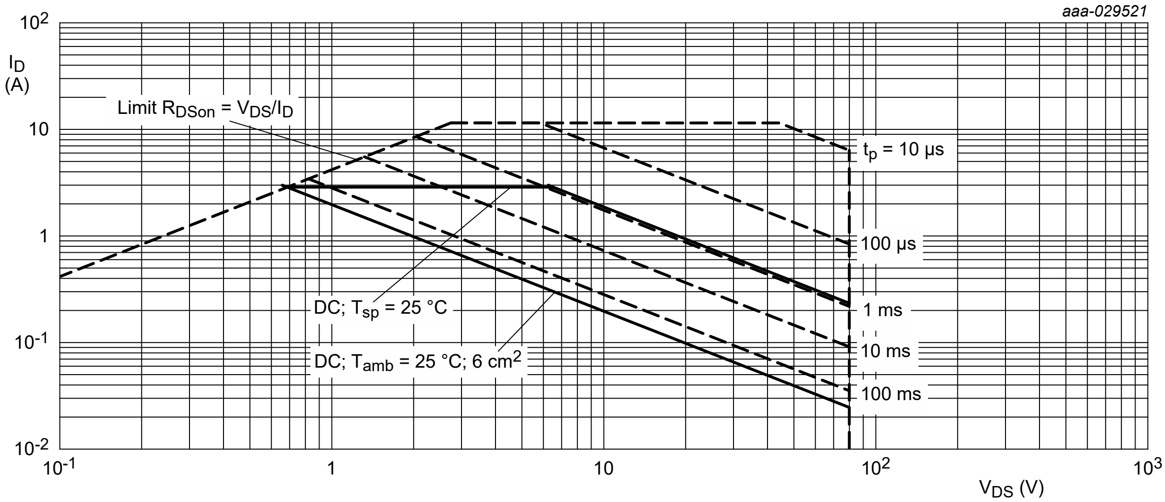



**Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage**

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | in free air | [1] | - | 66 | 76 | K/W |
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | | | - | 4 | 8 | K/W |

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 6 cm$^2$.

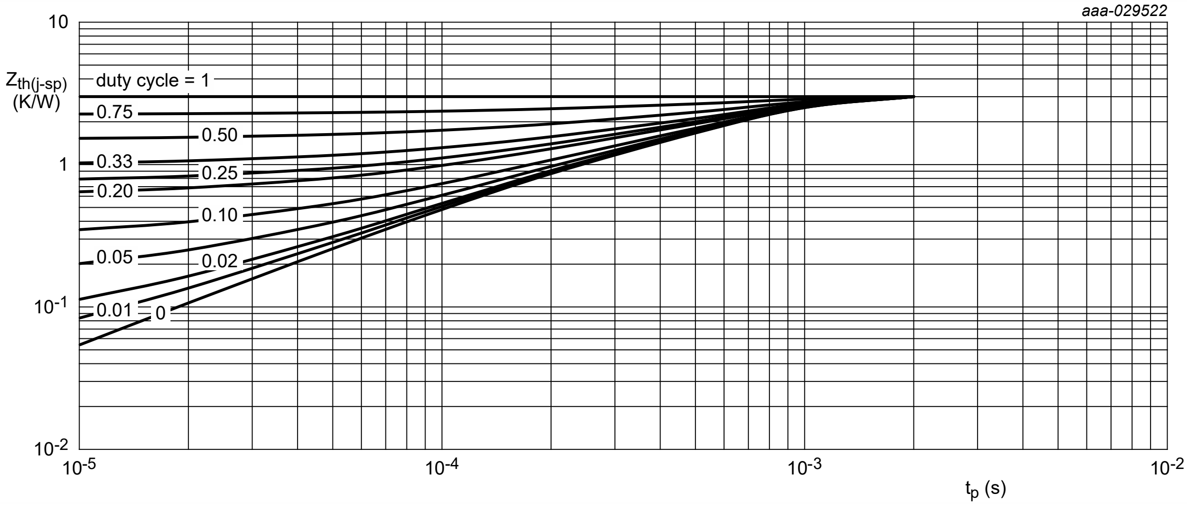
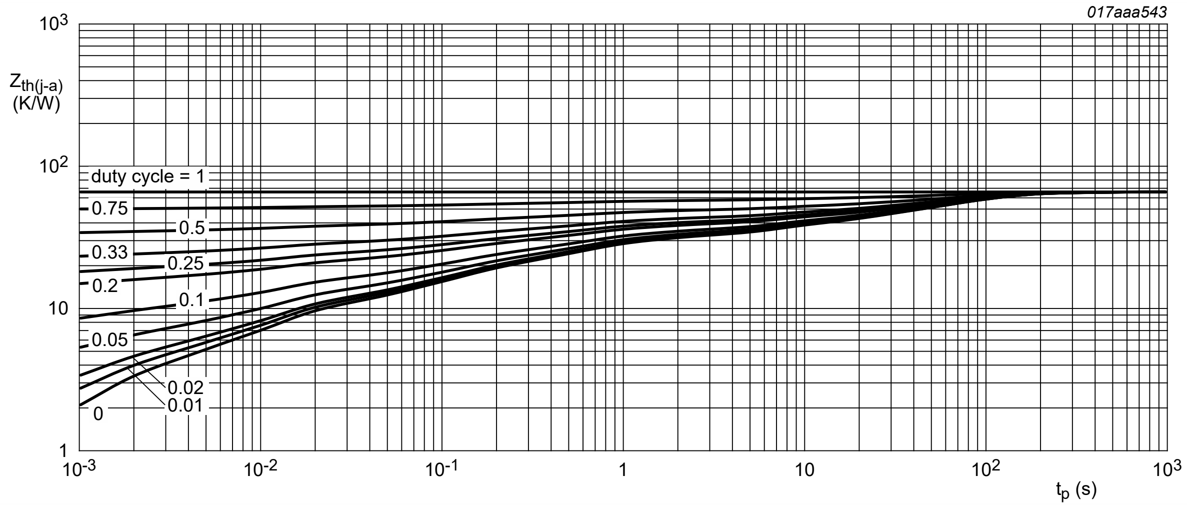



**Fig. 4. Transient thermal impedance from junction to solder point as a function of pulse duration; typical values**



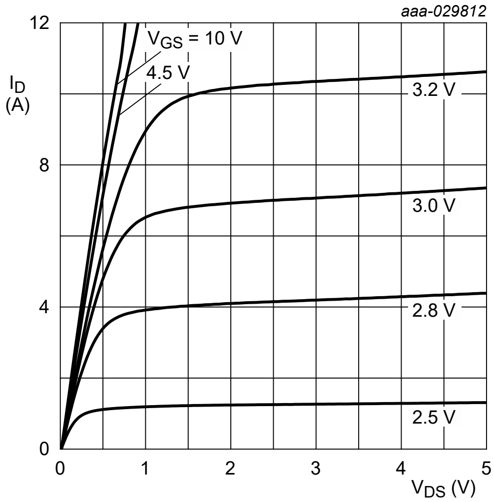

FR4 PCB, mounting pad for drain 6 cm$^2$

**Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values**

## 10. Characteristics

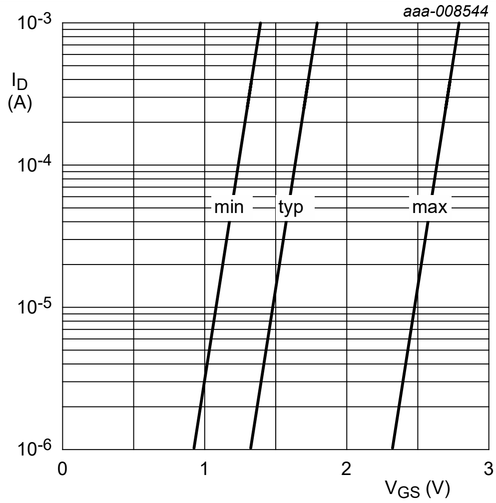
**Table 7. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D$ = 250 µA; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | 80 | - | - | V |
| $V_{GSth}$ | gate-source threshold voltage | $I_D$ = 250 µA; $V_{DS}$ = $V_{GS}$; $T_j$ = 25 °C | | 1.3 | 1.7 | 2.7 | V |
| $I_{DSS}$ | drain leakage current | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{DS}$ = 80 V; $V_{GS}$ = 0 V; $T_j$ = 125 °C | | - | - | 20 | µA |
| $I_{GSS}$ | gate leakage current | $V_{GS}$ = 20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 10 | µA |
| | | $V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | -10 | µA |
| | | $V_{GS}$ = 10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | 1 | µA |
| | | $V_{GS}$ = -10 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C | | - | - | -1 | µA |
| $R_{DSon}$ | drain-source on-state resistance | $V_{GS}$ = 10 V; $I_D$ = 3.2 A; $T_j$ = 25 °C | | - | 62 | 81 | mΩ |
| | | $V_{GS}$ = 10 V; $I_D$ = 3.2 A; $T_j$ = 175 °C | | - | 151 | 197 | mΩ |
| | | $V_{GS}$ = 4.5 V; $I_D$ = 2.9 A; $T_j$ = 25 °C | | - | 70 | 97 | mΩ |
| $g_{fs}$ | forward transconductance | $V_{DS}$ = 10 V; $I_D$ = 3.2 A; $T_j$ = 25 °C | | - | 13.3 | - | S |
| $R_G$ | gate resistance | f = 1 MHz | | - | 4.7 | - | Ω |
| **Dynamic characteristics** | | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $V_{DS}$ = 40 V; $I_D$ = 3.2 A; $V_{GS}$ = 10 V; $T_j$ = 25 °C | | - | 9.9 | 14.9 | nC |
| $Q_{GS}$ | gate-source charge | | | - | 1.2 | - | nC |
| $Q_{GD}$ | gate-drain charge | | | - | 1.8 | - | nC |
| $C_{iss}$ | input capacitance | $V_{DS}$ = 40 V; f = 1 MHz; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 504 | - | pF |
| $C_{oss}$ | output capacitance | | | - | 43 | - | pF |
| $C_{rss}$ | reverse transfer capacitance | | | - | 26 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS}$ = 40 V; $I_D$ = 3.2 A; $V_{GS}$ = 10 V; $R_{G(ext)}$ = 6 Ω; $T_j$ = 25 °C | | - | 5 | - | ns |
| $t_r$ | rise time | | | - | 4 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | | - | 15 | - | ns |
| $t_f$ | fall time | | | - | 7 | - | ns |
| **Source-drain diode** | | | | | | | |
| $V_{SD}$ | source-drain voltage | $I_S$ = 2 A; $V_{GS}$ = 0 V; $T_j$ = 25 °C | | - | 0.8 | 1.2 | V |
| $t_{rr}$ | reverse recovery time | $I_S$ = 1.9 A; $dI_S/dt$ = -100 A/µs; $V_{GS}$ = 0 V; $V_{DS}$ = 40 V; $T_j$ = 25 °C | | - | 12.4 | - | ns |
| $Q_r$ | recovered charge | | | - | 5.4 | - | nC |



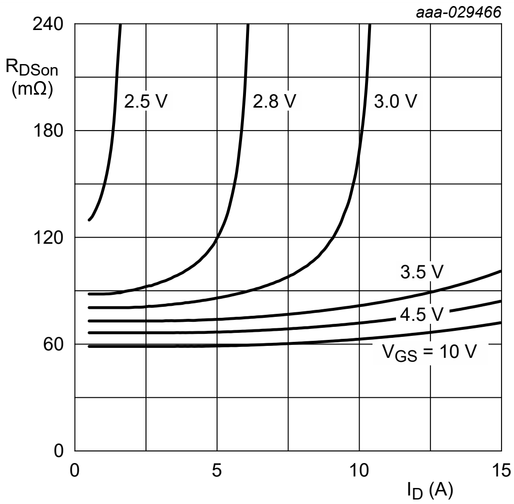

$T_j$ = 25 °C

**Fig. 6.** **Output characteristics: drain current as a function of drain-source voltage; typical values**



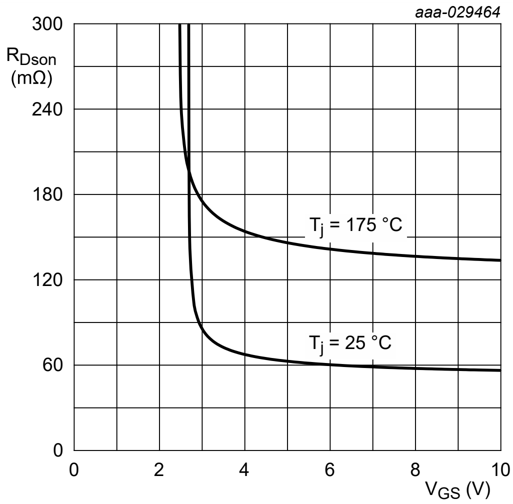

$T_j$ = 25 °C; $V_{DS}$ = 5 V

**Fig. 7.** **Sub-threshold drain current as a function of gate-source voltage**



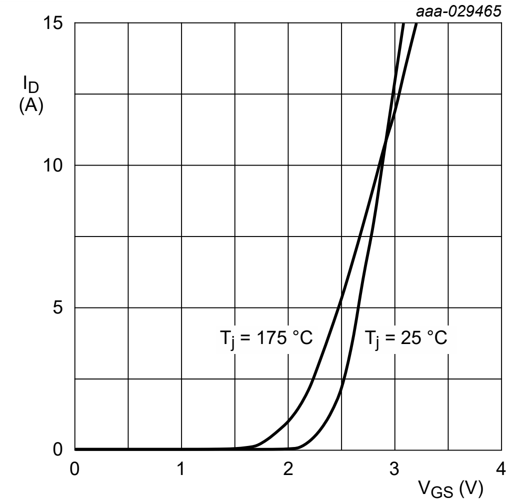

$T_j$ = 25 °C

**Fig. 8.** **Drain-source on-state resistance as a function of drain current; typical values**



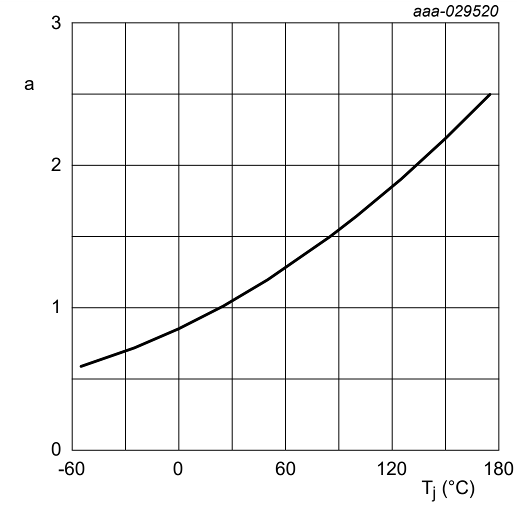

$I_D$ = 4 A

**Fig. 9.** **Drain-source on-state resistance as a function of gate-source voltage; typical values**



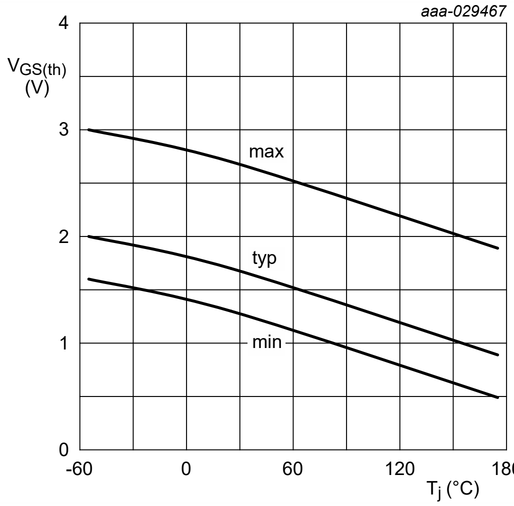

$V_{DS} > I_D \times R_{DSon}$

**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



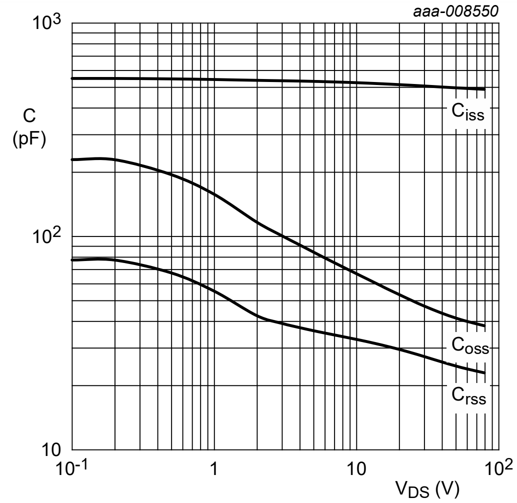

$$a = \frac{R_{DSon}}{R_{DSon(25\,°C)}}$$

**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



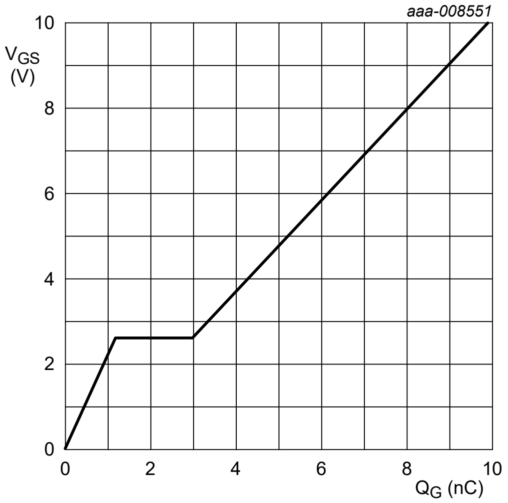

$I_D = 250\ \mu A$; $V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**




$f = 1\ MHz$; $V_{GS} = 0\ V$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**




$I_D$ = 2.8 A; $V_{DS}$ = 40 V; $T_{amb}$ = 25 °C

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

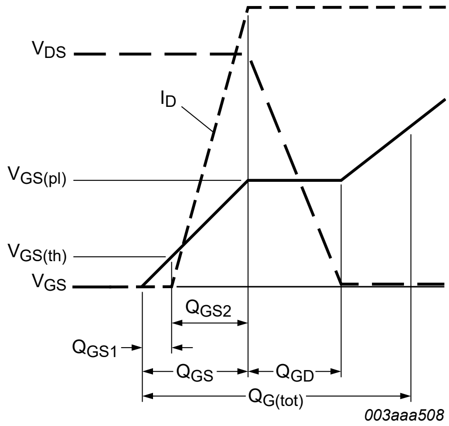
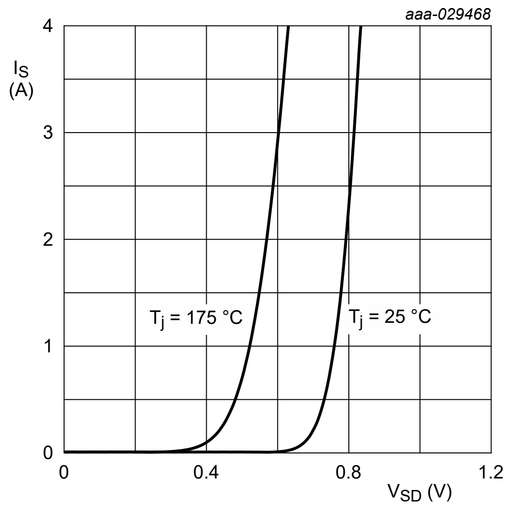



**Fig. 15. Gate charge waveform definitions**




$V_{GS}$ = 0 V

**Fig. 16. Source current as a function of source-drain voltage; typical values**

# 11. Test information

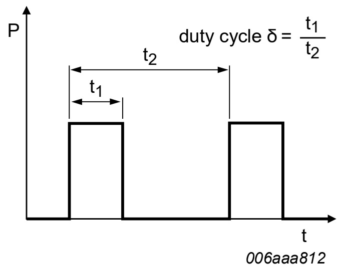


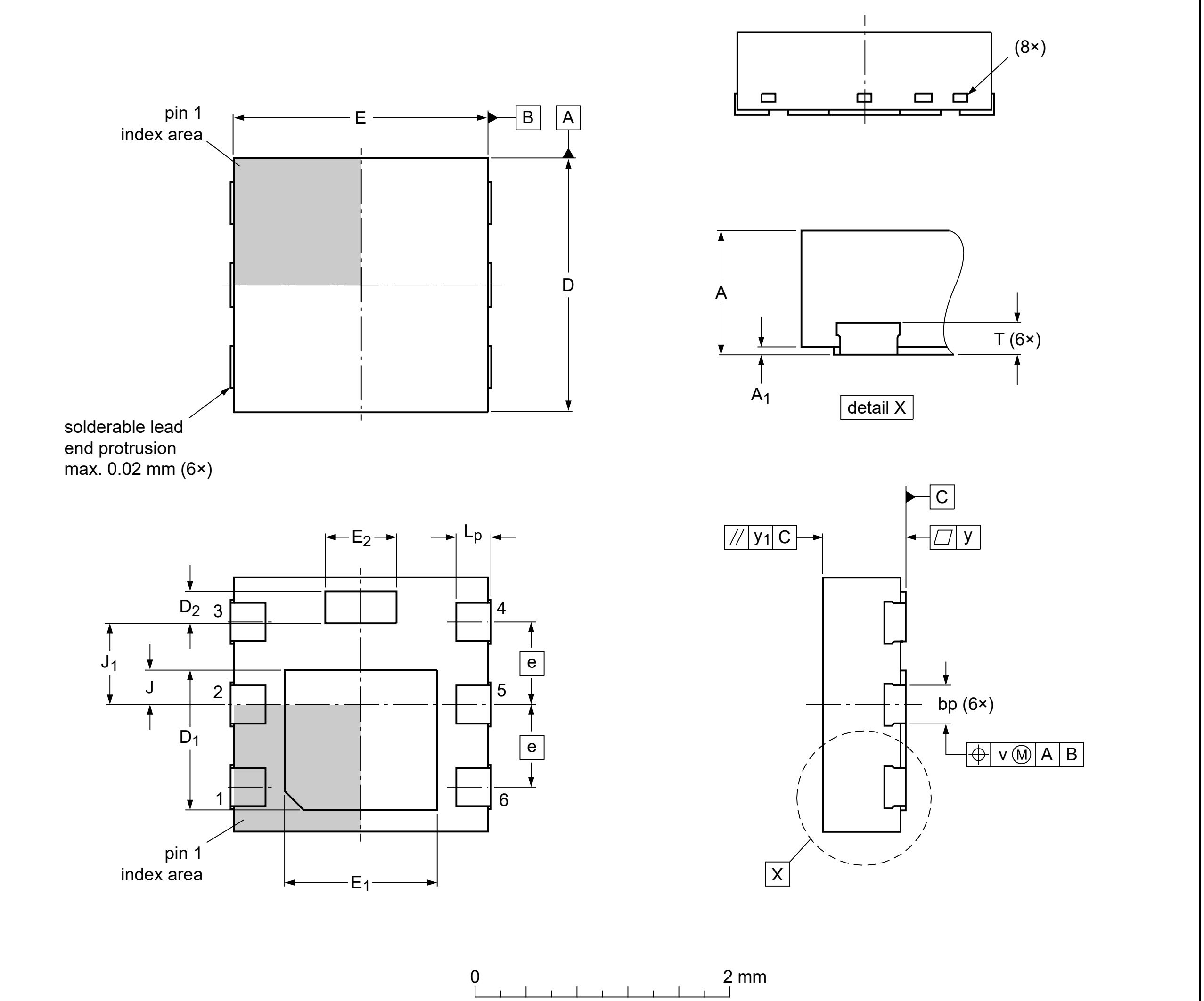

**Fig. 17. Duty cycle definition**

## Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

**DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm** **SOT1220**




Dimensions (mm are the original dimensions)

| Unit | | A | $A_1$ | bp | D | $D_1$ | $D_2$ | E | $E_1$ | $E_2$ | e | J | $J_1$ | $L_p$ | T | v | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | min | | | 0.25 | 1.9 | 1.0 | 0.2 | 1.9 | 1.1 | 0.51 | | | | 0.2 | 0.10 | | | |
| mm | nom | | | | | | | | | | 0.65 | 0.27 | 0.64 | | 0.16 | 0.1 | 0.05 | 0.1 |
| | max | 0.65 | 0.04 | 0.35 | 2.1 | 1.2 | 0.3 | 2.1 | 1.3 | 0.61 | | | | 0.3 | 0.22 | | | |

Note
1. Dimension A is including plating thickness.

*sot1220_po*

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT1220 | | | | | | ~~18-05-30~~ 18-06-07 |

**Fig. 18. Package outline** DFN2020MD-6 **(SOT1220)**

# 13. Soldering

**Footprint information for reflow soldering of DFN2020MD-6 package** **SOT1220**

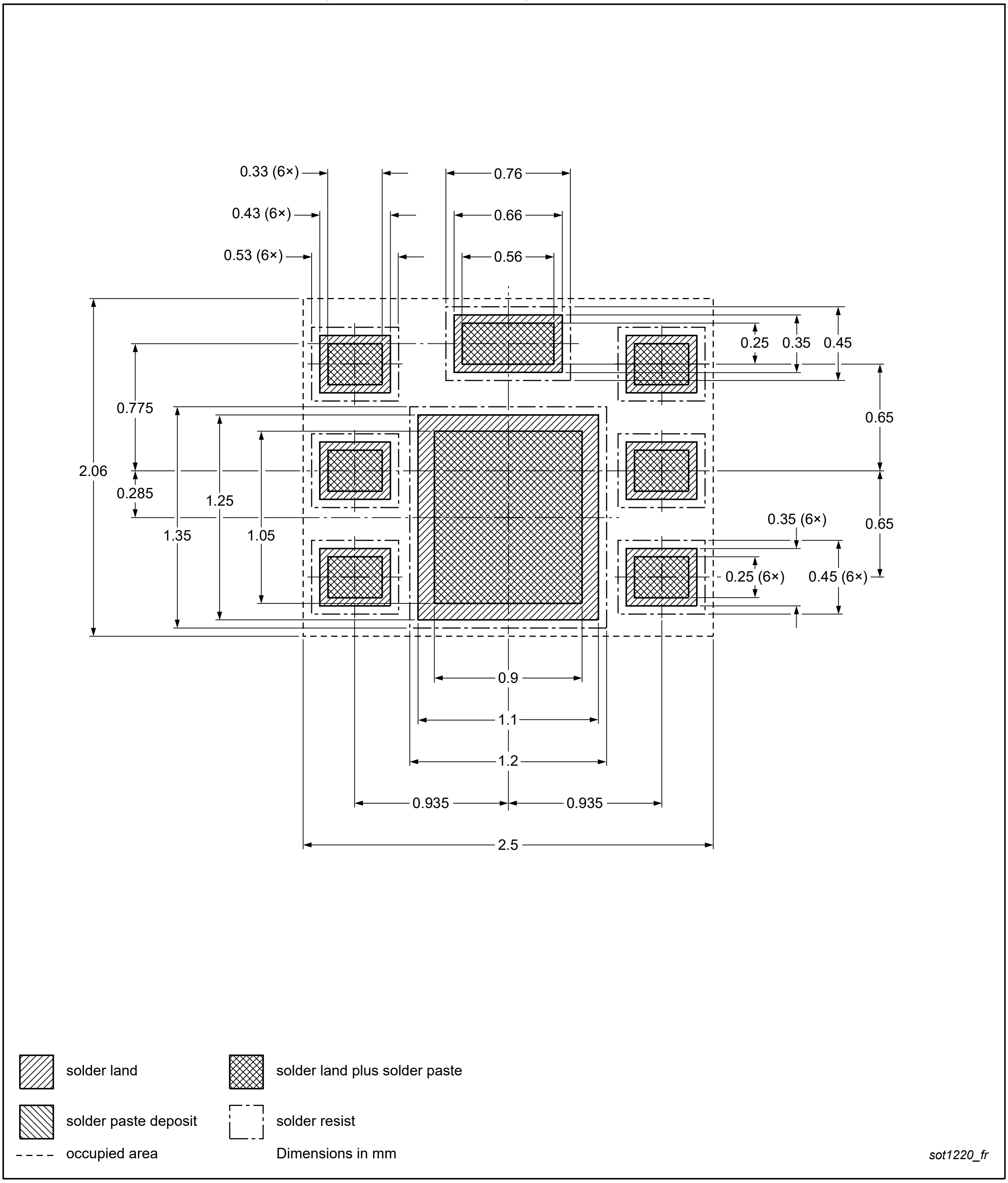



**Fig. 19. Reflow soldering footprint for** DFN2020MD-6 **(SOT1220)**

## 14. Revision history

**Table 8. Revision history**

| Data sheet ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| BUK6D81-80E v.1 | 20190404 | Product data sheet | - | - |

# 15. Legal information

### Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at https://www.nexperia.com.

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## Contents




Date of release: 4 April 2019