

N-channel TrenchMOS standard level FET 18 July 2013

Product data sheet

1. General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

3. Applications

- 12 V, 24 V and 42 V loads
- Automotive systems
- General purpose power switching
- Motors, lamps and solenoids

4. Quick reference data

Table 1. Q	uick reference data					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	-	75	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1; Fig. 3</u>	-	-	69	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	-	158	W
Static chara	cteristics					
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; <u>Fig. 11; Fig. 12</u>	-	12.6	14	mΩ
Dynamic cha	aracteristics					
Q _{GD}	gate-drain charge	V_{GS} = 10 V; I _D = 25 A; V _{DS} = 60 V; T _j = 25 °C; <u>Fig. 13</u>	-	15	-	nC
Avalanche r	uggedness	·				,
E _{DS(AL)S}	non-repetitive drain- source avalanche energy	I_D = 69 A; $V_{sup} \le$ 75 V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped	-	-	136	mJ

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5. Pinning information

Table 2.	Pinning	information		
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	mb	D
2	D	drain[1]		
3	S	source		G-UF44
mb	D	mounting base; connected to drain	DPAK (SOT428)	mbb076 S

[1] It is not possible to make a connection to pin 2

6. Ordering information

Table 3. Ordering in	formation					
Type number	Package					
	Name	Description	Version			
BUK7214-75B	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428			

7. Marking

Table 4. Marking codes	
Type number	Marking code
BUK7214-75B	BUK7214-75B

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Мах	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	75	V
V _{DGR}	drain-gate voltage	R _{GS} = 20 kΩ	-	75	V
V _{GS}	gate-source voltage		-20	20	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u> ; <u>Fig. 3</u>	-	69	А
		T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 1</u>	-	49	А
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \ \mu$ s; Fig. 3	-	276	А
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	158	W

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Symbol	Parameter	Conditions	Min	Max	Unit
T _{stg}	storage temperature		-55	175	°C
Tj	junction temperature		-55	175	°C
Source-drain	n diode				
I _S	source current	T _{mb} = 25 °C	-	69	А
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^\circ C$	-	276	А
Avalanche ru	uggedness				
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	$ I_D = 69 \text{ A}; V_{sup} \le 75 \text{ V}; \text{ R}_{GS} = 50 \Omega; V_{GS} = 10 \text{ V}; \text{ T}_{j(init)} = 25 \text{ °C}; \text{ unclamped} $	-	136	mJ

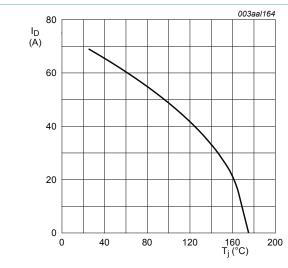


Fig. 1. Continuous drain current as a function of mounting base temperature

 $V_{GS} \ge 10V$

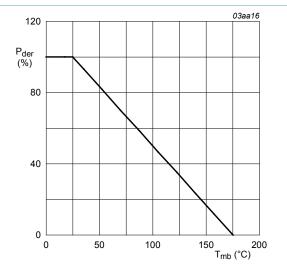
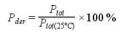
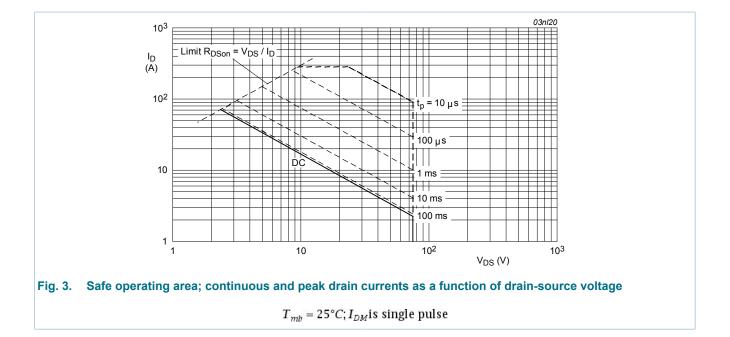


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

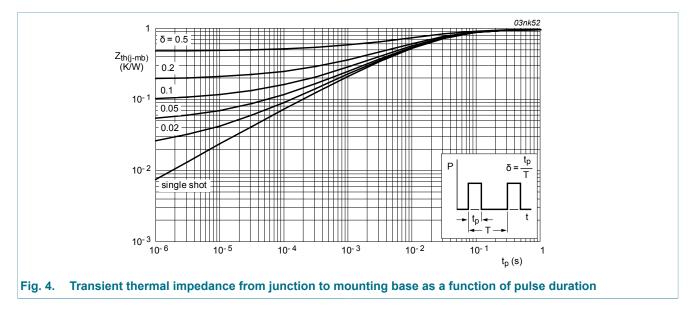


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9. Thermal characteristics

Table 6. The	rmal characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	<u>Fig. 4</u>	-	-	0.95	K/W
R _{th(j-a)}	thermal resistance from junction to ambient		-	71.4	-	K/W



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10. Characteristics

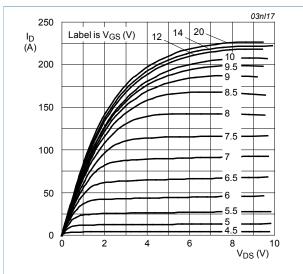
Symbol	Parameter	Conditions	Min	Тур	Мах	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	75	-	-	V
	breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	70	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 175 °C; <u>Fig. 10</u>	0.9	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS} ; T_j = 25 °C; Fig. 10	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 10	-	-	4.4	V
I _{DSS}	drain leakage current	V_{DS} = 75 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	μA
		V_{DS} = 75 V; V_{GS} = 0 V; T_j = 25 °C	-	0.02	1	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 °C	-	2	100	nA
R _{DSon} drain-source on-state resistance		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 11; Fig. 12	-	-	33	mΩ
	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11; Fig. 12	-	12.6	14	mΩ	
Dynamic ch	naracteristics		I			
Q _{G(tot)}	total gate charge I_D = 25 A; V_{DS} = 60 V; V_{GS} = 10 V;	-	41	-	nC	
Q _{GS}	gate-source charge	T _j = 25 °C; <u>Fig. 13</u>	-	9	-	nC
Q _{GD}	gate-drain charge		-	15	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz;	-	1959	2612	pF
C _{oss}	output capacitance	T _j = 25 °C; <u>Fig. 14</u>	-	326	391	pF
C _{rss}	reverse transfer capacitance		-	159	218	pF
t _{d(on)}	turn-on delay time	V_{DS} = 25 V; R _L = 1.2 Ω ; V _{GS} = 10 V;	-	18	-	ns
r	rise time	R _{G(ext)} = 10 Ω; T _j = 25 °C	-	114	-	ns
d(off)	turn-off delay time	1	-	52	-	ns
f	fall time		-	45	-	ns
LD	internal drain inductance	measured from drain to centre of die ; T _j = 25 °C	-	2.5	-	nH
L _S	internal source inductance	measured from source lead to source bond pad ; T _i = 25 °C	-	7.5	-	nH

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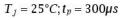
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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
Source-drain diode							
V _{SD}	source-drain voltage	I_{S} = 25 A; V_{GS} = 0 V; T_{j} = 25 °C; <u>Fig. 15</u>		-	0.85	1.2	V
t _{rr}	reverse recovery time	I _S = 20 A; dI _S /dt = -100 A/μs;		-	74	-	ns
Q _r	recovered charge	V _{GS} = -10 V; V _{DS} = 30 V; T _j = 25 °C		-	94	-	nC







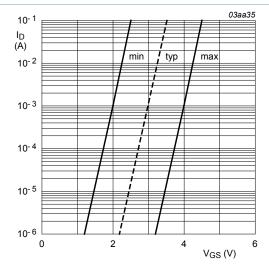


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

 $T_j = 25 \,^{\circ}C; V_{DS} = 5V$

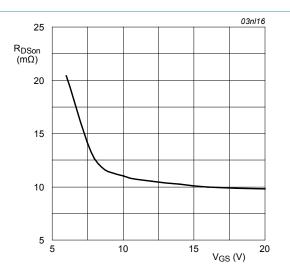
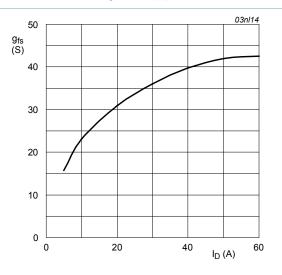


Fig. 6. Drain-source on-state resistance as a function of gate-source voltage; typical values

 $T_j = 25^{\circ}C; I_D = 25A$





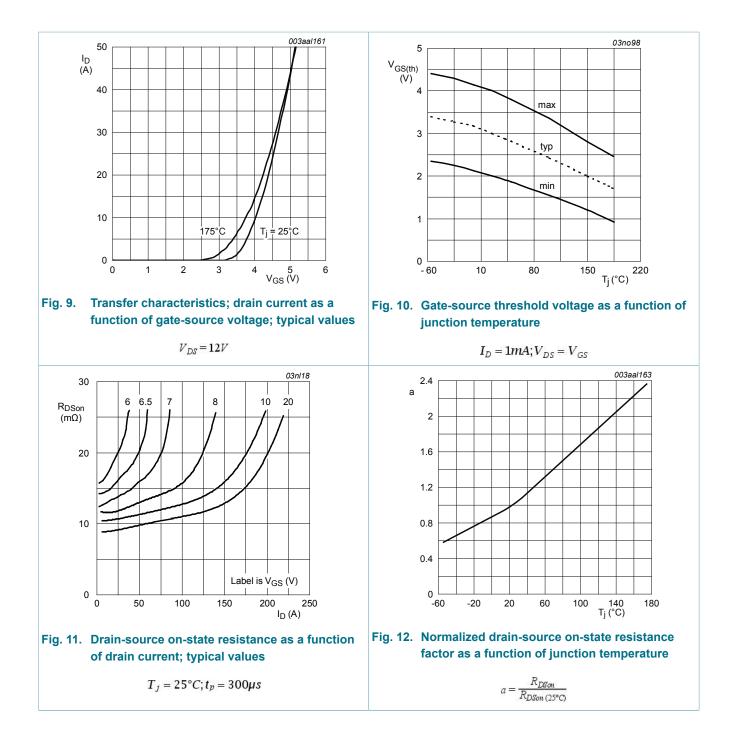
 $T_j = 25^{\circ}C; V_{DS} = 25V$



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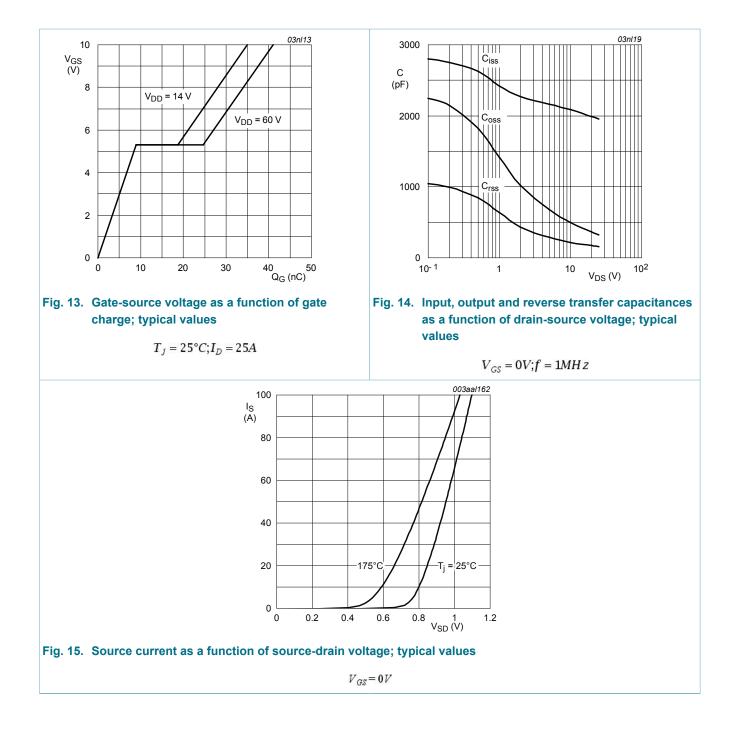
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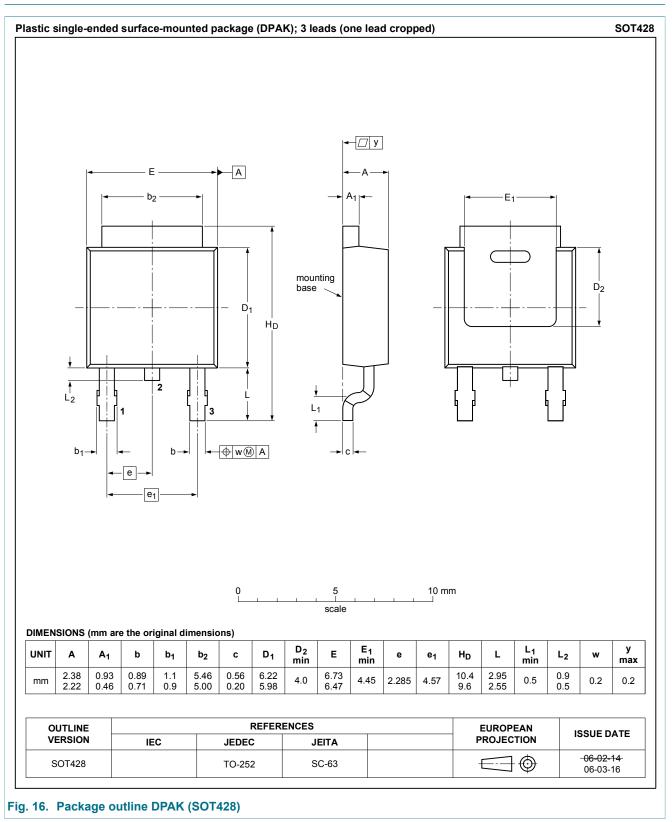
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11. Package outline



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Product data sheet

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12. Legal information

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Document status [1][2]	Product status [<u>3]</u>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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