



# BUK78150-55A

N-channel TrenchMOS standard level FET

Rev. 02 — 16 June 2010

Product data sheet

## 1. Product profile

### 1.1 General description

Standard level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for standard level gate drive sources
- Q101 compliant

### 1.3 Applications

- 12 V and 24 V loads
- Motors, lamps and solenoids
- Automotive and general purpose power switching

### 1.4 Quick reference data

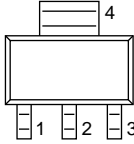
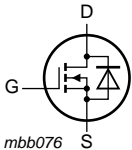
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 150\text{ °C}$	-	-	55	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	5.5	A
$P_{tot}$	total power dissipation	$T_{sp} = 25\text{ °C}$ ; see <a href="#">Figure 2</a>	-	-	8	W
<b>Static characteristics</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 150\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	278	m $\Omega$
		$V_{GS} = 10\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	128	150	m $\Omega$
<b>Avalanche ruggedness</b>						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 5\text{ A}$ ; $V_{sup} \leq 55\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 10\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped	-	-	25	mJ

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## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>SOT223 (SC-73)</p>	 <p>mbb076</p>
2	D	drain		
3	S	source		
4	D	drain		

## 3. Ordering information

Table 3. Ordering information

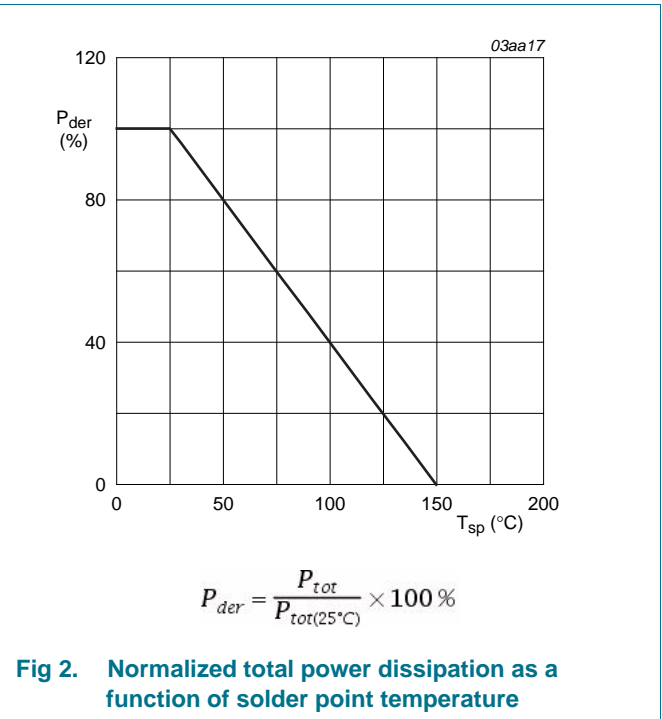
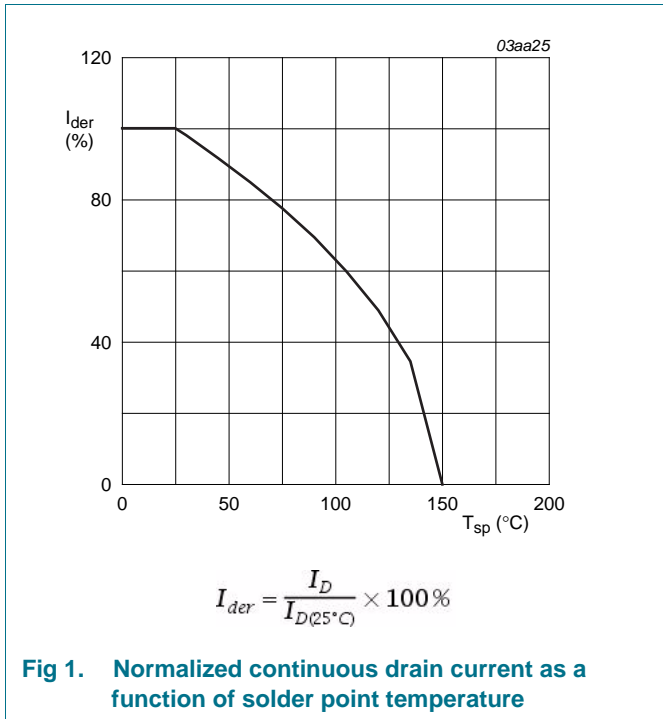
Type number	Package		
	Name	Description	Version
BUK78150-55A	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

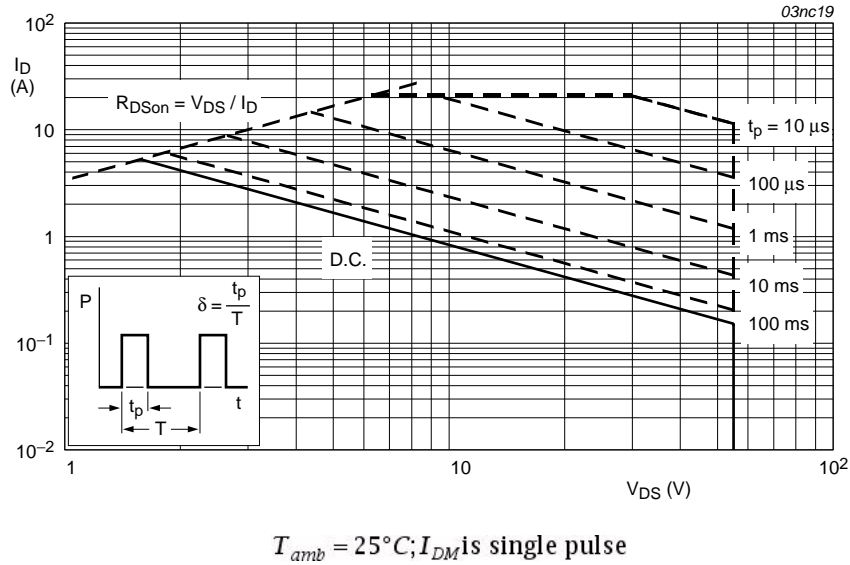
**4. Limiting values**

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	-	55	V
V <sub>DGR</sub>	drain-gate voltage	R <sub>GS</sub> = 20 kΩ	-	-	55	V
V <sub>GS</sub>	gate-source voltage		-20	-	20	V
I <sub>D</sub>	drain current	T <sub>sp</sub> = 25 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a> ; see <a href="#">Figure 3</a>	-	-	5.5	A
		T <sub>sp</sub> = 100 °C; V <sub>GS</sub> = 10 V; see <a href="#">Figure 1</a>	-	-	3.8	A
I <sub>DM</sub>	peak drain current	T <sub>sp</sub> = 25 °C; t <sub>p</sub> ≤ 10 μs; pulsed; see <a href="#">Figure 3</a>	-	-	22	A
P <sub>tot</sub>	total power dissipation	T <sub>sp</sub> = 25 °C; see <a href="#">Figure 2</a>	-	-	8	W
T <sub>stg</sub>	storage temperature		-55	-	150	°C
T <sub>j</sub>	junction temperature		-55	-	150	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>sp</sub> = 25 °C	-	-	5.5	A
I <sub>SM</sub>	peak source current	t <sub>p</sub> ≤ 10 μs; pulsed; T <sub>sp</sub> = 25 °C	-	-	22	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 5 A; V <sub>sup</sub> ≤ 55 V; R <sub>GS</sub> = 50 Ω; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; unclamped	-	-	25	mJ



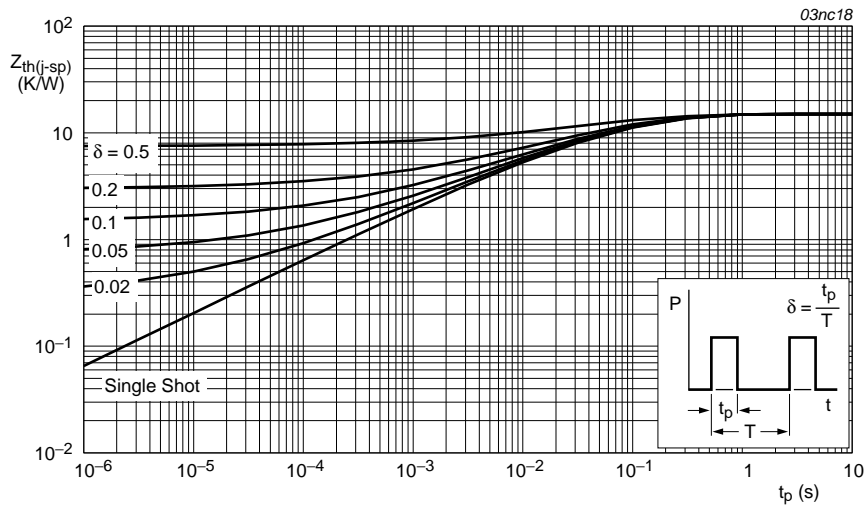


**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	see <a href="#">Figure 4</a>	-	70	-	K/W

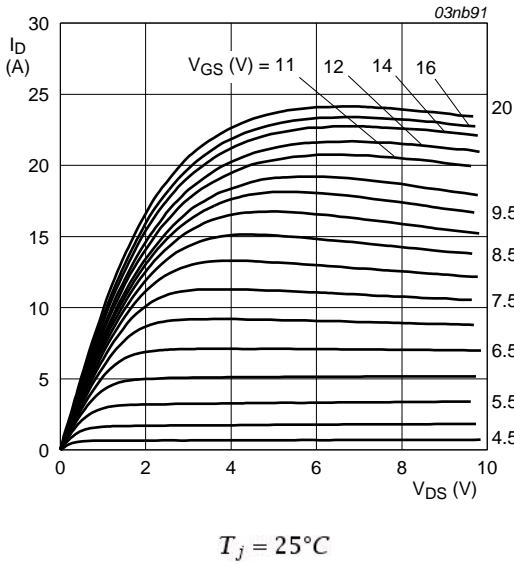


**Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration**

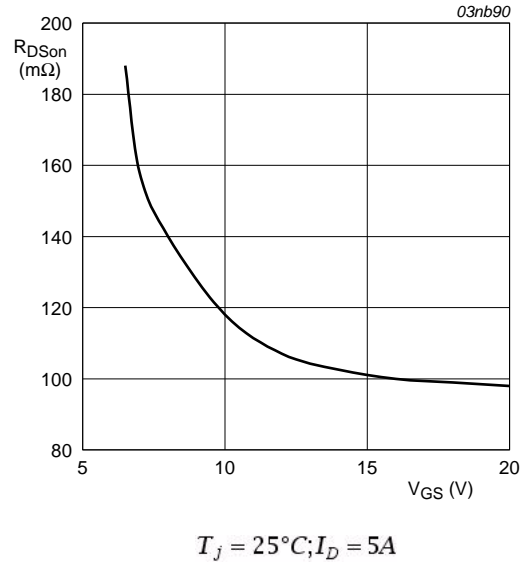
## 6. Characteristics

Table 6. Characteristics

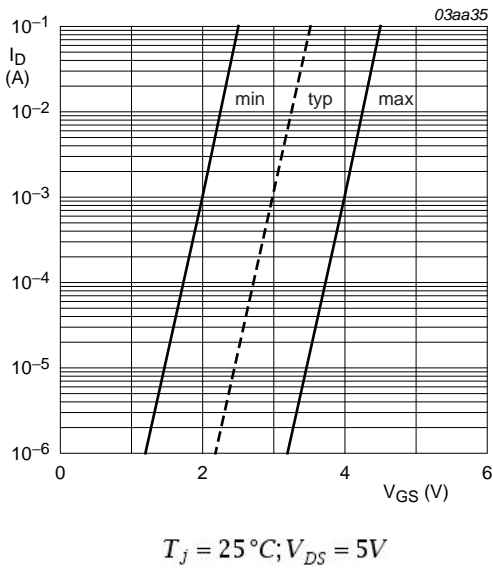
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	55	-	-	V
		$I_D = 0.25 \text{ mA}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	50	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	2	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ see <a href="#">Figure 11</a>	-	-	4.4	V
$I_{DSS}$	drain leakage current	$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 150 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
		$V_{DS} = 55 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.05	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{DS} = 0 \text{ V}; V_{GS} = 20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{DS} = 0 \text{ V}; V_{GS} = -20 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 150 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	-	278	$\text{m}\Omega$
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 12</a> ; see <a href="#">Figure 13</a>	-	128	150	$\text{m}\Omega$
<b>Dynamic characteristics</b>						
$C_{iss}$	input capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; f = 1 \text{ MHz};$ $T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 14</a>	-	170	230	pF
$C_{oss}$	output capacitance		-	54	65	pF
$C_{rss}$	reverse transfer capacitance		-	37	52	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 \text{ V}; R_L = 2.7 \text{ } \Omega; V_{GS} = 10 \text{ V};$ $R_{G(ext)} = 5.6 \text{ } \Omega; T_j = 25 \text{ }^\circ\text{C}$	-	3	-	ns
$t_r$	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	8	-	ns
$t_f$	fall time		-	10	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ see <a href="#">Figure 15</a>	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 10 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s};$ $V_{GS} = -10 \text{ V}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	32	-	ns
$Q_r$	recovered charge		-	50	-	nC



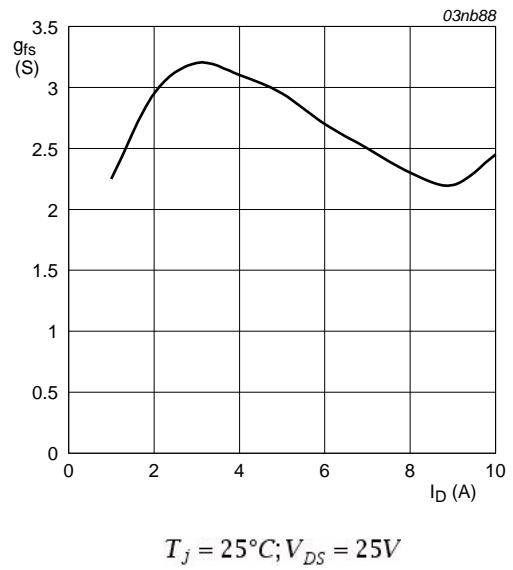
**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values**



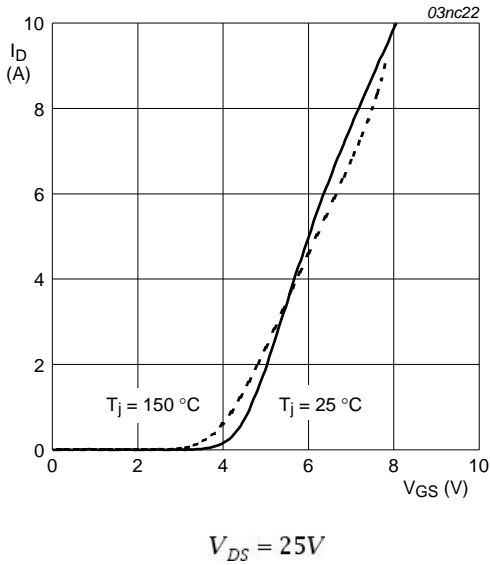
**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values**



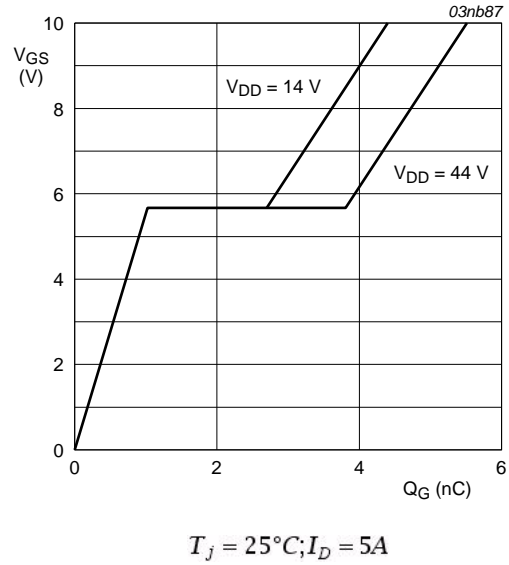
**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



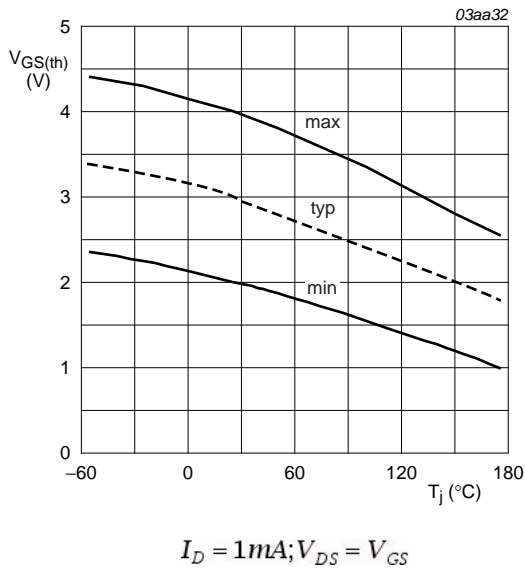
**Fig 8. Forward transconductance as a function of drain current; typical values**



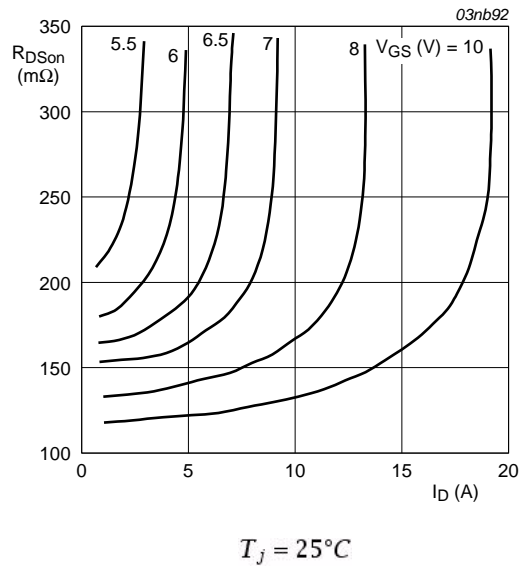
**Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



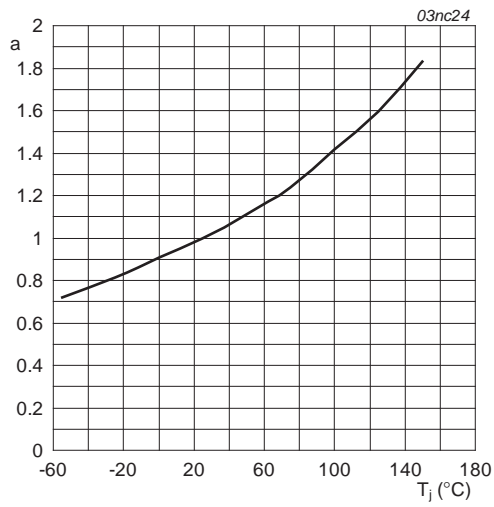
**Fig 10. Gate-source voltage as a function of turn-on gate charge; typical values**



**Fig 11. Gate-source threshold voltage as a function of junction temperature**

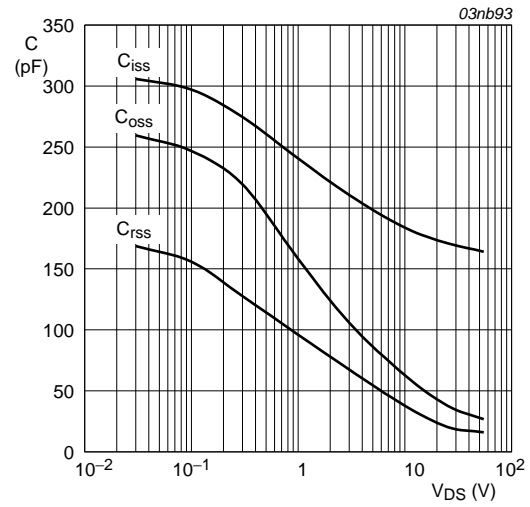


**Fig 12. Drain-source on-state resistance as a function of drain current; typical values**



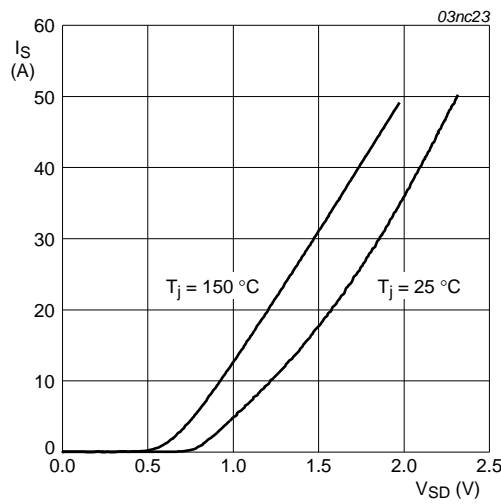
$$a = \frac{R_{DSon}}{R_{DSon(25^{\circ}\text{C})}}$$

**Fig 13. Normalized drain source on-state resistance factor as a function of junction temperature**



$$V_{GS} = 0V; f = 1MHz$$

**Fig 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$$V_{GS} = 0V$$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values**



**7. Package outline**

Plastic surface-mounted package with increased heatsink; 4 leads

SOT223

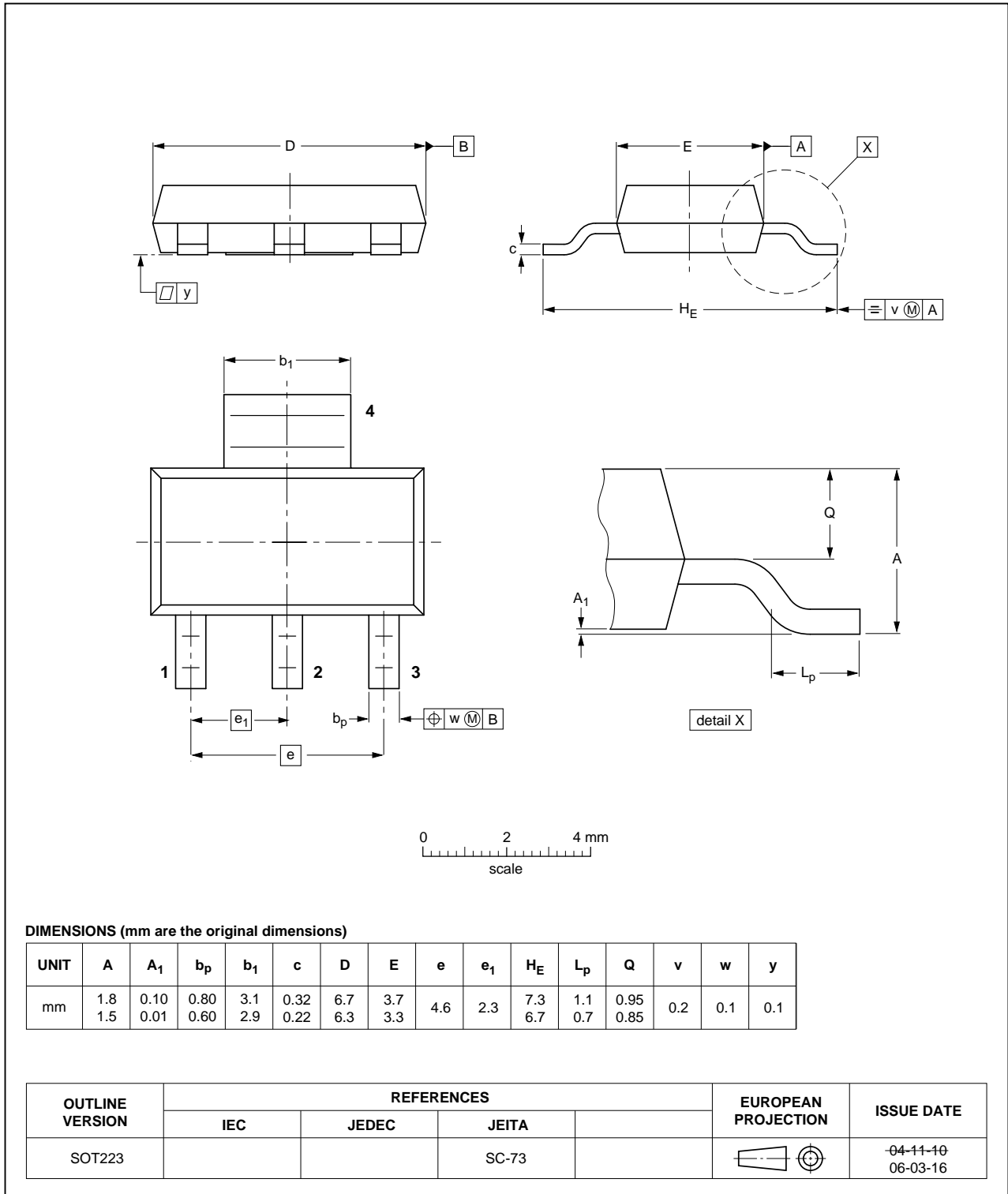


Fig 16. Package outline SOT223 (SC-73)

## 8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK78150-55A v.2	20100616	Product data sheet	-	BUK78150-55A v.1
Modifications:	<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors</li><li>• Legal texts have been adapted to the new company name where appropriate.</li></ul>			
BUK78150-55A v.1 (9397 750 07738)	20010130	Product Specification	-	-

## 9. Legal information

### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

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