



# BUK7K8R7-40E

Dual N-channel 40 V, 8.5 mΩ standard level MOSFET

6 November 2013

Product data sheet

## 1. General description

Dual standard level N-channel MOSFET in an LFPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with  $V_{GS(th)}$  of greater than 1 V at 175 °C

## 3. Applications

- 12 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

Table 1. Quick reference data

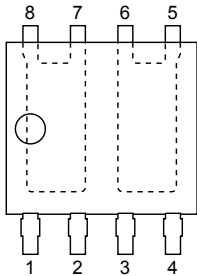
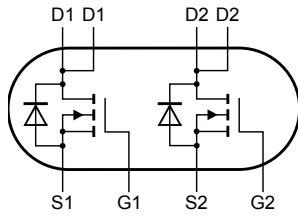
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$	-	-	40	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ <a href="#">Fig. 1</a>	[1]	-	30	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ <a href="#">Fig. 2</a>	-	-	53	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 15\text{ A}; T_j = 25\text{ °C};$ <a href="#">Fig. 11</a>	-	7	8.5	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 15\text{ A}; V_{DS} = 32\text{ V}; V_{GS} = 10\text{ V};$ $T_j = 25\text{ °C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	7.8	-	nC

[1] Continuous current is limited by package.

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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK7K8R7-40E	LFPAK56D	Plastic single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7K8R7-40E	78E740

## 8. Limiting values

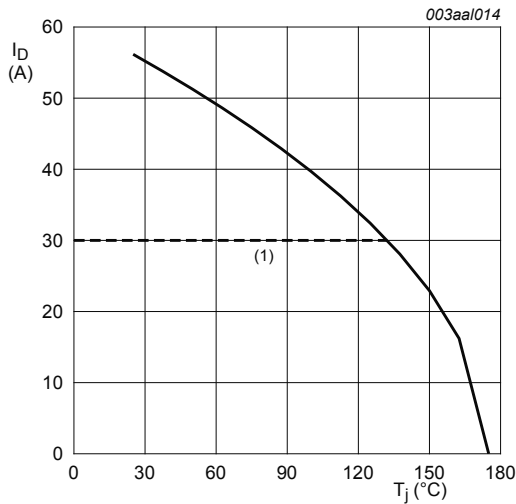
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$		-	40	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$		-	40	V
$V_{GS}$	gate-source voltage	$T_j \leq 175\text{ °C}$ ; DC		-20	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 1	[1]	-	30	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; Fig. 1	[1]	-	30	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; Fig. 4		-	225	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 2		-	53	W

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>stg</sub>	storage temperature			-55	175	°C
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode FET1 and FET2</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	30	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	225	A
<b>Avalanche Ruggedness FET1 and FET2</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	I <sub>D</sub> = 30 A; V <sub>sup</sub> ≤ 40 V; V <sub>GS</sub> = 10 V; T <sub>j(init)</sub> = 25 °C; Fig. 3	[2][3]	-	84	mJ

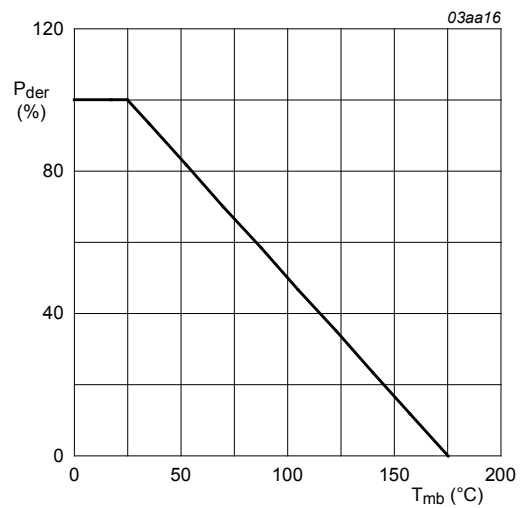
- [1] Continuous current is limited by package.
- [2] Refer to application note AN10273 for further information
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C



(1) Capped at 30A due to package

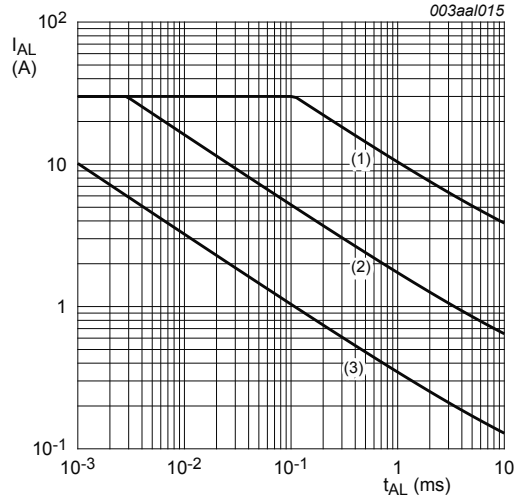
**Fig. 1. Continuous drain current as a function of mounting base temperature**

$$V_{GS} \geq 10V$$



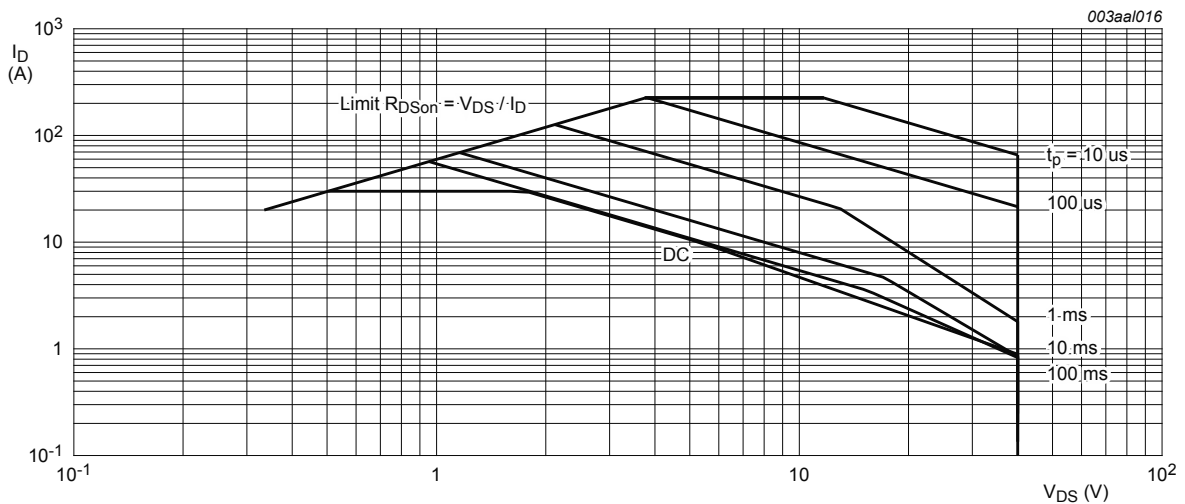
**Fig. 2. Normalized total power dissipation as a function of mounting base temperature**

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$



**Fig. 3. Avalanche rating; avalanche current as a function of avalanche time**

(1)  $T_{j (init)} = 25^{\circ}C$ ; (2)  $T_{j (init)} = 150^{\circ}C$ ; (3) Repetitive Avalanche



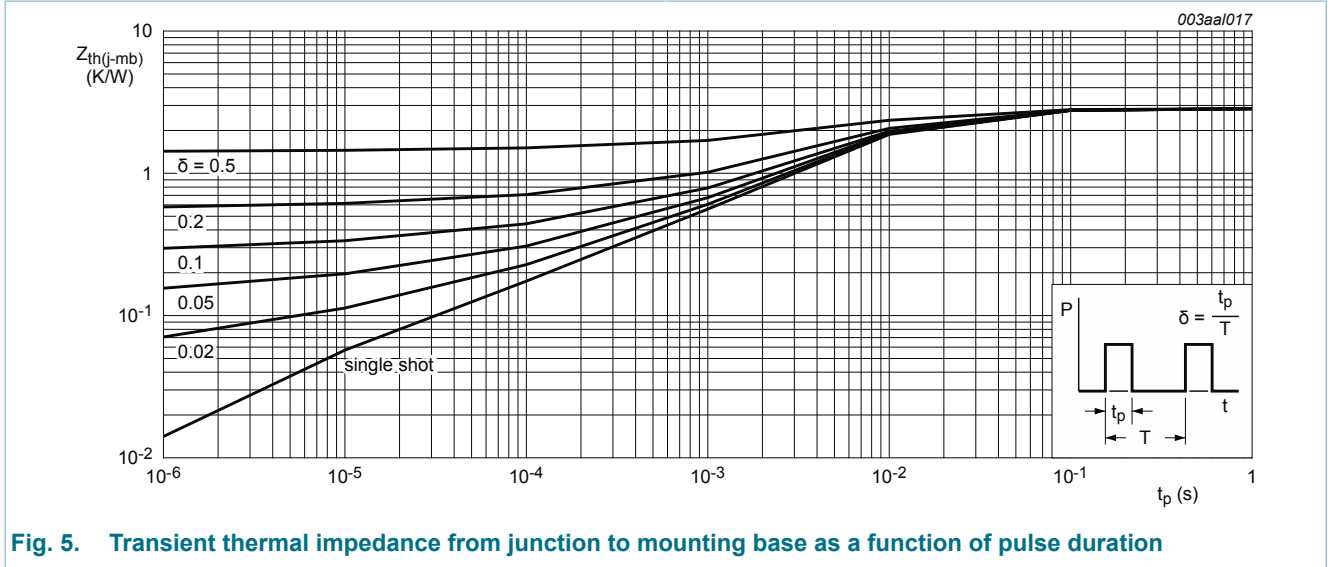
**Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage**

$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

## 9. Thermal characteristics

**Table 6. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	<a href="#">Fig. 5</a>	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W



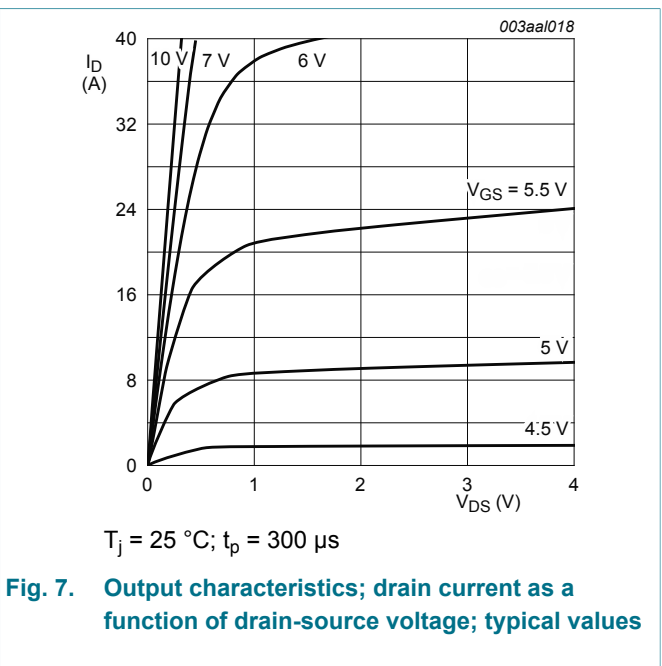
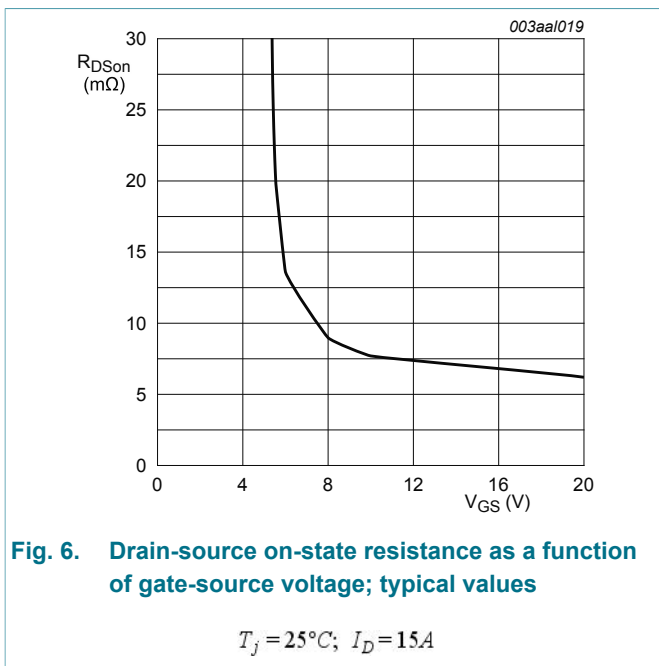
**Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration**

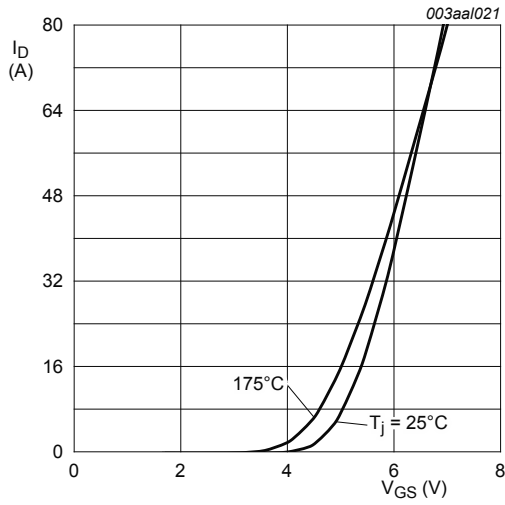
## 10. Characteristics

**Table 7. Characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C;$ <a href="#">Fig. 9; Fig. 10</a>	-	-	4.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.02	1	$\mu A$
		$V_{DS} = 40 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 15 A; T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 11</a>	-	7	8.5	mΩ
		$V_{GS} = 10 V; I_D = 15 A; T_j = 175 \text{ }^\circ C;$ <a href="#">Fig. 11; Fig. 12</a>	-	13.8	16.7	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 15 A; V_{DS} = 32 V; V_{GS} = 10 V;$ $T_j = 25 \text{ }^\circ C;$ <a href="#">Fig. 13; Fig. 14</a>	-	21.8	-	nC
$Q_{GS}$	gate-source charge		-	5.9	-	nC
$Q_{GD}$	gate-drain charge		-	7.8	-	nC

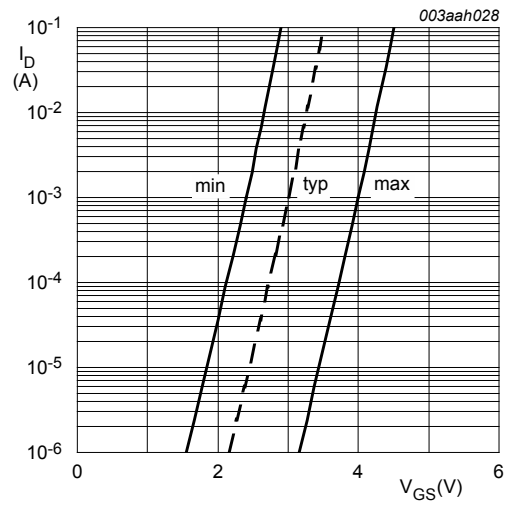
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz};$	-	1079	1439	pF
$C_{oss}$	output capacitance	$T_j = 25\text{ °C};$ <a href="#">Fig. 15</a>	-	235	282	pF
$C_{rss}$	reverse transfer capacitance		-	149	204	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 32\text{ V}; R_L = 2.4\text{ }\Omega; V_{GS} = 10\text{ V};$	-	7.4	-	ns
$t_r$	rise time	$R_{G(ext)} = 5\text{ }\Omega; T_j = 25\text{ °C}; I_D = 15\text{ A}$	-	12	-	ns
$t_{d(off)}$	turn-off delay time		-	13.8	-	ns
$t_f$	fall time		-	10.3	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 15\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ °C};$ <a href="#">Fig. 16</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 15\text{ A}; di_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$	-	20.3	-	ns
$Q_r$	recovered charge	$V_{DS} = 20\text{ V}; T_j = 25\text{ °C}$	-	11.7	-	nC





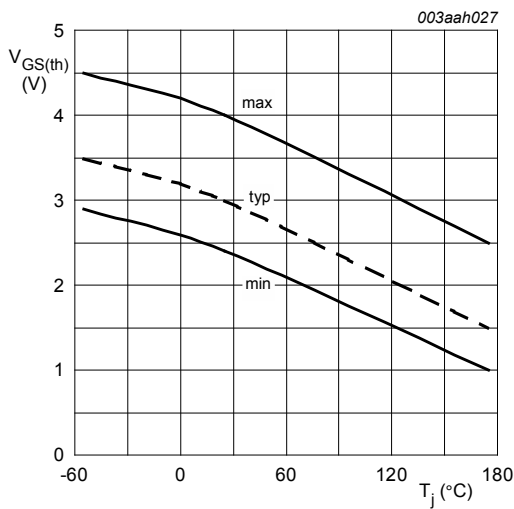
**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values**

$V_{DS} = 10V$



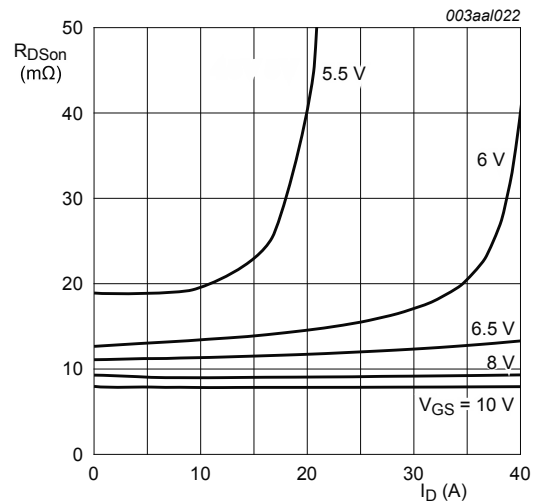
**Fig. 9. Sub-threshold drain current as a function of gate-source voltage**

$T_j = 25^\circ C; V_{DS} = 5V$



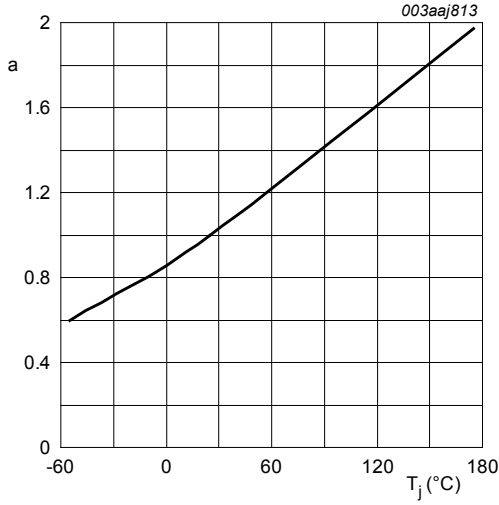
**Fig. 10. Gate-source threshold voltage as a function of junction temperature**

$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

$T_j = 25^\circ C; t_p = 300 \mu s$

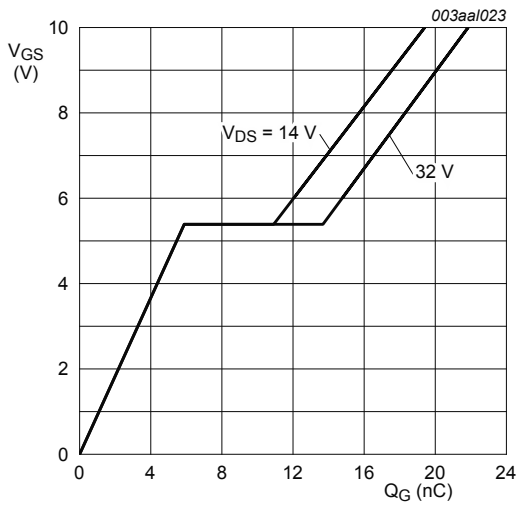


**Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

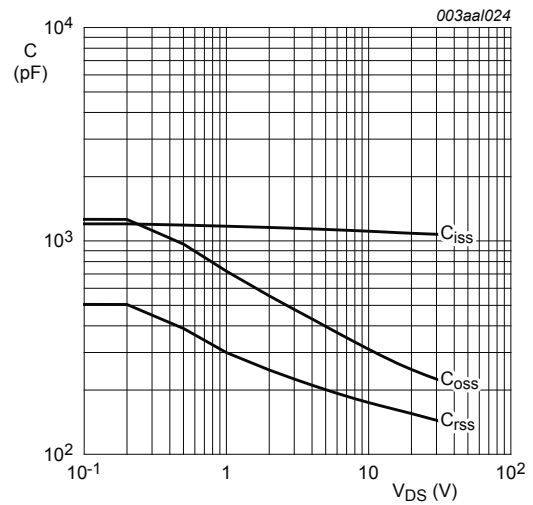


**Fig. 13. Gate charge waveform definitions**



**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

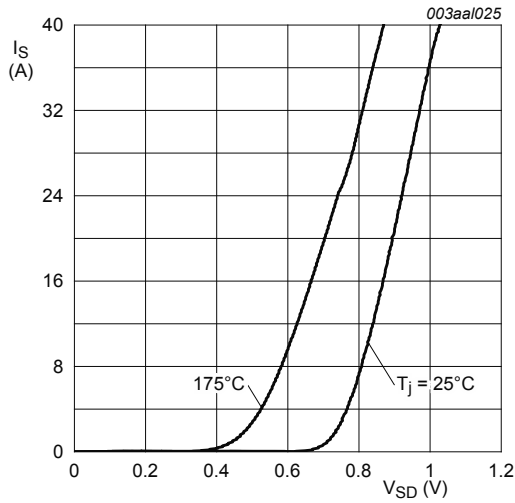
$$T_j = 25^\circ\text{C}; I_D = 15\text{A}$$



**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**

$$V_{GS} = 0\text{V}; f = 1\text{MHz}$$

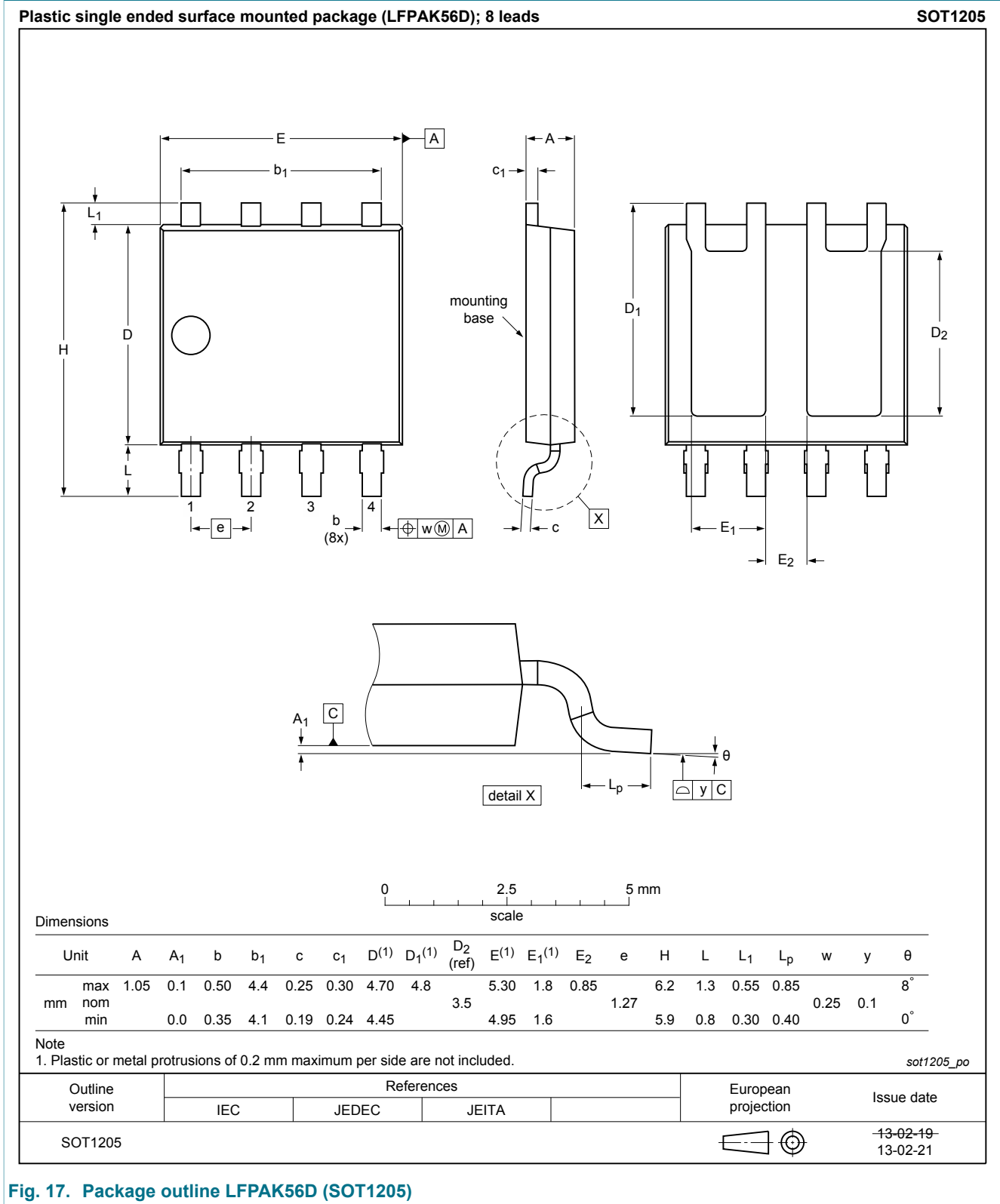




**Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values**

$$V_{GS} = 0V$$

### 11. Package outline



**Fig. 17. Package outline LPAK56D (SOT1205)**

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions".
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