

BUK7Y9R9-80E

N-channel 80 V, 9.9 mΩ standard level MOSFET in LFPAK56
8 May 2013 Product data sheet

1. General description

Standard level N-channel MOSFET in an LFPAK56 (Power SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC Q101 standard for use in high performance automotive applications.

2. Features and benefits

- Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True standard level gate with V_{GS(th)} rating of greater than 1 V at 175 °C

3. Applications

- 12 V, 24 V and 48 V Automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Тур	Max	Unit
V _{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C		-	-	80	V
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; <u>Fig. 1</u>		-	-	89	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>		-	-	195	W
Static characte	Static characteristics						
R _{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; Fig. 11		-	7.3	9.9	mΩ
Dynamic characteristics							
Q_{GD}	gate-drain charge	V _{GS} = 10 V; I _D = 25 A; V _{DS} = 64 V; Fig. 13; Fig. 14		-	14.4	-	nC



5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	mb	D
2	S	source		
3	S	source	q	G_U: 4
4	G	gate	و ق ق ق	mbb076 S
mb	D	mounting base; connected to drain	1 2 3 4 LFPAK56; Power- SO8 (SOT669)	

6. Ordering information

Table 3. Ordering information

Type number	Package				
	Name	Description	Version		
BUK7Y9R9-80E	LFPAK56; Power-SO8	Plastic single-ended surface-mounted package (LFPAK56; Power-SO8); 4 leads	SOT669		

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK7Y9R9-80E	79E980

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	T _j ≥ 25 °C; T _j ≤ 175 °C	-	80	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 k Ω	-	80	V
V_{GS}	gate-source voltage	T _j ≤ 175 °C; DC	-20	20	V
I _D	drain current	T _{mb} = 25 °C; V _{GS} = 10 V; <u>Fig. 1</u>	-	89	Α
		T _{mb} = 100 °C; V _{GS} = 10 V; <u>Fig. 1</u>	-	63	Α
I _{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \le 10 \mu s$; Fig. 4	-	354	Α
P _{tot}	total power dissipation	T _{mb} = 25 °C; <u>Fig. 2</u>	-	195	W
T _{stg}	storage temperature		-55	175	°C

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Symbol	Parameter	Conditions		Min	Max	Unit
Tj	junction temperature			-55	175	°C
Source-drai	in diode					
I _S	source current	T _{mb} = 25 °C		-	89	Α
I _{SM}	peak source current	pulsed; $t_p \le 10 \ \mu s$; $T_{mb} = 25 \ ^{\circ}C$		-	354	Α
Avalanche i	ruggedness		'			
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I_D = 89 A; $V_{sup} \le 80$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 3	[1][2]	-	106	mJ

- [1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [2] Refer to application note AN10273 for further information.

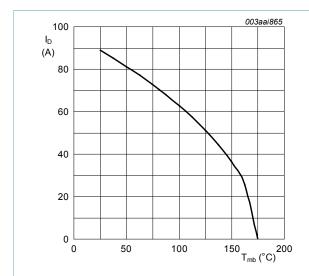


Fig. 1. Continuous drain current as a function of mounting base temperature

$$V_{GS} \ge 10V$$

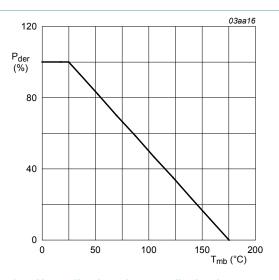


Fig. 2. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

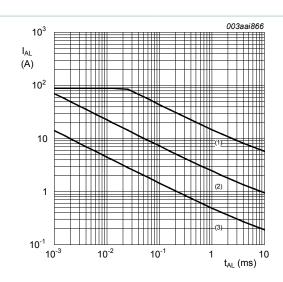
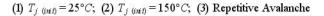


Fig. 3. Avalanche rating; avalanche current as a function of avalanche time



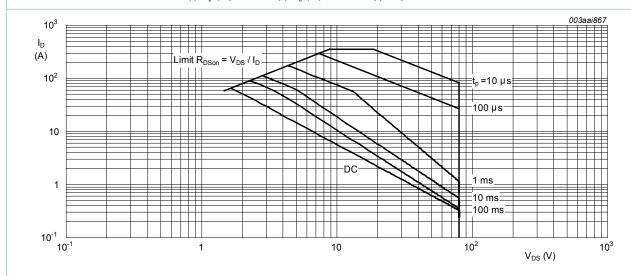


Fig. 4. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

 $T_{mb} = 25^{\circ}C$; I_{DM} is a single pulse

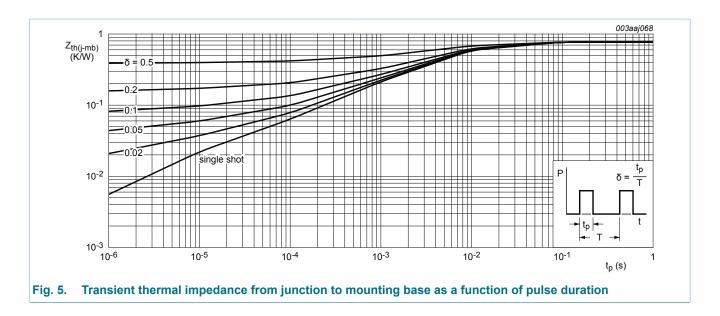
9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R _{th(j-mb)}	thermal resistance from junction to mounting base	Fig. 5	-	_	0.77	K/W

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10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static chara	acteristics					
V _{(BR)DSS}	drain-source	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 °C$	80	-	-	V
	breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 °C$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; Fig. 9; Fig. 10	2.4	3	4	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ °C};$ Fig. 9	-	-	4.5	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ °C};$ Fig. 9	1	-	-	V
I _{DSS}	drain leakage current	V _{DS} = 80 V; V _{GS} = 0 V; T _j = 25 °C	-	0.13	10	μA
		V _{DS} = 80 V; V _{GS} = 0 V; T _j = 175 °C	-	-	500	μA
I _{GSS}	gate leakage current	V _{GS} = 20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
		V _{GS} = -20 V; V _{DS} = 0 V; T _j = 25 °C	-	2	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 11; Fig. 12	-	-	24.9	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	-	7.3	9.9	mΩ
Dynamic ch	naracteristics				'	
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 64 V; V _{GS} = 10 V;	-	51.6	-	nC
Q _{GS}	gate-source charge	Fig. 13; Fig. 14	-	14.1	-	nC
Q _{GD}	gate-drain charge		-	14.4	-	nC

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Symbol	Parameter	Conditions		Min	Тур	Max	Unit
C _{iss}	input capacitance	$V_{GS} = 0 \text{ V; } V_{DS} = 25 \text{ V; } f = 1 \text{ MHz;}$ $T_j = 25 \text{ °C; } Fig. 15$		-	3200	4266	pF
C _{oss}	output capacitance			-	303	364	pF
C _{rss}	reverse transfer capacitance			-	165	226	pF
t _{d(on)}	turn-on delay time	V_{DS} = 60 V; R_{L} = 2.4 Ω ; V_{GS} = 10 V; $R_{G(ext)}$ = 5 Ω		-	15	-	ns
t _r	rise time			-	23	-	ns
t _{d(off)}	turn-off delay time			-	34	-	ns
t _f	fall time			-	21	-	ns
Source-dra	in diode	1		1			-1
V_{SD}	source-drain voltage	$I_S = 25 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 ^{\circ}\text{C}; Fig. 16$		-	0.83	1.2	V
t _{rr}	reverse recovery time	$I_S = 20 \text{ A}; dI_S/dt = -100 \text{ A/}\mu\text{s}; V_{GS} = 0 \text{ V};$		-	35	-	ns
Q _r	recovered charge	V _{DS} = 25 V		-	52	-	nC

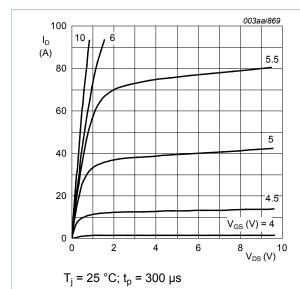


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

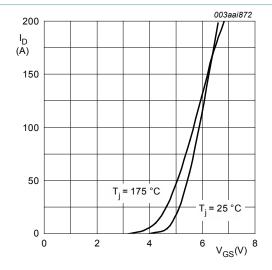


Fig. 7. Transfer characteristics; drain current as a function of gate-source voltage; typical values

$$V_{DS} = 10V$$

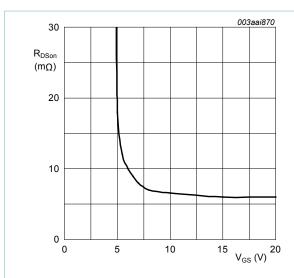


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

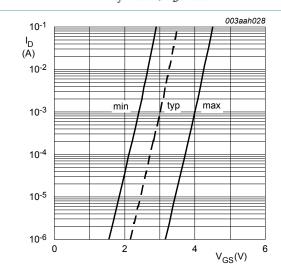


Fig. 10. Sub-threshold drain current as a function of gate-source voltage

$$T_j = 25$$
°C; $V_{DS} = 5V$

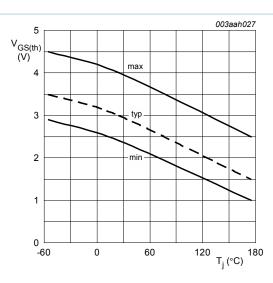


Fig. 9. Gate-source threshold voltage as a function of junction temperature

$$I_D = 1$$
 mA; $V_{DS} = V_{GS}$

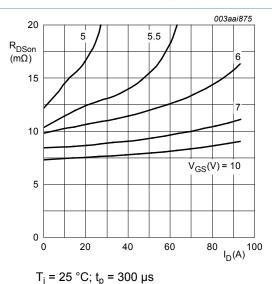


Fig. 11. Drain-source on-state resistance as a function of drain current; typical values

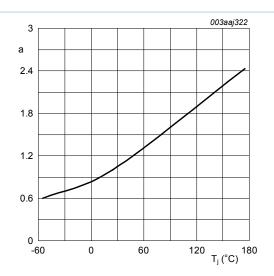


Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon (25^{\circ}C)}}$$

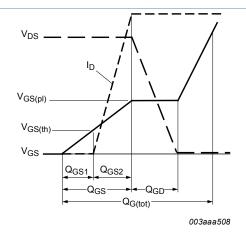


Fig. 14. Gate charge waveform definitions

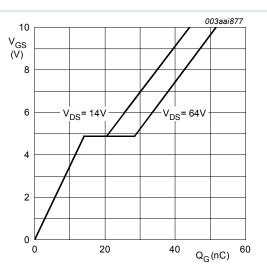


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$$T_j = 25^{\circ}C; I_D = 25A$$

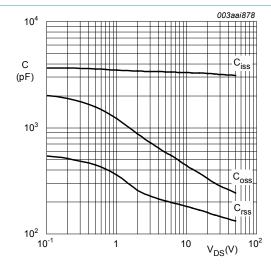


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$$V_{GS} = \mathbf{0}V; f = \mathbf{1}MHz$$

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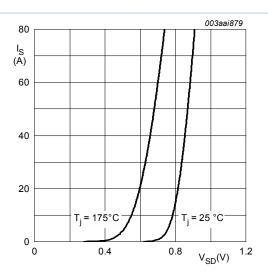
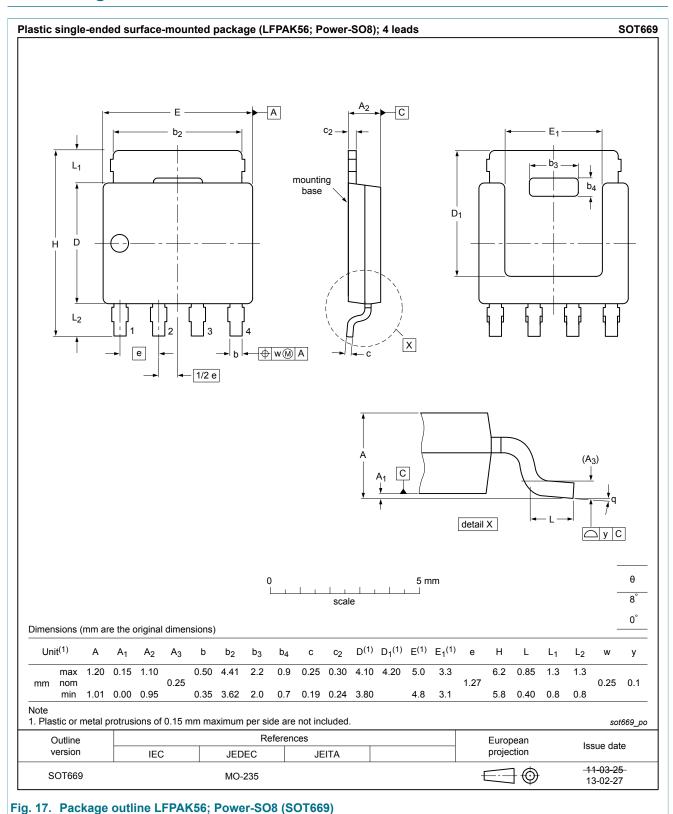


Fig. 16. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

$$V_{GS} = 0V$$

11. Package outline



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