BUK9675-100A

N-channel TrenchMOS logic level FET

18 August 2015 | Product data sheet

1. General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

2. Features and benefits

- AEC Q101 compliant
- Low conduction losses due to low on-state resistance

3. Applications

- Automotive and general purpose power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	-	100	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; Fig. 2		-	-	23	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; Fig. 1		-	-	98	W
Static characteristics							
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 10$ A; $T_j = 25$ °C; Fig. 12		-	55	72	mΩ
		$V_{GS} = 5$ V; $I_D = 10$ A; $T_j = 25$ °C; Fig. 12		-	60	75	mΩ
Avalanche ruggedness							
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 23$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped; Fig. 4	[1][2]	-	-	100	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.

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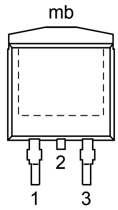
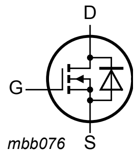
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 D2PAK (SOT404)	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9675-100A	D2PAK	plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)	SOT404

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9675-100A	BUK9675-100A

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C		-	100	V
V_{DGR}	drain-gate voltage	R_{GS} = 20 kΩ		-	100	V
V_{GS}	gate-source voltage			-15	15	V
P_{tot}	total power dissipation	T_{mb} = 25 °C; Fig. 1		-	98	W
I_D	drain current	T_{mb} = 100 °C; V_{GS} = 5 V; Fig. 2		-	16	A
		T_{mb} = 25 °C; V_{GS} = 5 V; Fig. 2		-	23	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Fig. 3		-	92	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
Source-drain diode						
I_S	source current	T_{mb} = 25 °C		-	23	A
I_{SM}	peak source current	pulsed; t_p ≤ 10 µs; T_{mb} = 25 °C		-	92	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	I_D = 23 A; V_{sup} ≤ 100 V; R_{GS} = 50 Ω; V_{GS} = 5 V; $T_{j(init)}$ = 25 °C; unclamped; Fig. 4	[1][2]	-	100	mJ

[1] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
[2] Refer to application note AN10273 for further information.

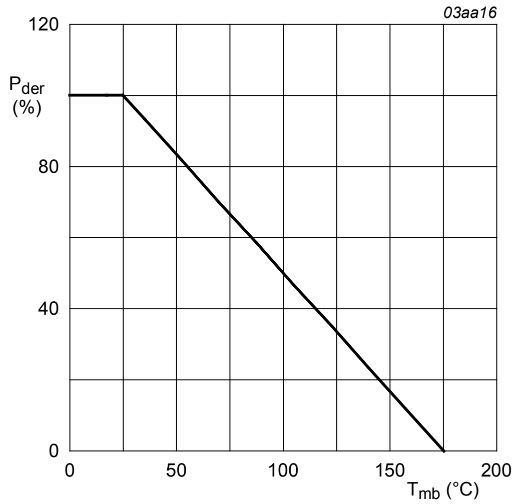
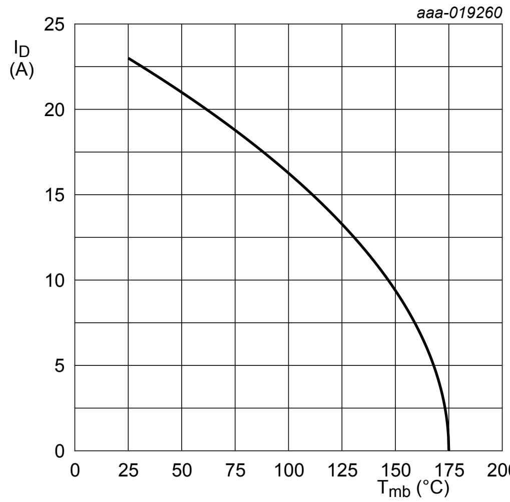


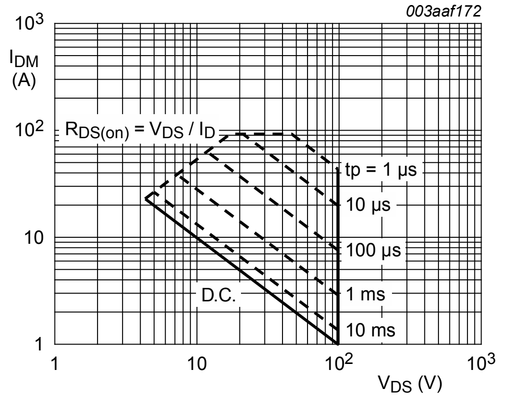
Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$



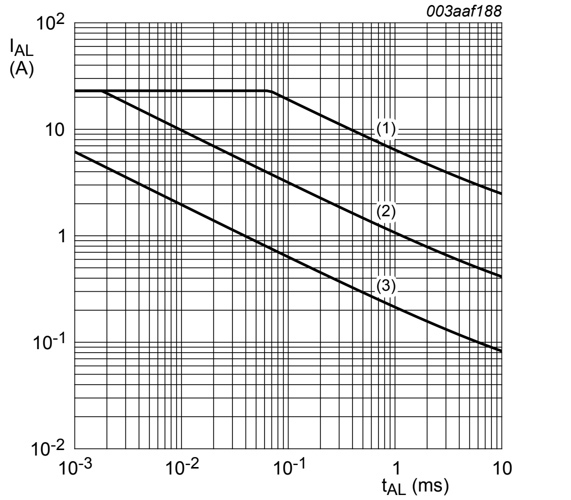
V_{GS} ≥ 5V

Fig. 2. Continuous drain current as a function of mounting base temperature



T_{mb} = 25 °C; I_{DM} is single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage



(1) $T_{j\ (init)}$ = 25°C; (2) $T_{j\ (init)}$ = 150°C; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base			-	-	1.5	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; FR4 board		-	50	-	K/W

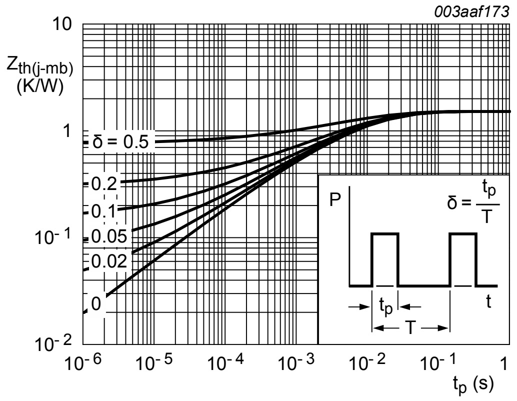


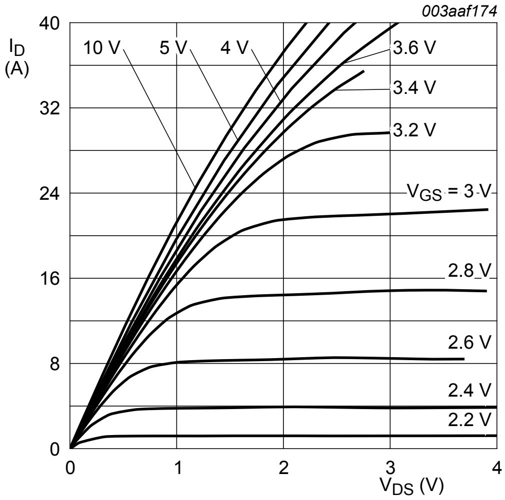
Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

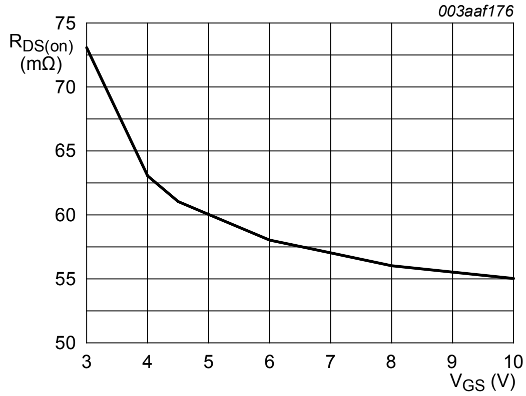
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C		100	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C		89	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; Fig. 10		0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; Fig. 10; Fig. 11		1	1.5	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; Fig. 10		-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C		-	-	500	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C		-	0.05	10	µA
I_{GSS}	gate leakage current	V_{GS} = 10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
		V_{GS} = -10 V; V_{DS} = 0 V; T_j = 25 °C		-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 10 A; T_j = 25 °C; Fig. 12		-	55	72	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 175 °C; Fig. 13		-	-	188	mΩ
		V_{GS} = 4.5 V; I_D = 10 A; T_j = 25 °C; Fig. 12		-	61	84	mΩ
		V_{GS} = 5 V; I_D = 10 A; T_j = 25 °C; Fig. 12		-	60	75	mΩ
Dynamic characteristics							
$Q_{G(tot)}$	total gate charge	I_D = 10 A; V_{DS} = 80 V; V_{GS} = 5 V; Fig. 14; Fig. 15		-	24.3	-	nC
Q_{GS}	gate-source charge			-	3	-	nC
Q_{GD}	gate-drain charge			-	12.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; Fig. 16		-	1278	1704	pF
C_{oss}	output capacitance			-	129	155	pF
C_{rss}	reverse transfer capacitance			-	88	120	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C		-	13	20	ns
t_r	rise time			-	120	168	ns
$t_{d(off)}$	turn-off delay time			-	58	87	ns
t_f	fall time			-	57	86	ns
L_D	internal drain inductance	from drain lead 6 mm from package to centre of die; T_j = 25 °C		-	4.5	-	nH

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		from upper edge of drain tab to centre of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; T_j = 25 °C	-	7.5	-	nH
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 10 A; V_{GS} = 0 V; T_j = 25 °C; Fig. 17	-	0.85	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C	-	53.7	-	ns
Q_r	recovered charge		-	126	-	nC



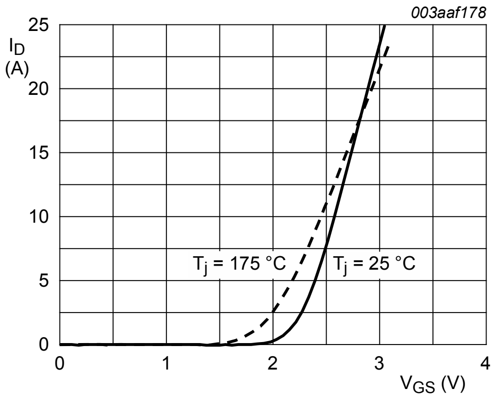
T_j = 25 °C

Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values



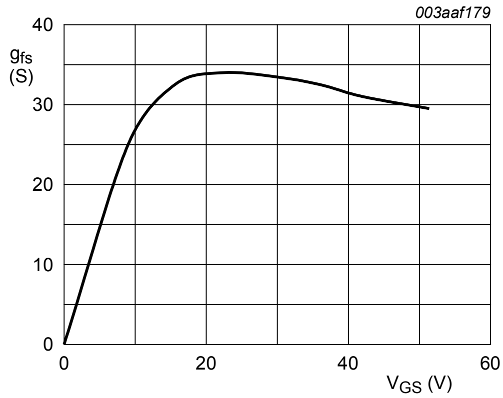
T_j = 25 °C; I_D = 25 A

Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig. 8. Transfer characteristics: drain current as a function of gate-source voltage; typical values



$V_{DS} > I_D \times R_{DSon}$

Fig. 9. Forward transconductance as a function of drain current; typical values

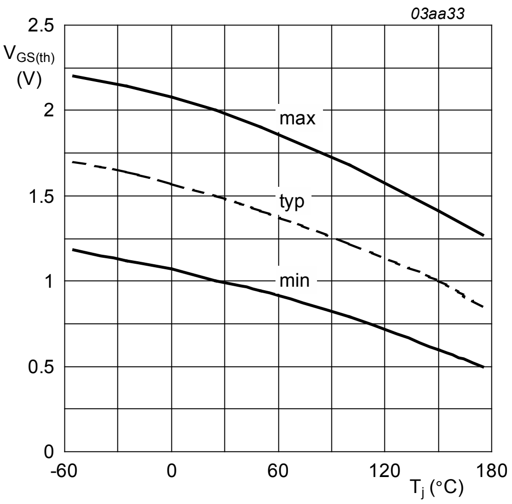
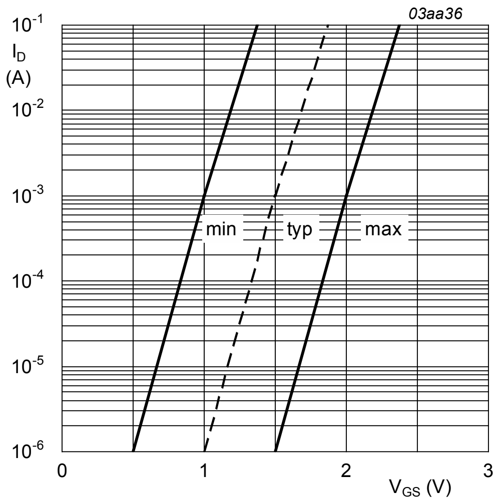


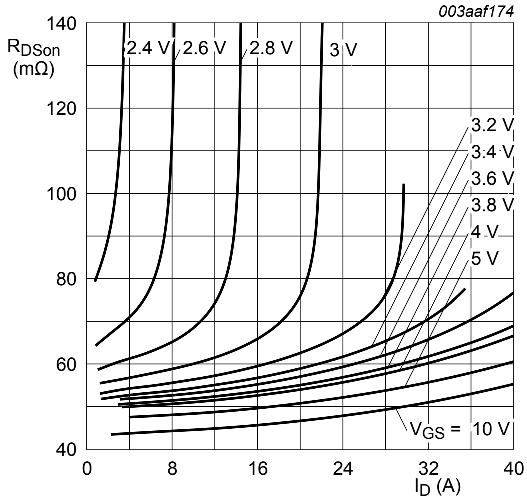
Fig. 10. Gate-source threshold voltage as a function of junction temperature

$I_D = 1 mA; V_{DS} = V_{GS}$



T_j = 25 °C; V_{DS} = 5 V

Fig. 11. Sub-threshold drain current as a function of gate-source voltage



T_j = 25 °C

Fig. 12. Drain-source on-state resistance as a function of drain current; typical values

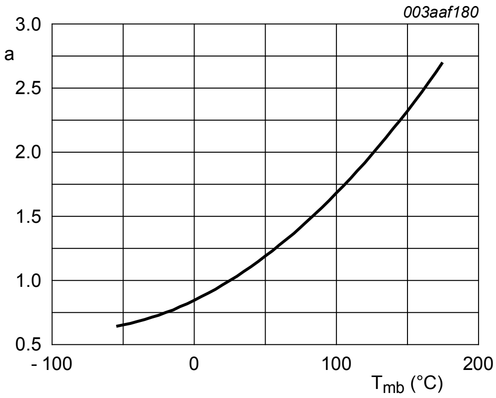


Fig. 13. Normalized drain-source on-state resistance factor as a function of junction temperature

$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

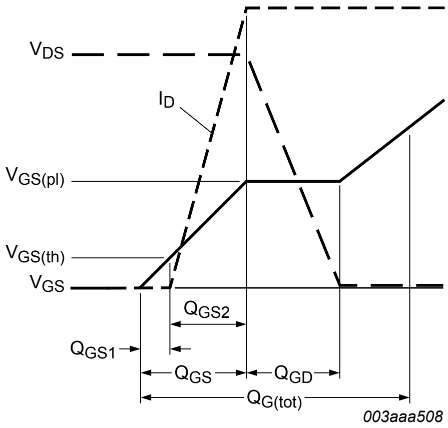
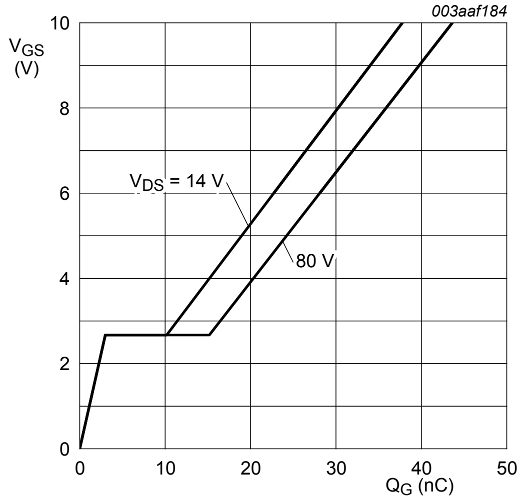
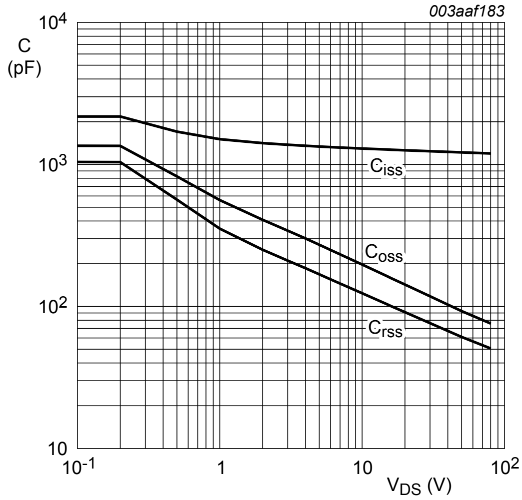


Fig. 14. Gate charge waveform definitions



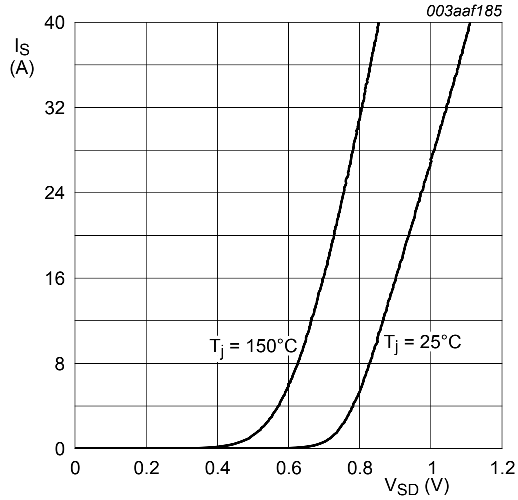
T_j = 25 °C; I_D = 10 A

Fig. 15. Gate-source voltage as a function of gate charge; typical values



V_{GS} = 0 V; f = 1 MHz

Fig. 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

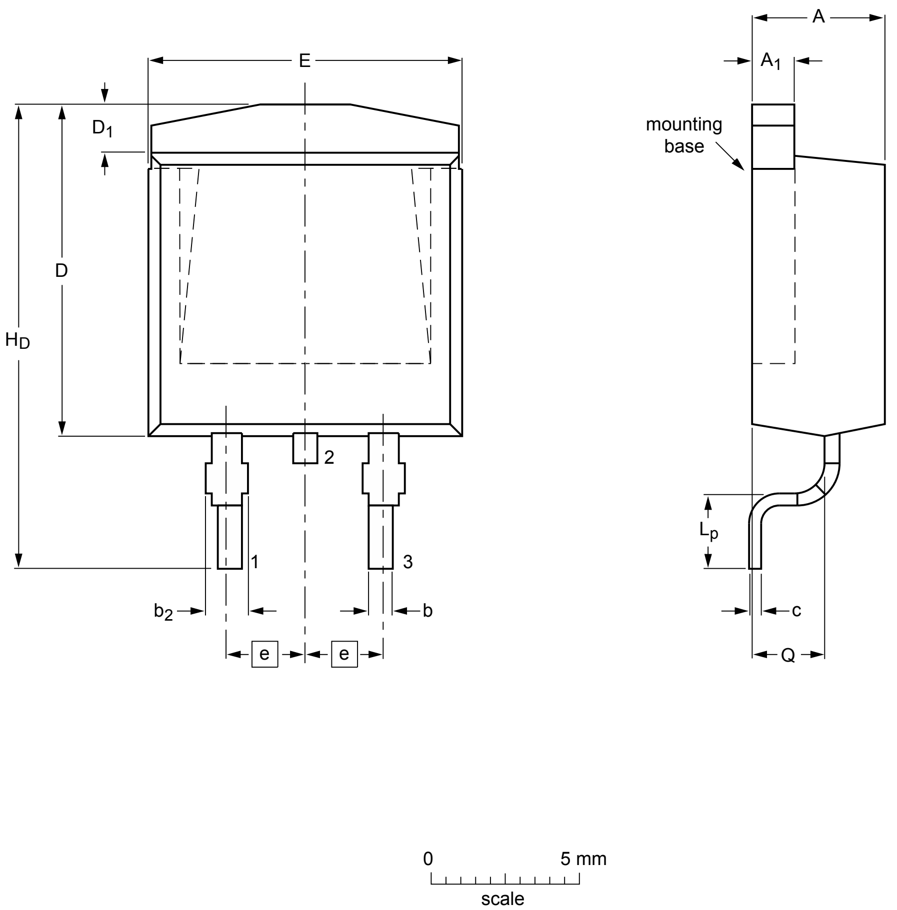


V_{GS} = 0 V

Fig. 17. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values

11. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) **SOT404**



Dimensions (mm are the original dimensions)

Unit		A	A_1	b	b_2	c	D	D_1	E	e	H_D	L_p	Q
mm	max	4.5	1.40	0.85	1.45	0.64	11	1.6	10.3		15.8	2.9	2.6
	nom									2.54			
	min	4.1	1.27	0.60	1.05	0.46		1.2	9.7		14.8	2.1	2.2

sot404_po

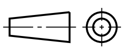
Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT404						~~06-03-16~~ 13-02-25

Fig. 18. Package outline D2PAK (SOT404)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
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13. Contents

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Date of release: 18 August 2015