



# BUK9K30-80E

Dual N-channel 80 V, 30 mΩ logic level MOSFET

12 May 2018

Product data sheet

## 1. General description

Dual Logic level N-channel MOSFET in an LPAK56D (Dual Power-SO8) package using TrenchMOS technology. This product has been designed and qualified to AEC-Q101 standard for use in high performance automotive applications.

## 2. Features and benefits

- Dual MOSFET
- AEC-Q101 compliant
- Repetitive avalanche rated
- Suitable for thermally demanding environments due to 175 °C rating
- True logic level gate with  $V_{GS(th)}$  rating of greater than 0.5 V at 175 °C

## 3. Applications

- 12 V, 24 V and 48 V automotive systems
- Motors, lamps and solenoid control
- Transmission control
- Ultra high performance power switching

## 4. Quick reference data

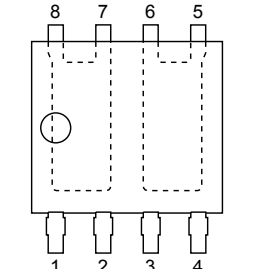
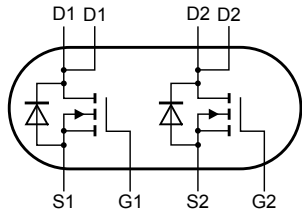
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Limiting values FET1 and FET2</b>						
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	-	80	V
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 2</a>	-	-	17	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <a href="#">Fig. 1</a>	-	-	53	W
<b>Static characteristics FET1 and FET2</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 5\text{ V}$ ; $I_D = 5\text{ A}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 11</a>	-	21	30	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{GD}$	gate-drain charge	$I_D = 5\text{ A}$ ; $V_{DS} = 64\text{ V}$ ; $V_{GS} = 5\text{ V}$ ; $T_j = 25\text{ °C}$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	6.2	-	nC
<b>Source-drain diode FET1 and FET2</b>						
$Q_r$	recovered charge	$I_S = 5\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$ ; $T_j = 25\text{ °C}$	-	30.8	-	nC

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## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source1	 <p>LFPAK56D (SOT1205)</p>	 <p>mbk725</p>
2	G1	gate1		
3	S2	source2		
4	G2	gate2		
5	D2	drain2		
6	D2	drain2		
7	D1	drain1		
8	D1	drain1		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BUK9K30-80E	LFPAK56D	plastic, single ended surface mounted package (LFPAK56D); 8 leads	SOT1205

## 7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9K30-80E	93080E

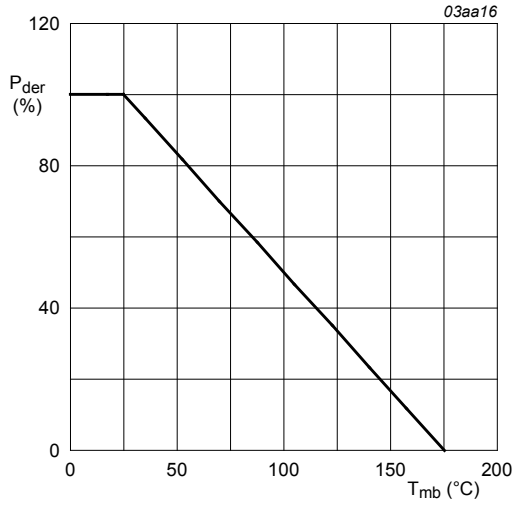
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

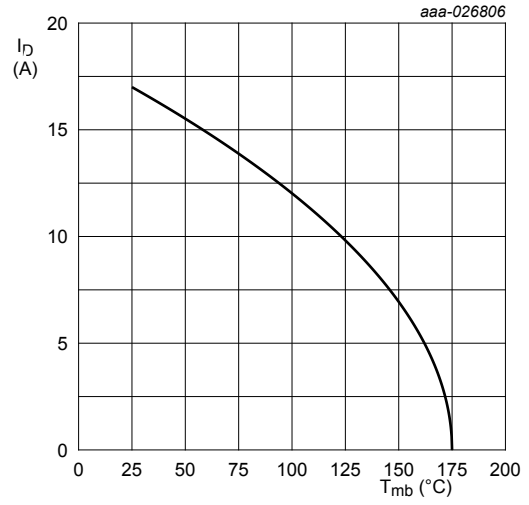
Symbol	Parameter	Conditions	Min	Max	Unit
<b>Limiting values FET1 and FET2</b>					
$V_{DS}$	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	80	V
$V_{DGR}$	drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	80	V
$V_{GS}$	gate-source voltage	DC; $T_j \leq 175\text{ °C}$	-10	10	V
		Pulsed; $T_j \leq 175\text{ °C}$	[1] [2] -15	15	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	53	W
$I_D$	drain current	$V_{GS} = 5\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2	-	17	A
		$V_{GS} = 5\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	-	12	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	68	A
$T_{stg}$	storage temperature		-55	175	°C
$T_j$	junction temperature		-55	175	°C
<b>Source-drain diode FET1 and FET2</b>					
$I_S$	source current	$T_{mb} = 25\text{ °C}$	-	17	A
$I_{SM}$	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$	-	68	A
<b>Avalanche ruggedness FET1 and FET2</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 17\text{ A}$ ; $V_{sup} \leq 80\text{ V}$ ; $R_{GS} = 50\text{ }\Omega$ ; $V_{GS} = 5\text{ V}$ ; $T_{j(init)} = 25\text{ °C}$ ; unclamped; Fig. 4	[3] [4] -	72	mJ

- [1] Accumulated Pulse duration up to 50 hours delivers zero defect ppm.  
 [2] Significantly longer life times are achieved by lowering  $T_j$  and or  $V_{GS}$ .  
 [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.  
 [4] Refer to application note AN10273 for further information.



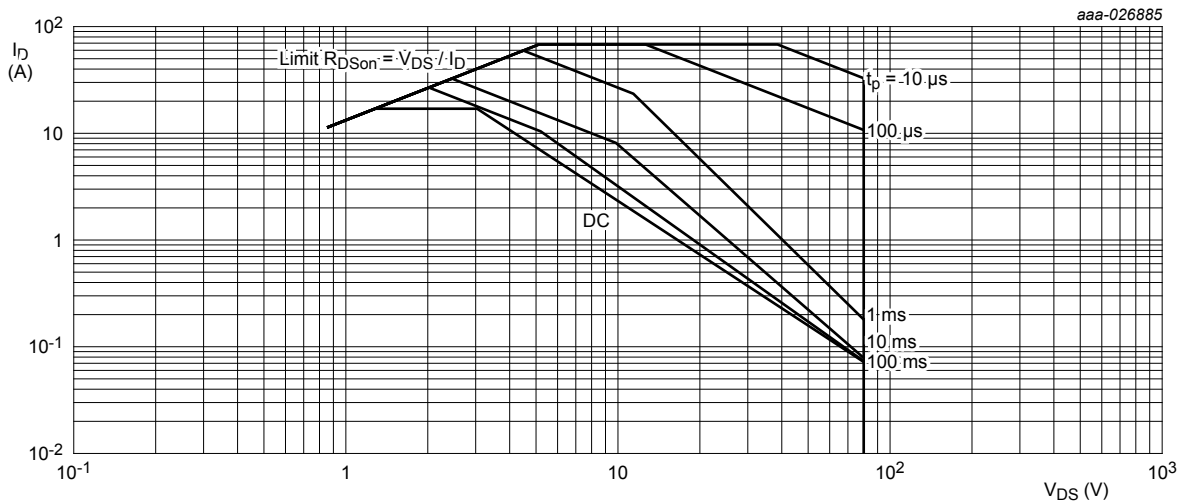
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig. 1. Normalized total power dissipation as a function of mounting base temperature**



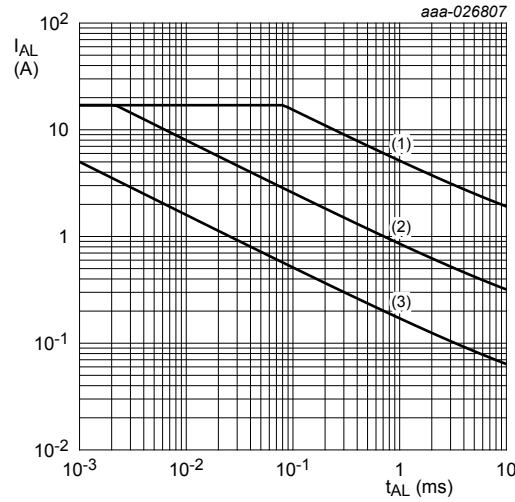
$V_{GS} \geq 5\text{ V}$

**Fig. 2. Continuous drain current as a function of mounting base temperature, FET1 and FET2**



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  is a single pulse

**Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage, FET1 and FET2**



(1)  $T_{j\text{ (init)}} = 25^{\circ}\text{C}$ ; (2)  $T_{j\text{ (init)}} = 150^{\circ}\text{C}$ ; (3) Repetitive Avalanche

Fig. 4. Avalanche rating; avalanche current as a function of avalanche time, FET1 and FET2

### 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	-	2.84	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Minimum footprint; mounted on a printed circuit board	-	95	-	K/W

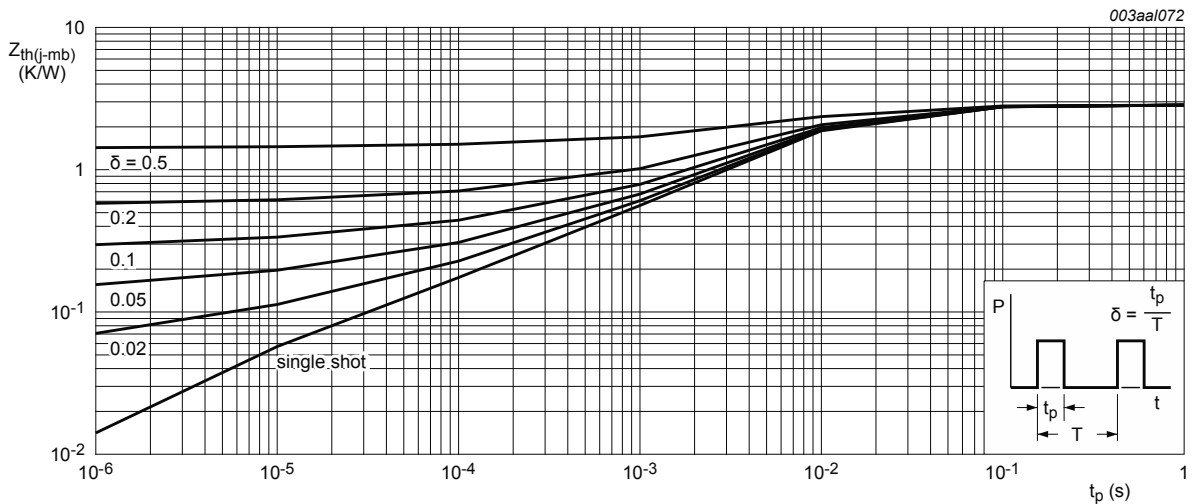
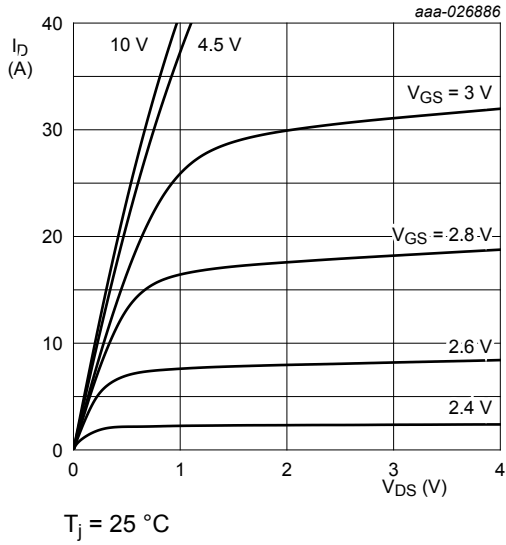


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration, FET1 and FET2

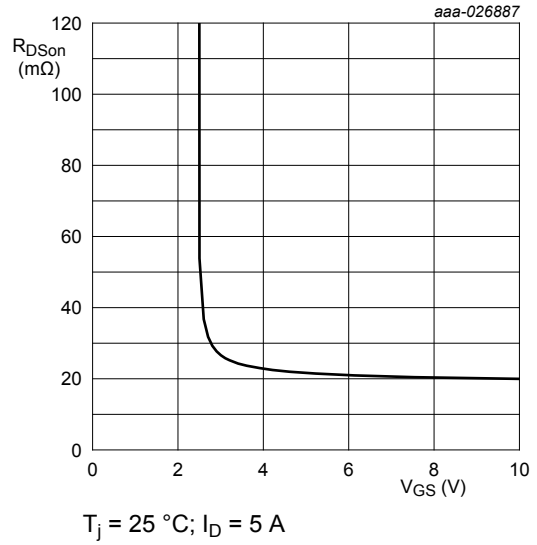
## 10. Characteristics

Table 7. Characteristics

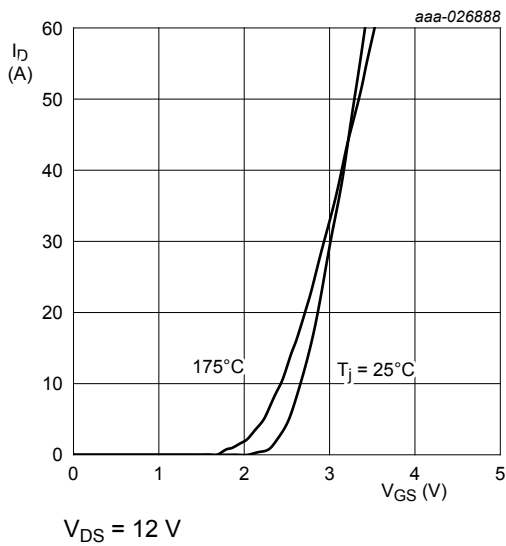
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics FET1 and FET2</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	80	-	-	V
		$I_D = 250 \mu\text{A}; V_{GS} = 0 \text{ V}; T_j = -55 \text{ }^\circ\text{C}$	72	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 9</a> ; <a href="#">Fig. 10</a>	1.4	1.7	2.1	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = -55 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	-	-	2.45	V
		$I_D = 1 \text{ mA}; V_{DS}=V_{GS}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 10</a>	0.5	-	-	V
$I_{DSS}$	drain leakage current	$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	0.01	1	$\mu\text{A}$
		$V_{DS} = 80 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ\text{C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	2	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	21	30	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 11</a>	-	20	26	mΩ
		$V_{GS} = 5 \text{ V}; I_D = 5 \text{ A}; T_j = 175 \text{ }^\circ\text{C};$ <a href="#">Fig. 12</a>	-	-	75	mΩ
<b>Dynamic characteristics FET1 and FET2</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 5 \text{ A}; V_{DS} = 64 \text{ V}; V_{GS} = 5 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	17.5	-	nC
$Q_{GS}$	gate-source charge		-	3.9	-	nC
$Q_{GD}$	gate-drain charge		-	6.2	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 25 \text{ V}; V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 15</a>	-	1727	2297	pF
$C_{oss}$	output capacitance		-	126	151	pF
$C_{rss}$	reverse transfer capacitance		-	68	93	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 60 \text{ V}; R_L = 12 \text{ }^\Omega; V_{GS} = 5 \text{ V}; R_{G(ext)} = 5 \text{ }^\Omega; T_j = 25 \text{ }^\circ\text{C}$	-	10.4	-	ns
$t_r$	rise time		-	14.8	-	ns
$t_{d(off)}$	turn-off delay time		-	24.7	-	ns
$t_f$	fall time		-	15	-	ns
<b>Source-drain diode FET1 and FET2</b>						
$V_{SD}$	source-drain voltage	$I_S = 5 \text{ A}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ\text{C};$ <a href="#">Fig. 16</a>	-	0.78	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 5 \text{ A}; dI_S/dt = -100 \text{ A}/\mu\text{s}; V_{GS} = 0 \text{ V}; V_{DS} = 25 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$	-	27.2	-	ns
$Q_r$	recovered charge		-	30.8	-	nC



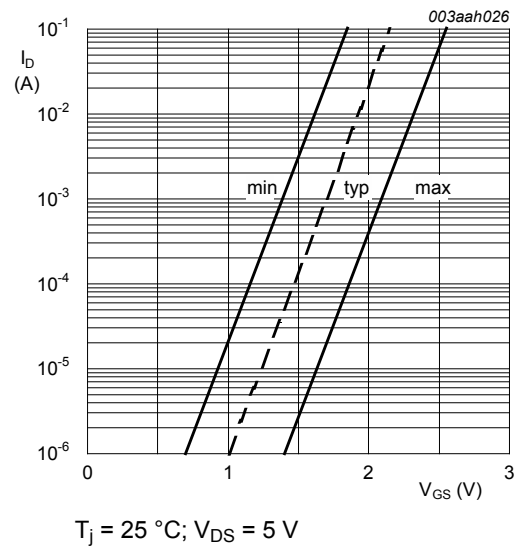
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values, FET1 and FET2**



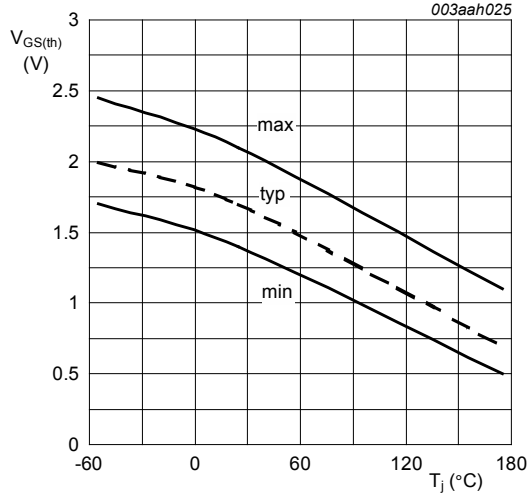
**Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values, FET1 and FET2**



**Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values, FET1 and FET2**

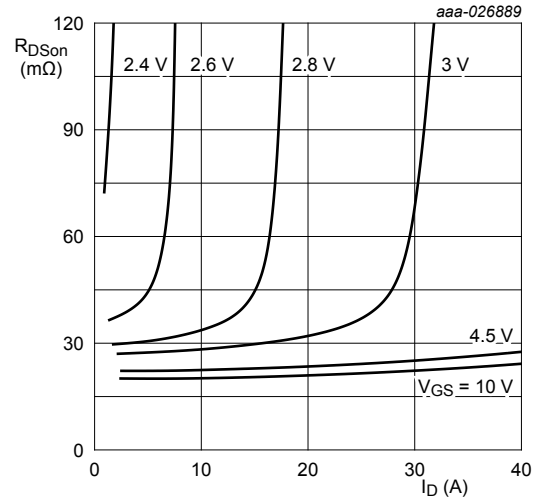


**Fig. 9. Sub-threshold drain current as a function of gate-source voltage, FET1 and FET2**



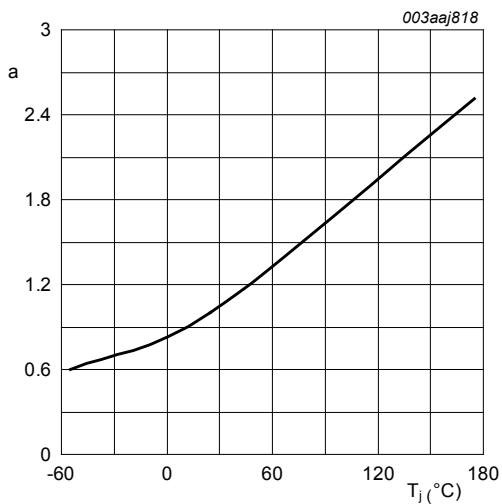
$I_D = 1 \text{ mA}$  ;  $V_{DS} = V_{GS}$

Fig. 10. Gate-source threshold voltage as a function of junction temperature, FET1 and FET2



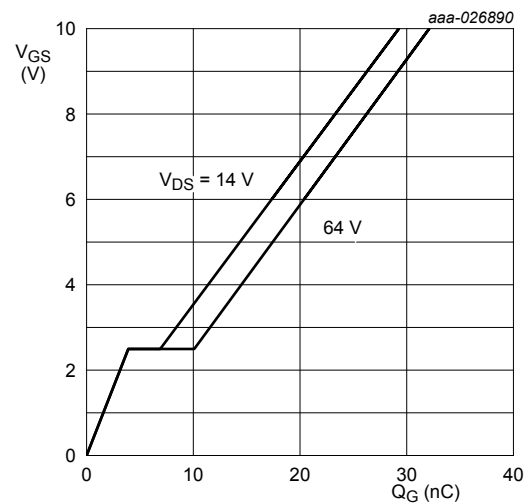
$T_j = 25 \text{ °C}$

Fig. 11. Drain-source on-state resistance as a function of drain current; typical values, FET1 and FET2



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

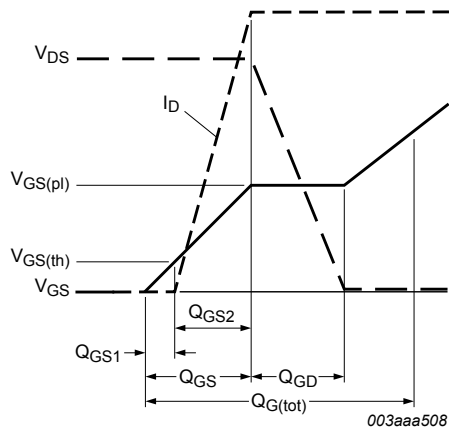
Fig. 12. Normalized drain-source on-state resistance factor as a function of junction temperature, FET1 and FET2



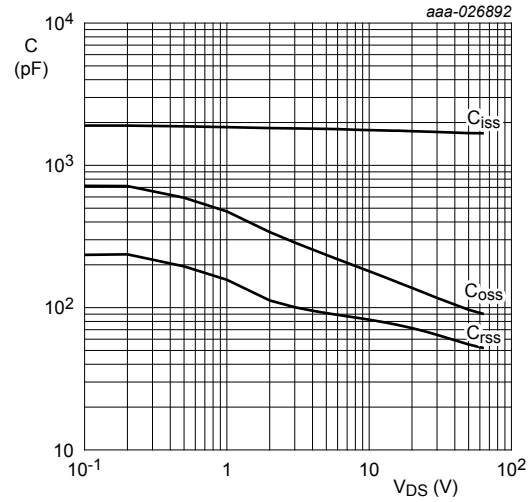
$T_j = 25 \text{ °C}$ ;  $I_D = 5 \text{ A}$

Fig. 13. Gate-source voltage as a function of gate charge; typical values, FET1 and FET2



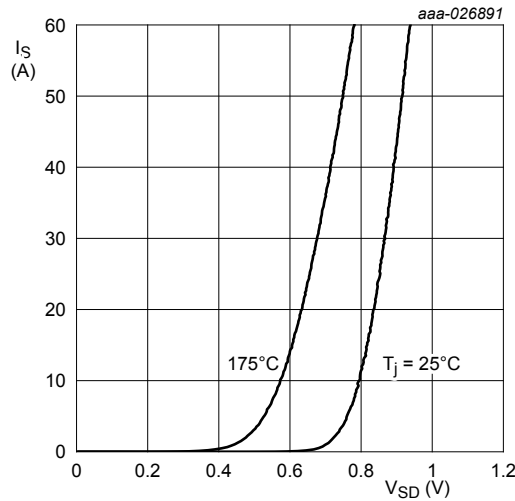


**Fig. 14. Gate charge waveform definitions**



$V_{GS} = 0$  V;  $f = 1$  MHz

**Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values, FET1 and FET2**



$V_{GS} = 0$  V

**Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values, FET1 and FET2**

### 11. Package outline

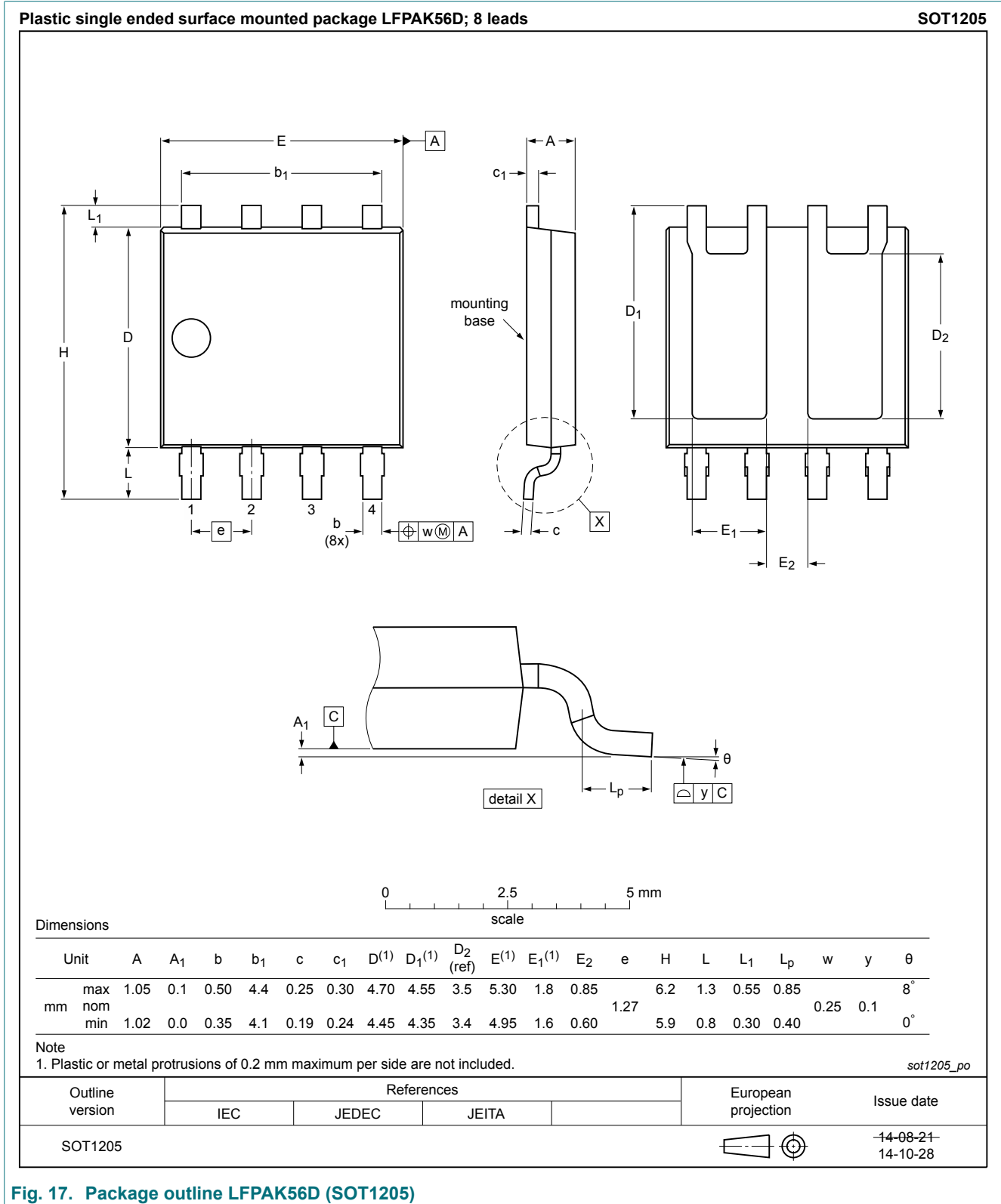


Fig. 17. Package outline LFAK56D (SOT1205)

## 12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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Date of release: 12 May 2018

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