



BUK9Y1R3-40H

N-channel 40 V, 1.3 mΩ logic level MOSFET in LFPAK56

31 May 2018

Product data sheet

1. General description

Automotive qualified N-channel MOSFET using the latest Trench 9 low ohmic superjunction technology, housed in a robust LFPAK56 package. This product has been fully designed and qualified to meet AEC-Q101 requirements delivering high performance and endurance.

2. Features and benefits

- Fully automotive qualified to AEC-Q101:
 - 175 °C rating suitable for thermally demanding environments
- Trench 9 Superjunction technology:
 - Reduced cell pitch enables enhanced power density and efficiency with lower R_{DSon} in same footprint
 - Improved SOA and avalanche capability compared to standard TrenchMOS
 - Tight $V_{GS(th)}$ limits enable easy paralleling of MOSFETs
- LFPAK Gull Wing leads:
 - High Board Level Reliability absorbing mechanical stress during thermal cycling, unlike traditional QFN packages
 - Visual (AOI) soldering inspection, no need for expensive x-ray equipment
 - Easy solder wetting for good mechanical solder joint
- LFPAK copper clip technology:
 - Improved reliability, with reduced R_{th} and R_{DSon}
 - Increases maximum current capability and improved current spreading

3. Applications

- 12 V automotive systems
- Motors, lamps and solenoid control
- Start-Stop micro-hybrid applications
- Transmission control
- Ultra high performance power switching

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	-	40	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C};$ Fig. 2	[1]	-	-	190	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C};$ Fig. 1		-	-	395	W

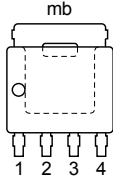
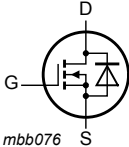
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Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	0.67	0.96	1.3	mΩ
Dynamic characteristics						
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 13 ; Fig. 14	-	11.2	22.4	nC
Source-drain diode						
Q _r	recovered charge	I _S = 25 A; di _S /dt = -100 A/μs; V _{GS} = 0 V;	-	38.8	-	nC
S	softness factor	V _{DS} = 20 V; T _j = 25 °C; Fig. 17	-	0.8	-	

[1] 190A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 <p>LFAK56; Power-SO8 (SOT669)</p>	 <p>mbb076 S</p>
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BUK9Y1R3-40H	LFAK56; Power-SO8	plastic, single-ended surface-mounted package; 4 terminals	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
BUK9Y1R3-40H	91H340

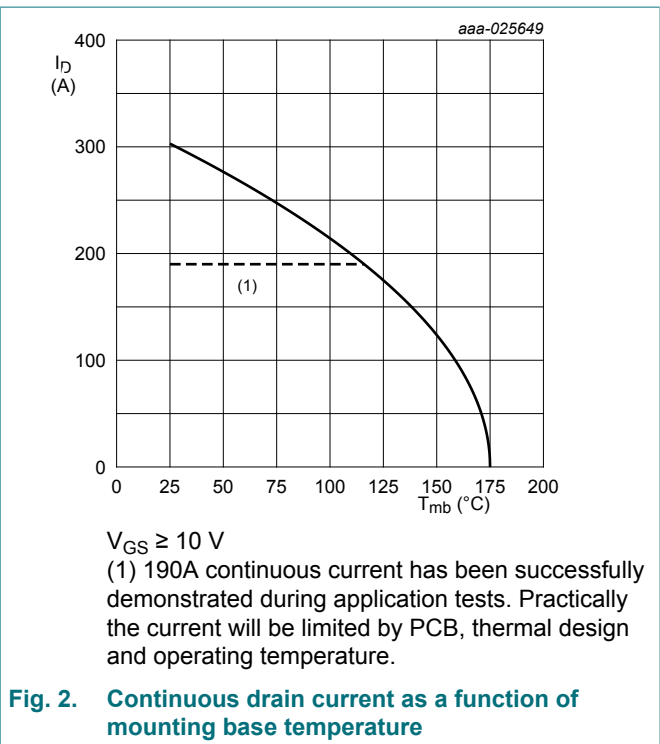
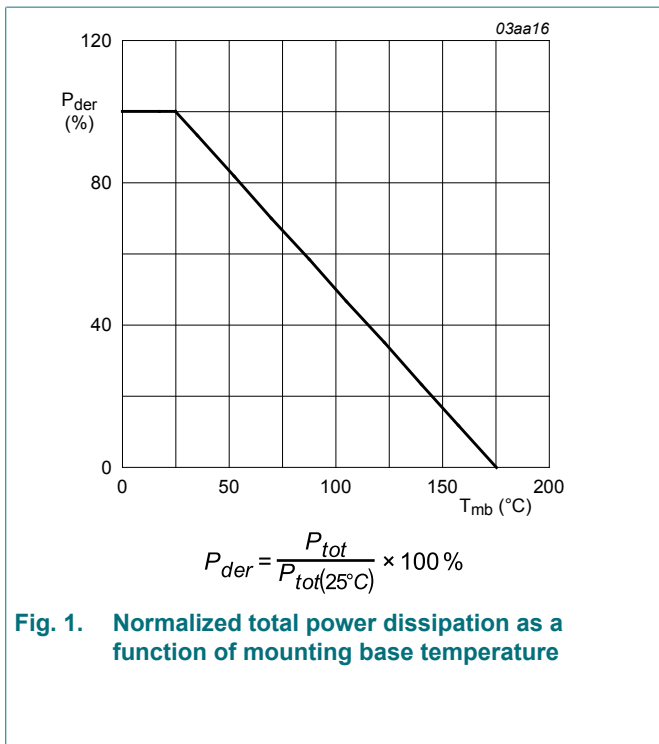
8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	25 °C ≤ T _j ≤ 175 °C		-	40	V
V _{GS}	gate-source voltage	DC; T _j ≤ 175 °C		-10	16	V
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	395	W
I _D	drain current	V _{GS} = 10 V; T _{mb} = 25 °C; Fig. 2	[1]	-	190	A
		V _{GS} = 10 V; T _{mb} = 100 °C; Fig. 2	[1]	-	190	A
I _{DM}	peak drain current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C; Fig. 3		-	600	A
T _{stg}	storage temperature			-55	175	°C
T _j	junction temperature			-55	175	°C
Source-drain diode						
I _S	source current	T _{mb} = 25 °C	[2]	-	145	A
I _{SM}	peak source current	pulsed; t _p ≤ 10 μs; T _{mb} = 25 °C		-	600	A
Avalanche ruggedness						
E _{DS(AL)S}	non-repetitive drain-source avalanche energy	I _D = 190 A; V _{sup} ≤ 40 V; R _{GS} = 50 Ω; V _{GS} = 10 V; T _{j(init)} = 25 °C; unclamped; Fig. 4	[3] [4]	-	154	mJ

- [1] 190A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
- [2] 145A continuous current has been successfully demonstrated during application tests. Practically the current will be limited by PCB, thermal design and operating temperature
- [3] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.
- [4] Refer to application note AN10273 for further information.



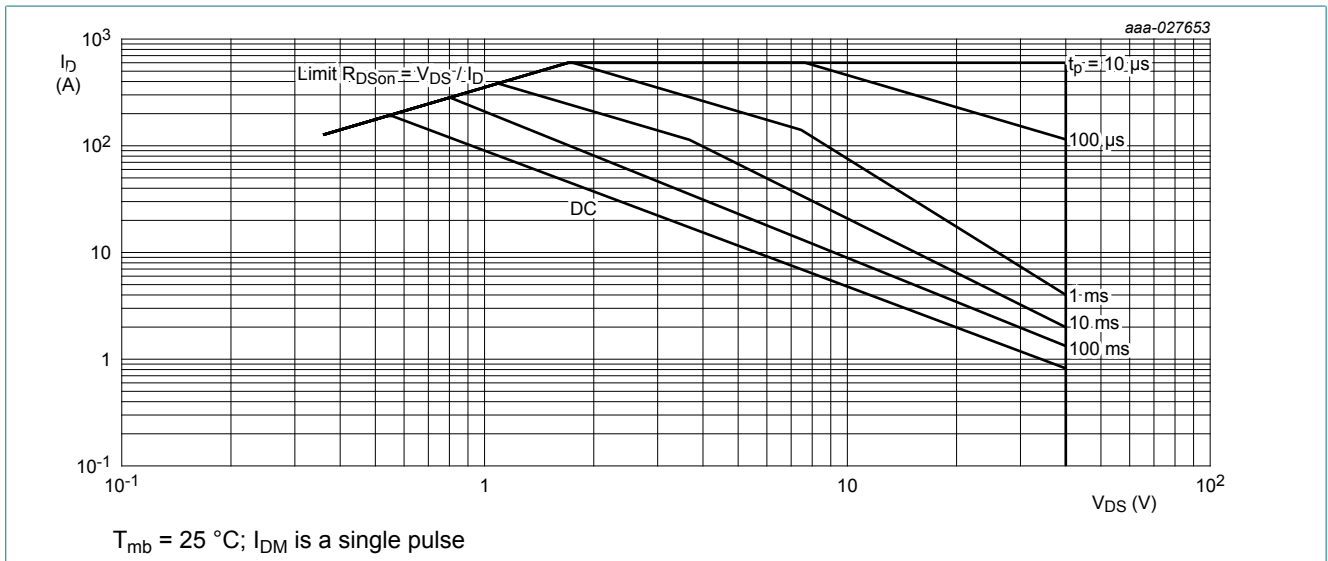


Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

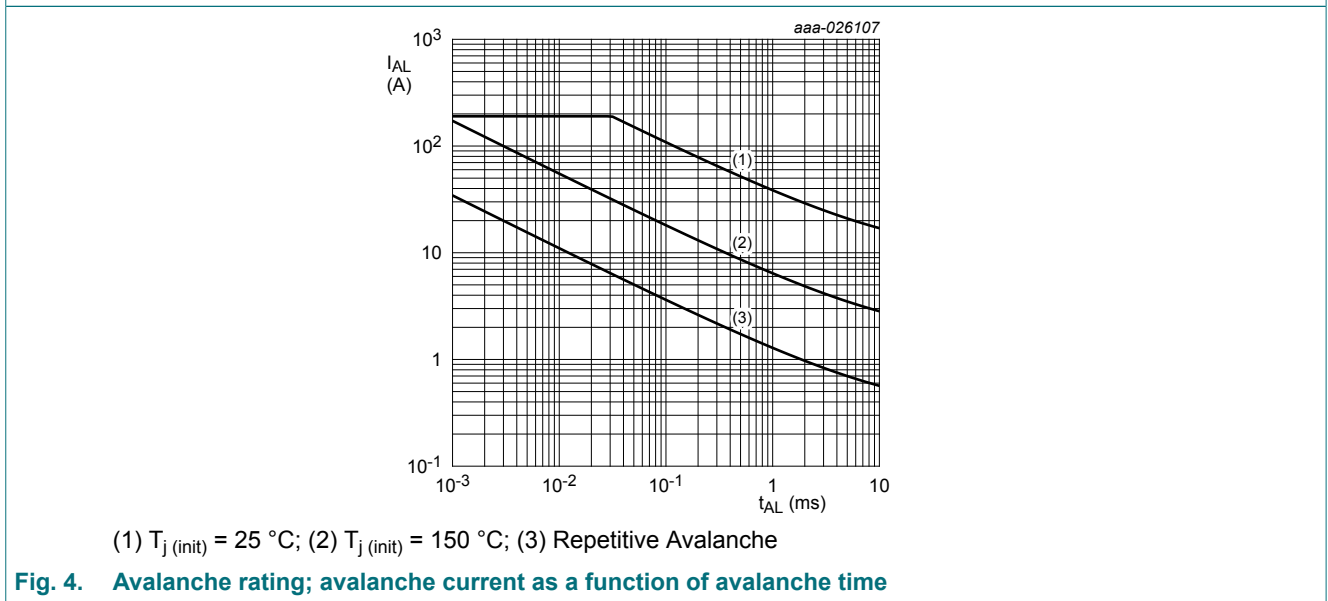


Fig. 4. Avalanche rating; avalanche current as a function of avalanche time

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 5	-	0.29	0.38	K/W

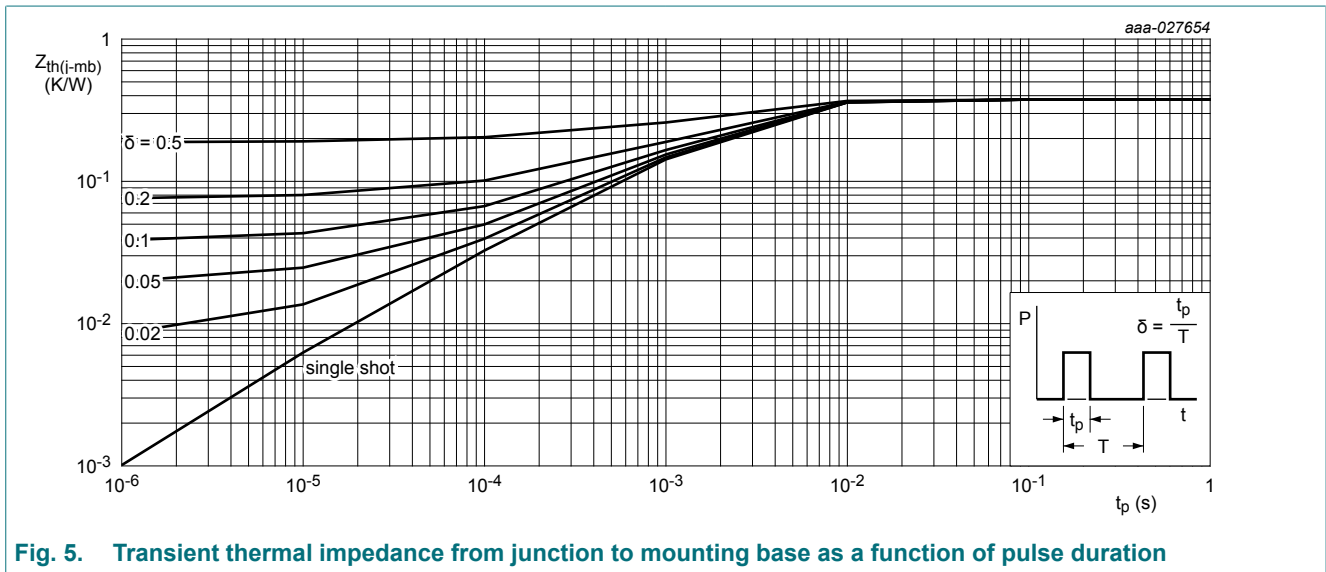


Fig. 5. Transient thermal impedance from junction to mounting base as a function of pulse duration

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	40	43	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -40 \text{ }^\circ C$	-	40.5	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	36	40	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C; \text{ Fig. 9}; \text{ Fig. 10}$	1.35	1.62	2.05	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C; \text{ Fig. 10}$	0.6	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C; \text{ Fig. 10}$	-	-	2.5	V
I_{DSS}	drain leakage current	$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	0.4	1	μA
		$V_{DS} = 16 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 125 \text{ }^\circ C$	-	2.4	10	μA
		$V_{DS} = 40 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 175 \text{ }^\circ C$	-	0.34	1	mA
I_{GSS}	gate leakage current	$V_{GS} = 16 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = -10 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ }^\circ C$	-	2	100	nA

N-channel 40 V, 1.3 mΩ logic level MOSFET in LPAK56

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 11	0.67	0.96	1.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 105 °C; Fig. 12	1	1.47	2.1	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 125 °C; Fig. 12	1.1	1.6	2.3	mΩ
		V _{GS} = 10 V; I _D = 25 A; T _j = 175 °C; Fig. 12	1.4	2.04	2.8	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 11	0.85	1.21	1.8	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 105 °C; Fig. 12	1.26	1.82	2.8	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 125 °C; Fig. 12	1.4	1.97	3.1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 175 °C; Fig. 12	1.76	2.5	3.9	mΩ
R _G	gate resistance	f = 1 MHz; T _j = 25 °C	0.58	1.46	3.65	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 20 V; V _{GS} = 10 V; Fig. 13 ; Fig. 14	-	99	139	nC
		I _D = 25 A; V _{DS} = 20 V; V _{GS} = 4.5 V; Fig. 13 ; Fig. 14	-	45.3	63.4	nC
Q _{GS}	gate-source charge		-	16.1	24.2	nC
Q _{GD}	gate-drain charge		-	11.2	22.4	nC
C _{iss}	input capacitance	V _{DS} = 25 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; Fig. 15	-	6978	9769	pF
C _{oss}	output capacitance		-	1244	1742	pF
C _{rss}	reverse transfer capacitance		-	269	592	pF
t _{d(on)}	turn-on delay time	V _{DS} = 20 V; R _L = 0.8 Ω; V _{GS} = 4.5 V; R _{G(ext)} = 5 Ω	-	36.3	-	ns
t _r	rise time		-	42.5	-	ns
t _{d(off)}	turn-off delay time		-	51.8	-	ns
t _f	fall time		-	30.7	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 25 A; V _{GS} = 0 V; T _j = 25 °C; Fig. 16	-	0.8	1.2	V
t _{rr}	reverse recovery time	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 17	-	38.7	-	ns
Q _r	recovered charge		-	38.8	-	nC
S	softness factor		-	0.8	-	
		I _S = 25 A; dI _S /dt = -500 A/μs; V _{GS} = 0 V; V _{DS} = 20 V; T _j = 25 °C; Fig. 17	-	0.72	-	

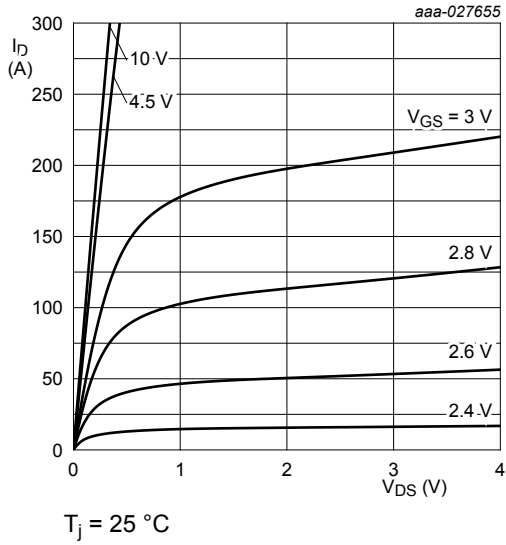


Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values

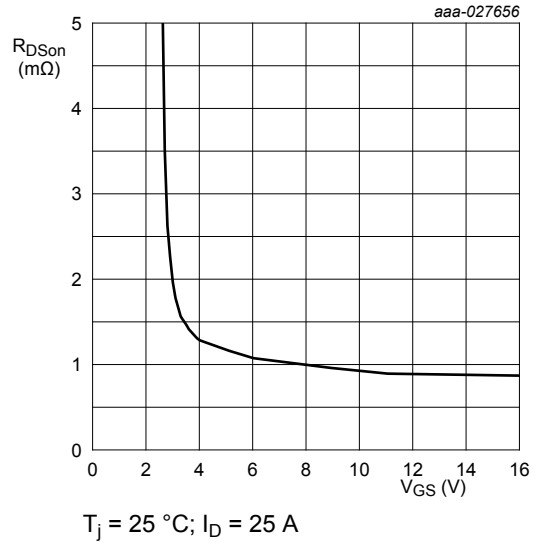


Fig. 7. Drain-source on-state resistance as a function of gate-source voltage; typical values

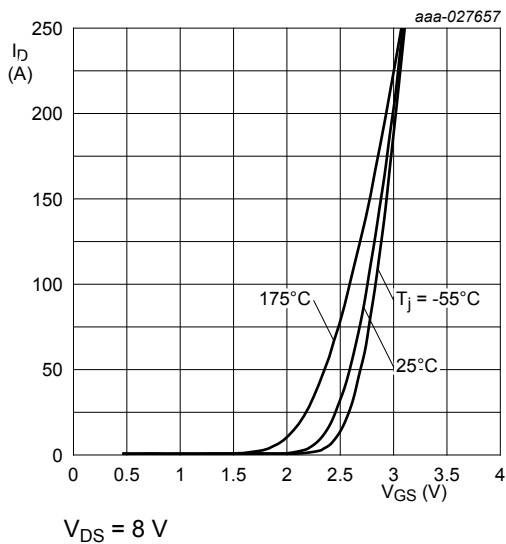


Fig. 8. Transfer characteristics; drain current as a function of gate-source voltage; typical values

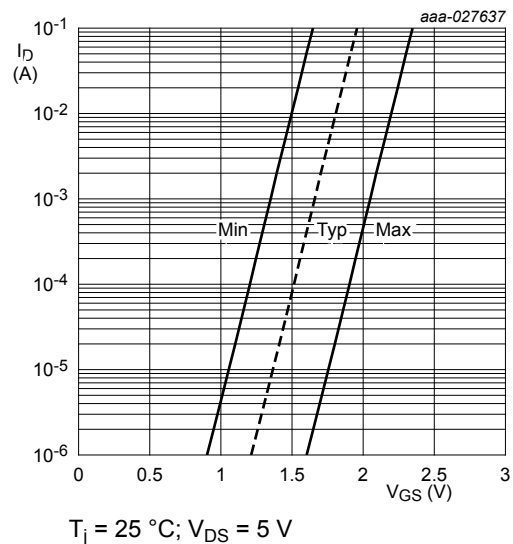
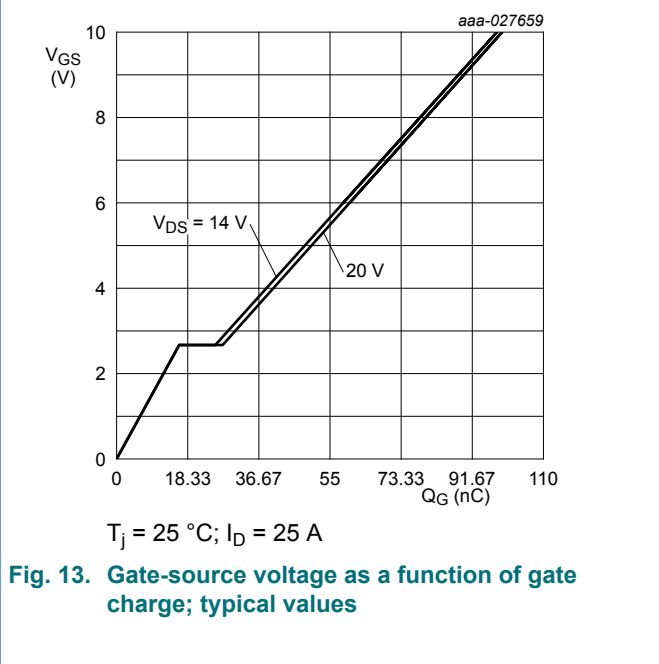
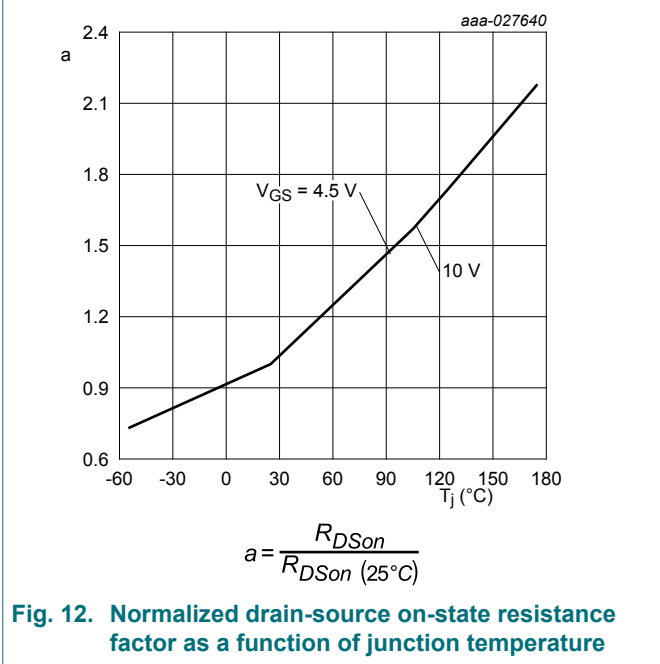
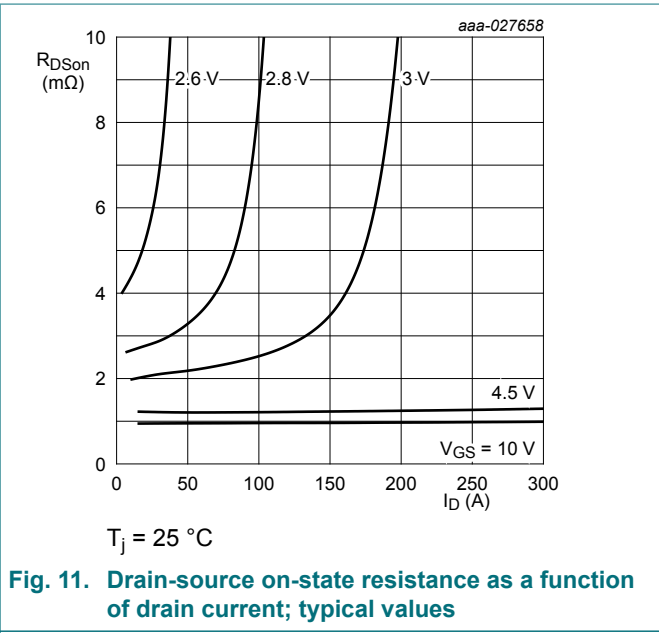
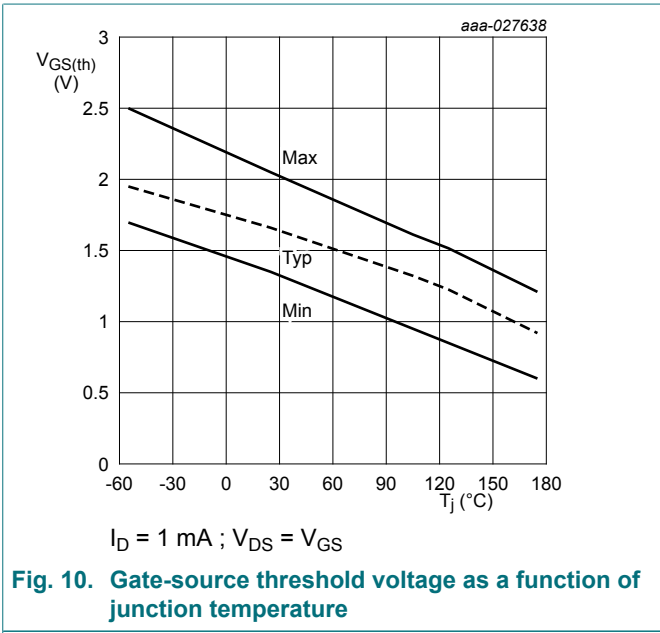


Fig. 9. Sub-threshold drain current as a function of gate-source voltage



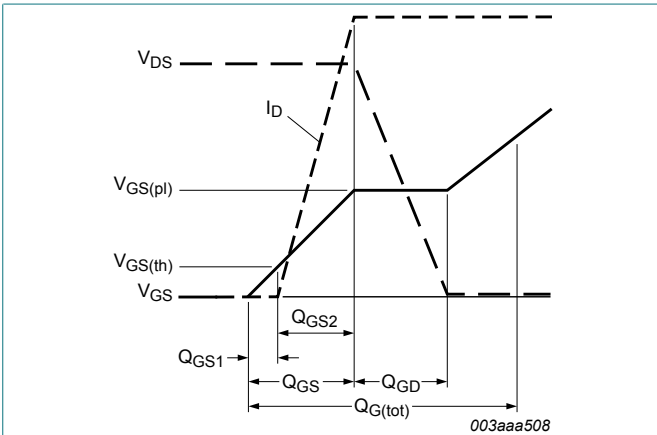


Fig. 14. Gate charge waveform definitions

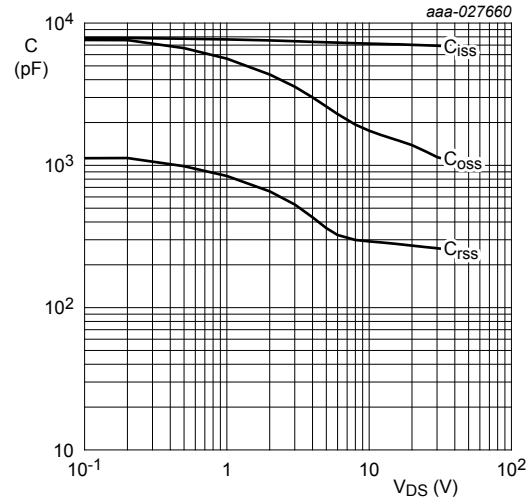


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

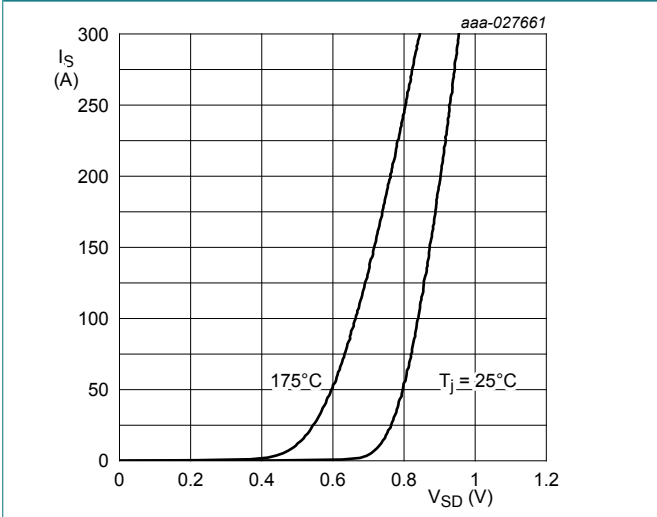


Fig. 16. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

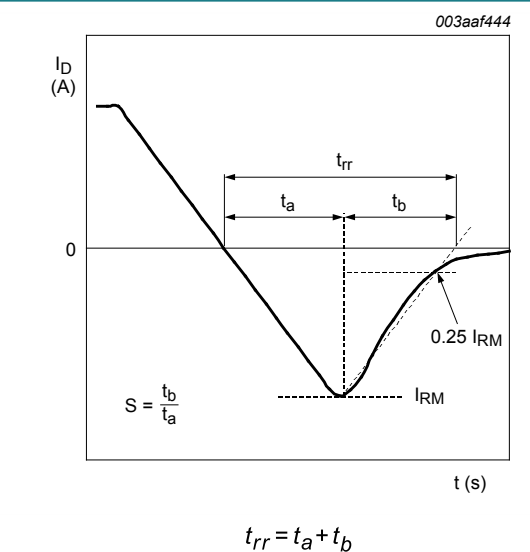


Fig. 17. Reverse recovery waveform definitions

11. Package outline

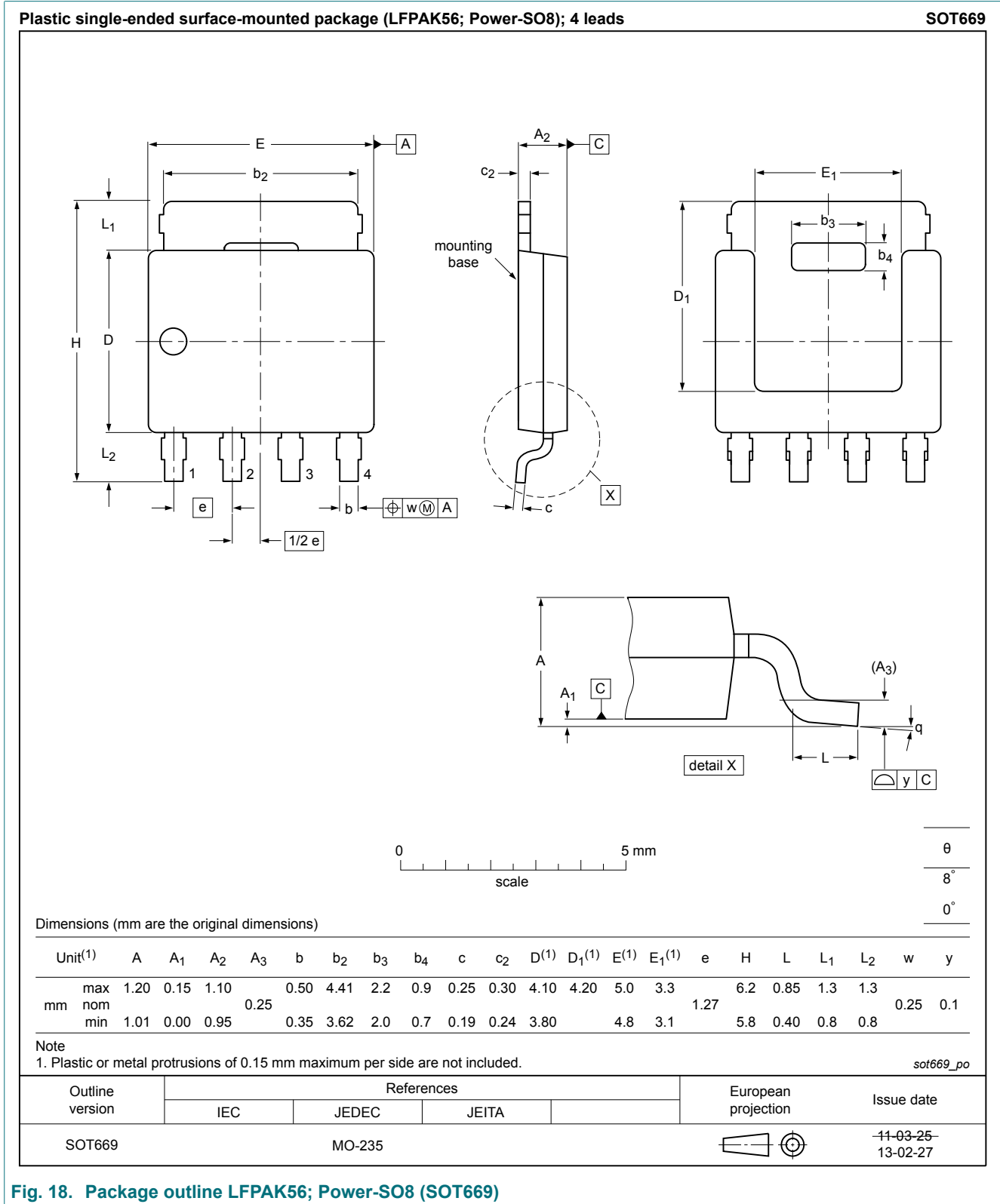


Fig. 18. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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